Chapter 5 An Autozeroing Floating-Gate Amplifier

This chapter presents a bandpass floating-gate amplifier that uses tunneling and pFET hot-electron injection so that it can return to its sensitive region despite large changes in the DC input voltage. Offsets often present a difficult problem for designers of MOS analog circuits. A time-honored tradition for addressing this problem is to use a blocking capacitor to eliminate the input DC component; however, for integrated filters, this approach requires enormous input capacitors and resistors to get time constants of less than 1Hz. Existing on-chip autozeroing techniques rely on clocking schemes that compute the input offset periodically, then subtract the correction from the input [85]. These autozeroing techniques add significant complexity to the circuit, as well as clock noise, aliasing, etc.

This chapter presents the *autozeroing floating-gate amplifier* (AFGA). The AFGA is an integrated continuous-time filter that is intrinsically autozeroing. It can achieve a high-pass characteristic at frequencies well below 1Hz. In contrast with conventional autozeroing amplifiers that eliminate their input offset, the AFGA nulls its output offset. The AFGA is a continuous-time filter; it does not require any clocking. The AFGA is the first known application of pFET hot-electron injection. Until now, pFET hot-electron injection has attracted attention only as a source of MOSFET oxide degradation [86]. The autozeroing technique used in the AFGA can be applied to a wide variety of floating-gate MOS circuits (FGMOS) to continuously restore a desired baseline operation on a slow timescale.

Section 5.1 gives a qualitative overview of AFGA operation. Section 5.2 considers how the steady-state voltage varies with the circuit parameters—most notably with the tunneling voltage and the nFET bias current. Section 5.3 considers the AFGA's high-pass filter behavior, and addresses long-term parameter drift. Section

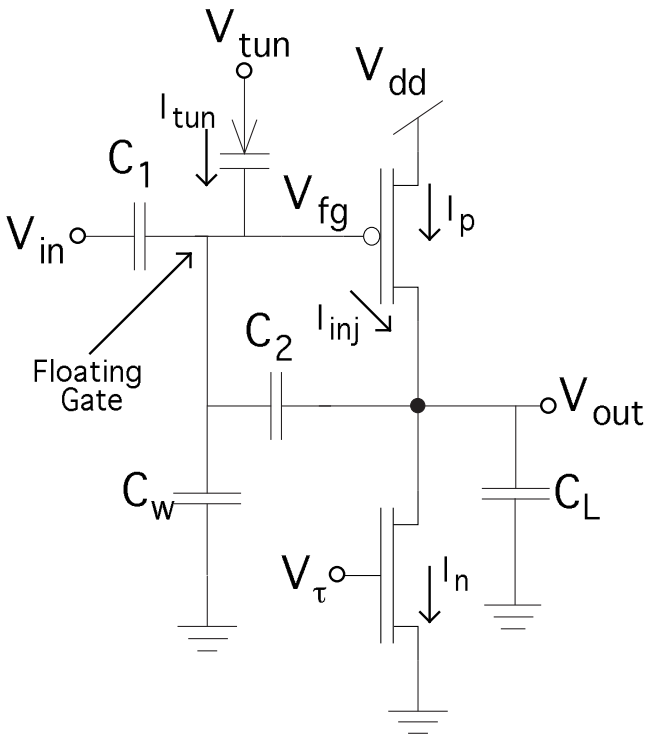


Figure 5.1: An autozeroing floating-gate amplifier (AFGA) that uses pFET hot-electron injection. The ratio of C_2 to C_1 sets the gain of this inverting amplifier. The nFET is a current source, and it sets the current through the pFET. Steady state occurs when the injection current is equal to the tunneling current. The capacitance from the floating gate to ground, C_w, represents both the parasitic and the explicitly drawn capacitances. Increasing C_w will increase the linear input range of the circuit. The capacitance connected to the output terminal, C_L, is the load capacitance. Between V_{tun} and V_{fg} is our symbol for a tunneling junction, which is a capacitor between the floating-gate and an $n$well.

5.4 considers the AFGA's low-pass filter behavior. Section 5.5 describes the AFGA's frequency response and dynamic range. Section 5.6 investigates how the steady-state voltage changes with input signal amplitude. Up to that point, this chapter will have primarily considered the AFGA biased with subthreshold currents; the discussion in Section 5.7 considers the differences in circuit operation when the AFGA is biased with above-threshold currents. Section 5.7 also discusses other AFGA effects. I will present some conclusions Section 5.8.

5.1 Qualitative Presentation of AFGA Operation

Figure 5.1 shows the autozeroing floating-gate amplifier. The open-loop amplifier consists of a pFET input transistor and an nFET current source. With capacitive feedback, the input signal is amplified by a closed-loop gain approximately equal to $-\frac{C_1}{C_2}$. The maximum gain is limited both by the open-loop gain, and by the parasitic floating-gate–to–drain overlap capacitance.

The complementary tunneling and hot-electron injection processes adjust the floating-gate charge such that the amplifier's output voltage returns to a steady-state value on a slow time scale. If the output voltage is below its equilibrium value, then the injection current exceeds the tunneling current, decreasing the charge on the floating gate; that, in turn, increases the output voltage back toward its equilibrium value. If the output voltage is above its equilibrium value, then the tunneling current exceeds the injection current, increasing the charge on the floating gate; that, in turn, decreases the output voltage back toward its equilibrium value. The circuit behaves like a high-pass filter with a long time constant.

Two conditions must be satisfied for the circuit to be in equilibrium. First, the pFET channel current, I_p, must be equal to the nFET channel current, I_n. I shall define this quiescent channel current as I_{s0}. Second, the injection gate current must be equal to the tunneling gate current. I shall define I_{inj0} as the quiescent injection current that must equal I_{tun0}, the quiescent tunneling current, at equilibrium. Since the tunneling and injection currents are many orders of magnitude smaller than I_{so} and are charging similar-sized capacitances, the first condition is satisfied much faster than is the second condition. The frequency range over which the first condition is satisfied, but the second condition is not satisfied, is where the AFGA behaves as an amplifier. The combination of electron tunneling and pFET hot-electron injection applies the appropriate negative feedback to stabilize the output voltage such that the second condition also is satisfied.

In the frequency range where the first condition does not hold, the output voltage is attenuated. In this regime, the circuit behaves as a low-pass filter. Since the

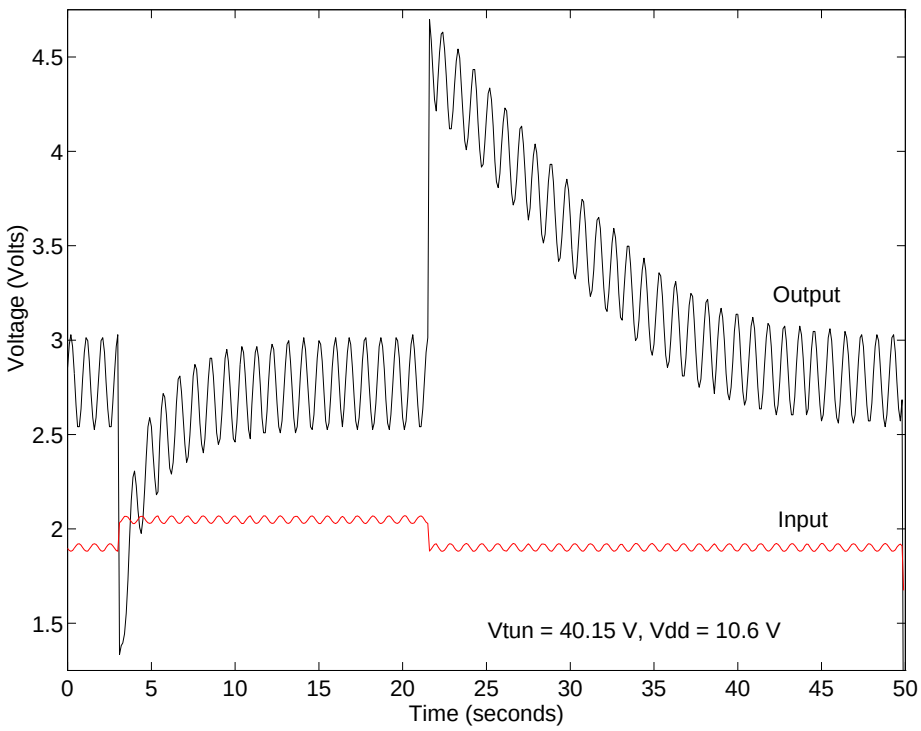


Figure 5.2: Response of the AFGA to a 1Hz sinewave superimposed on a 19s voltage pulse. The AFGA has a closed-loop gain of 11.2, and a low-frequency cutoff at 100mHz. The 1Hz signal is amplified, but the much slower step is adapted away.

output capacitances are charged or discharged by currents on the scale of I_{s0}, the cutoff frequency will be directly dependent on the bias current. Continuous-time integrators operate on a similar principle [87, 82]. The AFGA transfer function is a bandpass, with the low-frequency cutoff set by the equilibrium tunneling and injection currents, and the high-pass cutoff independently set by the equilibrium pFET and nFET channel currents.

Figure 5.2 shows the response of the autozeroing floating-gate amplifier to a 1Hz sine wave superimposed on an input pulse. If the input changes on a timescale that is much shorter than the adaptation, then the output is an amplified version of the input signal. The amplifier adapts to the pulse input after an initial transient, while preserving the amplified 1Hz sine wave.

Before proceeding, let us consider the behavior of the Early voltage, because

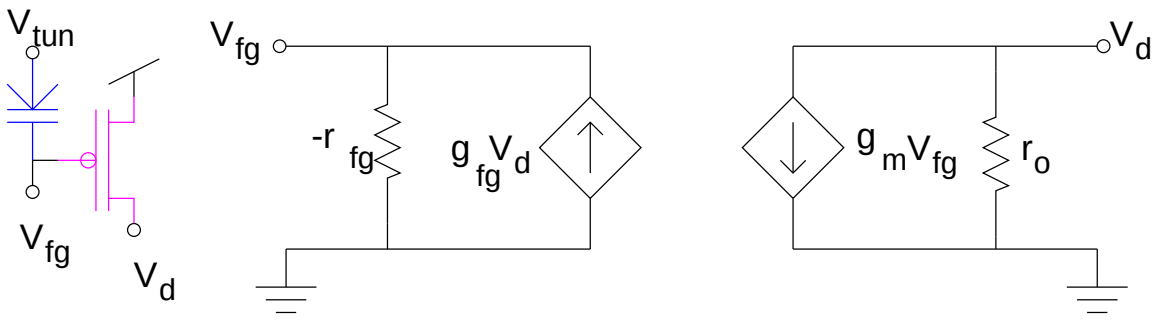


Figure 5.3: The small-signal model of a pFET with the effects of hot-electron injection. I assume a constant tunneling current at the floating gate (V_{fg}); this tunneling current sets the bias point for the hot-electron injection parameters.

the Early voltage is directly related to the amplifier's open-loop gain. Figure 5.3 reviews the small-signal model of a pFET that includes the effects of tunneling and hot-electron injection. Following the conventional definitions of small-signal transconductance, g_m, and output resistance, r_o [81], we obtain

$$g_m = \frac{\kappa I_{so}}{U_T}, \quad \text{and} \quad r_o = \frac{V_o}{I_{so}}, \tag{5.1}$$

for a subthreshold pFET. Figure 5.4 shows how the Early voltage, V_o, changes when the FETs operate with large drain-to-source voltages. The Early voltage decreases at large drain-to-source voltages due to impact ionization in the drain-to-channel depletion region. In the drain-to-channel depletion region, holes are accelerated to large energies; if a hole has an energy larger than the bandgap, then it may undergo impact ionization. The result of an impact ionization is two holes and one electron. For the nFET biased with a drain-to-source voltage of 3.0V and the pFET biased with a drain-to-source voltage of 8.5V, V_o is nearly constant for both transistors; therefore the AFGA's open-loop gain is also nearly constant. For the amplifiers presented in this chapter, the maximum open-loop gain is roughly 1400. The definitions of the small-signal quantities, g_{fg} and r_{fg}, were presented in Chapter 4.

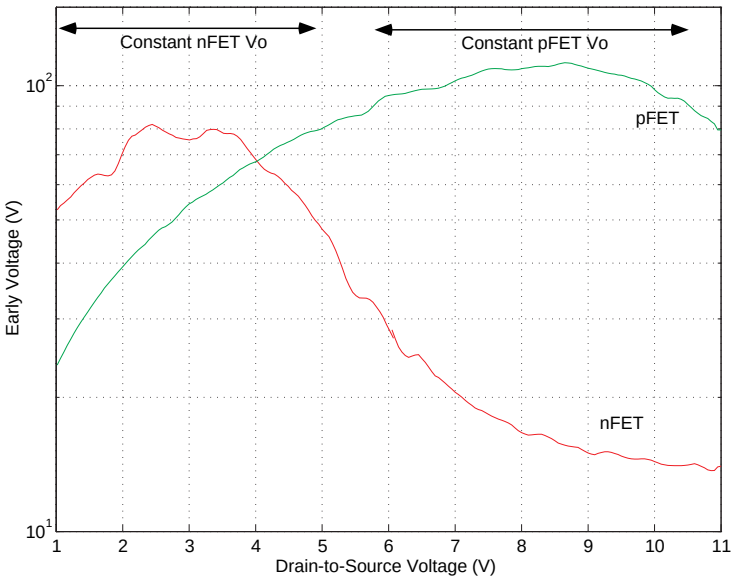


Figure 5.4: The effect of drain-to-source voltage on the Early voltage of an nFET and pFET. The AFGA's open loop-gain as a function of the output voltage is directly related to the change in the Early voltage. The decrease in the nFET's Early voltage at high drain-to-source voltages is due to the impact ionization in its drain-to-channel depletion region. For typical steady-state output voltages around 1V to 5V, the Early voltage of both the pFET and nFET are nearly constant; therefore, the open-loop gain is constant.

5.2 Equilibrium Voltages of the AFGA

Qualitatively, two factors change the steady-state output voltage. For the injection current to match the tunneling current after a change in V_τ or V_{tun}, the output voltage must reach a new equilibrium. Increasing the bias voltage or channel current requires increasing in the output voltage, because the pFET must reduce its injection efficiency so that the injection current matches the original tunneling current. Increasing the tunneling voltage, which increases the steady-state tunneling current, requires decreasing the output voltage, because the pFET must increase its injection efficiency so that the injection current matches the new tunneling current.

In Section 5.1, I postulated two conditions for equilibrium; now I describe them quantitatively. I assume an initial operating point, and consider changes in the steady-state output voltage in response to a change in V_τ or in V_{tun}, as in Chapter 3. First,

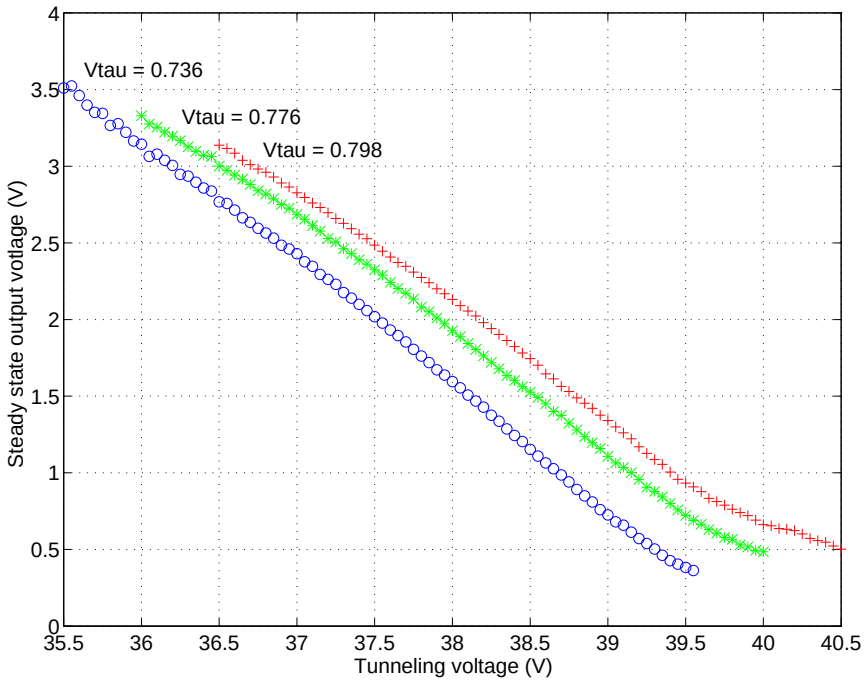


Figure 5.5: Steady-state output voltage versus the tunneling voltage for three values of V_τ. This data set agrees with the model described in (5.5). The AC gain of this amplifier was 146.

the current in the nFET must be equal to the current in the pFET:

$$\begin{aligned} I_n &= I_p, \\ I_{so} \exp\left(\frac{\kappa_n \Delta V_\tau}{U_T}\right) &= I_{so} \exp\left(\frac{-\kappa \Delta V_{fg}}{U_T}\right), \end{aligned} \tag{5.2}$$

where ΔV_τ is the change in the bias voltage, and ΔV_{fg} is the change in the pFET's floating-gate voltage. Therefore, we can solve for the relation

$$\Delta V_{fg} = -\frac{\kappa_n}{\kappa} \Delta V_\tau. \tag{5.3}$$

Qualitatively, the bias current in the nFET sets the current in the pFET, and therefore sets the floating-gate voltage.

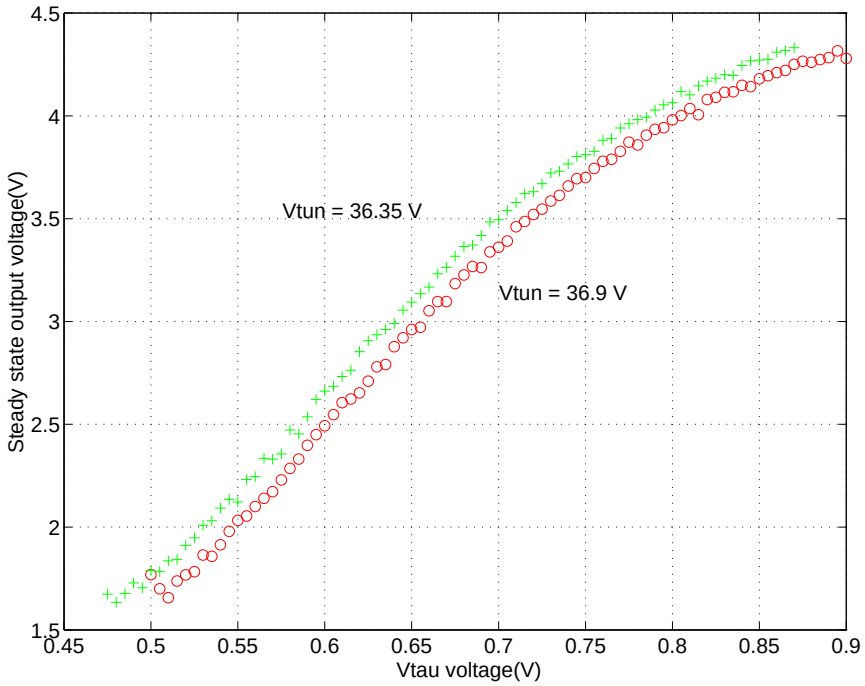


Figure 5.6: Steady-state output voltage versus V_τ for two tunneling voltages. This data set agrees with the model described in (5.5). The AC gain of this amplifier was 146.

Second, the tunneling current must be equal to the injection current:

$$I_{inj0} e^{-\frac{\alpha\kappa\Delta V_{fg}}{U_T}} e^{\frac{-\Delta V_{out}}{V_{inj}}} = I_{tun0} e^{\frac{\Delta V_{tun} - \Delta V_{fg}}{V_x}}. \tag{5.4}$$

I assume that I_{inj0} is equal to I_{tun0} at the initial operating point. Then, we obtain the second equilibrium relationship:

$$\Delta V_{out} = -\frac{V_{inj}}{V_x}\Delta V_{tun} + V_{inj}\frac{\kappa_n}{\kappa}\left(\frac{\alpha\kappa}{U_T} - \frac{1}{V_x}\right)\Delta V_\tau. \tag{5.5}$$

For above-threshold operation, the above equation becomes

$$\Delta V_{out} = -\frac{V_{inj}}{V_x}\Delta V_{tun} + V_{inj}\frac{\kappa_n}{\kappa}\left(\frac{2}{V_{dd} - V_{fg} + V_T} - \frac{1}{V_x}\right)\Delta V_\tau. \tag{5.6}$$

Figures 5.5 and 5.6 show the measured equilibrium output voltage as a function of the bias parameters for an AFGA with a gain of 146. Figure 5.5 shows the equilibrium

output voltage versus the tunneling voltage. Figure 5.6 shows the equilibrium output voltage versus the bias current; the curves begin to saturate for above-threshold bias currents, as predicted by (5.6).

An amplifier should be insensitive to variations in the bias voltages; the data in Figs. 5.5 and 5.6 show the circuit's DC sensitivity to V_τ and V_{tun}. First, the DC gain from the tunneling node to the output is given by $\frac{V_{inj}}{V_x}$, which, for this measured data, is 0.64. The DC gain from the nFET gate to the output is given by $V_{inj}\frac{\kappa_n}{\kappa}\left(\frac{\alpha\kappa}{U_T}-\frac{1}{V_x}\right)$, which, for this measured data, is 10. The DC gain from the input to the output is zero. All three DC gains are smaller than the AFGA AC gain of 146.

The power-supply rejection depends on the choice of reference. With the input and output referenced to V_{dd}, and with V_τ referred to GND, the AFGA gain from the power-supply to the output is 0.1, which results in a power-supply rejection ratio in the passband of 64dB. The power-supply rejection ratio is limited by the open-loop gain of the amplifier. If we instead refer all nodes to GND, the AC power supply gain is 146, which decreases the power-supply rejection ratio to 0dB. The circuit designer must also be careful of where the floating-gate capacitances are connected; for good power-supply rejection, all these capacitors must be referenced to V_{dd}. Otherwise, the power supply becomes another input to the AFGA, and any AC power supply noise will appear at the output, amplified by the AFGA's AC gain.

The steady-state output voltage and the high-pass cutoff frequency are set explicitly by V_{tun} and by the power-supply voltage. Increasing V_{tun} increases the tunneling current, which in turn decreases the settling time, but also decreases the steady-state output voltage, since the pFET must increase its drain-to-source voltage. Increasing the power-supply voltage decreases the tunneling current by decreasing the voltage across the oxide, increasing the settling time and increasing the steady-state output voltage.

5.3 Low-Frequency AFGA Behavior

The quantitative AFGA dynamics are described by two general equations governing the autozeroing floating-gate amplifier around an equilibrium output voltage. We can obtain the first equation by applying Kirchoff's current law (KCL) at the floating gate:

$$(C_1 + C_2 + C_w)\frac{dV_{fg}}{dt} = C_1\frac{dV_{in}}{dt} + C_2\frac{dV_{out}}{dt} + I_{tun0}\left(1 - \exp\left(-\alpha\frac{\kappa\Delta V_{fg}}{U_T} - \frac{\Delta V_{out}}{V_{inj}}\right)\right). \tag{5.7}$$

We can obtain the second equation by applying KCL at the output node:

$$(C_2 + C_L)\frac{dV_{out}}{dt} = C_2\frac{dV_{fg}}{dt} + I_\tau\left(\exp\left(-\frac{\kappa\Delta V_{fg}}{U_T}\right) - 1\right). \tag{5.8}$$

I have neglected the Early effect, which adds a correction term to (5.8). As long as the closed-loop gain is much lower than the amplifier gain, ignoring the Early effect is a good approximation.

In the passband, where the AFGA is an amplifier, the floating gate is held nearly constant by the amplifier feedback, and the tunneling and injection currents are negligible. This approximation simplifies (5.7) to

$$C_2\frac{dV_{out}}{dt} = -C_1\frac{dV_{in}}{dt}; \tag{5.9}$$

thus, the change in the output voltage (ΔV_{out}) is equal to the input voltage (ΔV_{in}) amplified by $-\frac{C_1}{C_2}$.

5.3.1 Low-Frequency Model

I make an approximation to model the low-frequency response of the AFGA. The open-loop gain from the floating gate to the output can be large. If the output voltage is to be kept between the supply rails, the floating-gate voltage must be confined to a 10mV swing. Thus, I approximate the floating-gate voltage to be constant. Therefore, because the floating-gate voltage is nearly constant, the source

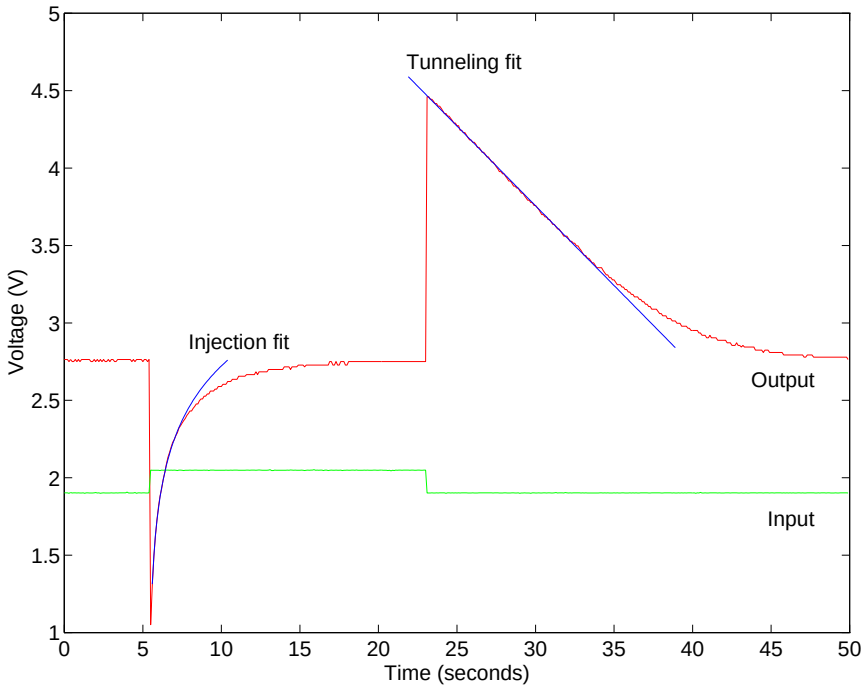


Figure 5.7: Response of the AFGA to an upgoing and a downgoing step input. The adaptation in response to an upward step results from electron tunneling; the adaptation in response to a downward step results from pFET hot-electron injection. This amplifier had a gain of 11.2. I plot the curve fits of the simplified expressions of (5.17), where either tunneling or injection dominates the restoration process. Using the curve fits, τ is 4.3s and I_{tun0} is 50fA. The value of τ can be set reliably to more than 10^5 seconds.

current varies only slightly. The quiescent source current (I_{s0}) is set by the nFET current source. From (3.17), the model of injection current for a fixed a source current I_{s0} is

$$I_{tun} - I_{inj} = I_{tun0}\left(1 - \exp\left(-\frac{\Delta V_{out}}{V_{inj}}\right)\right), \tag{5.10}$$

where $I_{tun0} = I_{inj0}$ for the circuit in equilibrium. Since the floating gate is held nearly constant by feedback, the floating-gate voltage dependence in (3.17) is negligible. Even when the circuit is biased with above-threshold currents, the tunneling current still remains nearly constant. Since the injection efficiency is still an exponential function of the drain voltage for above-threshold currents, the low-frequency dynamics are similar in below- and above-threshold operation.

With the preceding approximations, we can model the amplifier's output voltage,

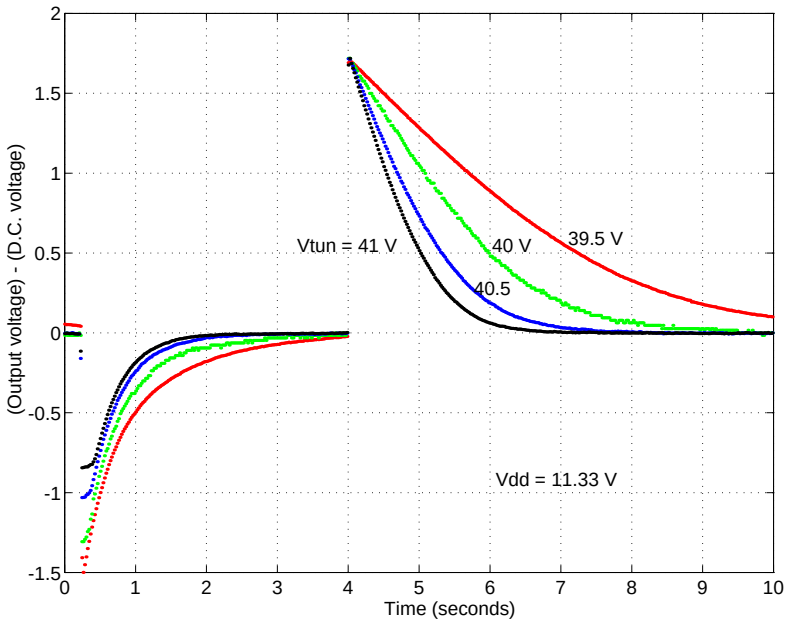


Figure 5.8: The response to a square wave for four different values of the tunneling voltage. This amplifier had a gain of 147; the input square wave is not shown. The steady-state output voltage decreased in the same manner as seen in Fig. 5.5 for increasing tunneling voltages. The initial tail in the upgoing response is due to the output voltage going to ground.

V_{out}, in terms of V_{in}, with a single equation. The total floating-gate current is the sum of the capacitive currents of the input and output terminals, plus the tunneling and injection currents. From (5.7) I write

$$C_2 \frac{dV_{out}}{dt} = -C_1 \frac{dV_{in}}{dt} + I_{tun0} \left(\exp\left(-\frac{\Delta V_{out}}{V_{inj}} \right) - 1 \right). \tag{5.11}$$

To solve (5.11), I make the following change of variables:

$$X = e^{\frac{\Delta V_{out}}{V_{inj}}}. \tag{5.12}$$

The resulting equation for X is a linear, first-order differential equation with variable coefficients

$$\tau_l \frac{dX}{dt} = -\frac{\tau_l A_v X}{V_{inj}} \frac{dV_{in}}{dt} + 1 - X, \tag{5.13}$$

where τ_l, the low-frequency cutoff, is equal to $\frac{C_2 V_{inj}}{I_{tun0}}$, and A_v is the closed-loop AC gain of the amplifier, $-\frac{C_1}{C_2}$.

5.3.2 Response to a Voltage Step

Consider the AFGA's response to an input voltage step. Assume that the output voltage initially has adapted to its steady-state value. To solve (5.13), I first assume that the output voltage immediately after applying the step, $\Delta V_{out}(0^+)$, is given by the magnitude of the input step times the AFGA AC gain. I employ $\Delta V_{out}(0^+)$ as a new effective initial condition, and denote the effective initial condition in X by

$$X(0^+) = \exp\left(\frac{V_{out}(0^+)}{V_{inj}}\right). \tag{5.14}$$

For a downward step, $X(0^+)$ is greater than 1; for an upward step, $X(0^+)$ is less than 1. After the input step, $\frac{dV_{in}}{dt} = 0$; therefore (5.13) becomes

$$\begin{cases} \tau_l \frac{dX}{dt} = 1 - X \\ X(0) = X(0^+). \end{cases} \tag{5.15}$$

The solution to (5.15) in terms of ΔV_{out} is

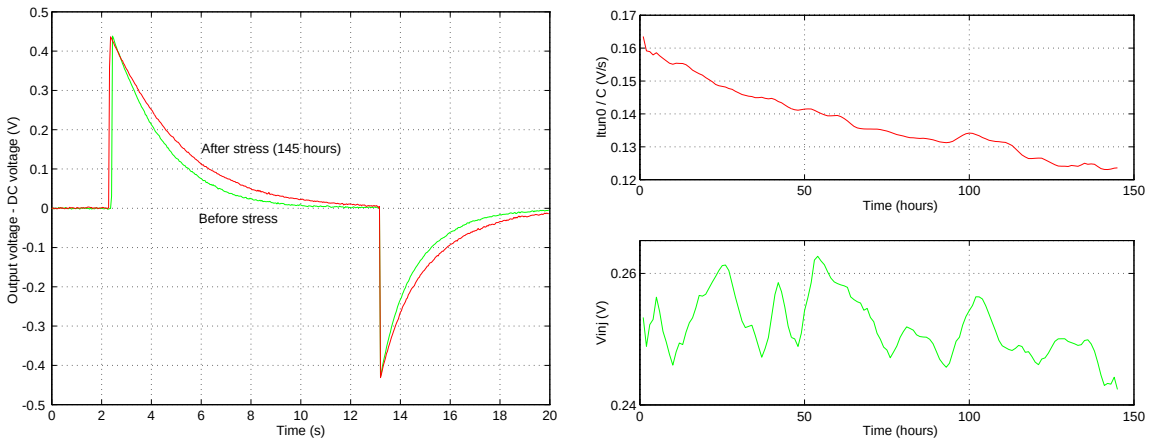
$$\Delta V_{out}(t) = V_{inj} \ln\left(1 + \left(X(0^+) - 1\right) e^{-\frac{t}{\tau_l}}\right), \tag{5.16}$$

where $\Delta V_{out} \to 0$ as $t \to \infty$.

The step response has three interesting regimes, which are approximated by

$$\Delta V_{out} \approx \begin{cases} \Delta V_{out}(0^+) e^{-\frac{t}{\tau_l}}, & X(0^+) \approx 1, \\ \Delta V_{out}(0^+) - \frac{I_{tun0}}{C_2} t, & X(0^+) \gg 1, \\ V_{inj} \ln\left(X(0^+) + \frac{t}{\tau_l}\right), & X(0^+) \ll 1. \end{cases} \tag{5.17}$$

The first case occurs when the tunneling current is nearly equal to the injection current just after the voltage step. The solution in this region is the familiar exponential decay



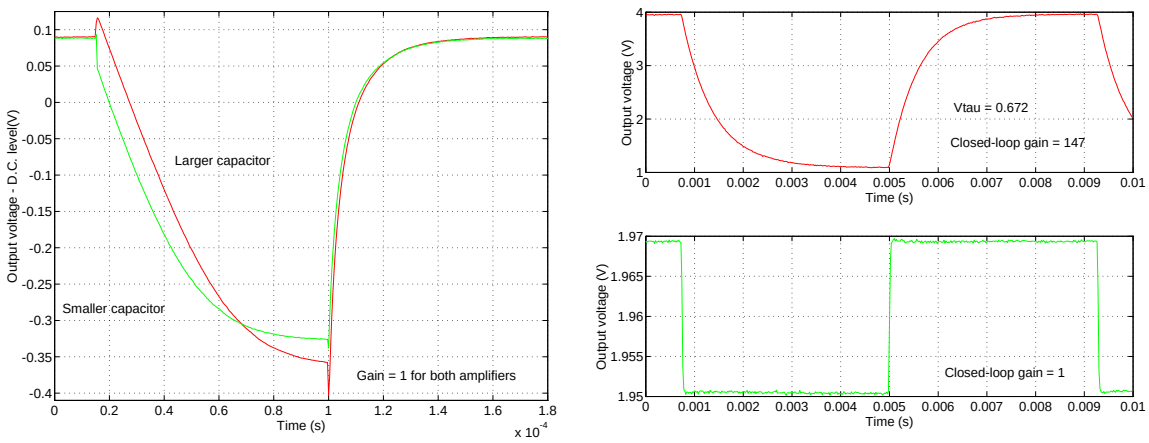
(a) (b)

Figure 5.9: The effect of long-duration AFGA operation. (a) The responses to an upgoing and downgoing voltage step before and after 145 hours of operation. I plot the difference in the output voltage from the equilibrium DC level as a function of time; the equilibrium output voltage increased slightly over the 145 hours of operation. (b) The extracted device parameters as a function of time. Since I_{tun0}/C_2 changes more than does V_{inj}, most of the long-term change is caused from the tunneling junction, which is probably caused by oxide trapping.

of a linear system. The second case occurs when the tunneling current dominates the injection current. The behavior of the output voltage in this regime results from the constant tunneling current removing electrons from the floating gate. The third case occurs when the injection current dominates the tunneling current. Figure 5.7 shows a measured response to an input pulse, with curve fits to the regions where either the tunneling or injection current dominates.

5.3.3 Long-Term Parameter Drift

The physical properties of the tunneling and hot-electron injection mechanisms change with time. These processes are permanently modified as electrons pass through the oxide, creating electron traps. I investigated the long-term changes by performing an accelerated stress experiment, where I operated an AFGA continuously for 145 hours with an average τ_l of 1.7s. When an AFGA is used as an amplifier or as a



(a) (b)

Figure 5.10: High-frequency AFGA behavior. (a) Two AFGAs with unity gain, but with different values for C_1. The larger-capacitor circuit had $C_1 = C_2 = 300$ fF; the smaller-capacitor circuit had $C_1 = C_2 = 50$ fF. For both AFGAs, C_L was the same. I operated the two AFGAs with different subthreshold bias currents to achieve comparable settling times. (b) Two AFGAs with different gains.

low-pass filter, a more reasonable τ_l would be at least several minutes; therefore, this experiment represents the stress of operating the AFGA continuously for a few years. The effect of an input signal only slightly modifies the results of this experiment. To characterize the behavior of the AFGA over time, I performed a square wave experiment similar to the one shown in Fig. 5.7, once per hour for 145 hours. To each of the resulting output waveforms, I fit the expressions of (5.17) and extracted the relevant device parameters. Figure 5.9a shows the square-wave response of the AFGA before and after this lifetime test. The adaptation time constant has increased noticeably, but the general behavior is unaffected. Figure 5.9b shows the change in the extracted parameters during the experiment. Since I_{tun0}/C_2 changes more than V_{inj}, we see that most of the long-term change is due to changes in the tunneling junction, which is probably a consequence of electron trapping.

5.4 High-Frequency AFGA Behavior

For sufficiently high frequencies, the autozeroing floating-gate amplifier is a low-pass filter. In this regime, the tunneling and injection currents are negligible; therefore we approximate (5.7) as

$$(C_1 + C_2 + C_w)\frac{dV_{fg}}{dt} = C_1\frac{dV_{in}}{dt} + C_2\frac{dV_{out}}{dt}. \tag{5.18}$$

From (5.18), we see that changes in V_{out} are proportional to changes in V_{fg} and V_{in}. At extremely high frequencies, the transistor channel currents are negligible compared to the capacitive currents. In this capacitive-feedthrough regime, the solutions to (5.8) and (5.18) are

$$\begin{aligned} \frac{\Delta V_{fg}}{\Delta V_{in}} &= \frac{C_1(C_2+C_L)}{(C_1+C_2+C_w)(C_2+C_L)-C_2^2}, \\ \frac{\Delta V_{out}}{\Delta V_{in}} &= \frac{C_1C_2}{(C_1+C_2+C_w)(C_2+C_L)-C_2^2}. \end{aligned} \tag{5.19}$$

We can reduce the effects of the capacitive feedthrough by increasing either C_L or C_W.

At frequencies between the low-frequency cutoff and the capacitive-feedthrough regime, the behavior of the AFGA results from the floating-gate voltage settling back to its equilibrium value. Therefore, we can combine (5.8) and (5.18) to form a single equation for the floating-gate voltage, which we write as

$$\begin{aligned} &\left((C_1 + C_2 + C_w)(C_2 + C_L) - C_2^2\right)\frac{dV_{fg}}{dt} = \\ &C_1(C_2 + C_L)\frac{dV_{in}}{dt} + C_2 I_\tau\left(e^{-\frac{\kappa\Delta V_{fg}}{U_T}} - 1\right). \end{aligned} \tag{5.20}$$

This equation is similar to (5.13), which describes the output-voltage response in the low-frequency case. Correspondingly, substituting

$$Y = e^{\frac{\kappa\Delta V_{fg}}{U_T}} \tag{5.21}$$

into (5.20) results in the linear differential equation

$$\tau_h \frac{dY}{dt} = \frac{\tau_{h2}\kappa}{U_T}\frac{dV_{in}}{dt}Y + 1 - Y, \tag{5.22}$$

where I shall define τ_{h2} to be

$$\tau_{h2} = \frac{C_1(C_2 + C_L)U_T}{\kappa C_2 I_\tau}, \tag{5.23}$$

which is the time constant that marks the onset of capacitive feedthrough. I shall define τ_h to be

$$\tau_h = \frac{((C_1 + C_2 + C_w)(C_2 + C_L) - C_2^2)\,U_T}{\kappa C_2 I_\tau}, \tag{5.24}$$

which represents the time constant for the high-frequency cutoff.

As we did in the low-frequency case, we shall consider the response to an input voltage step. To solve (5.22), I first assume that the floating-gate voltage immediately after applying the step, $\Delta V_{fg}(0^+)$, is given by the magnitude of the input step attenuated by the capacitive divider ratio, (5.19). With this initial condition, the solution is

$$\Delta V_{fg} = \frac{U_T}{\kappa} \ln\left(1 + \left(e^{\frac{\kappa \Delta V_{fg}(0^+)}{U_T}} - 1\right) e^{-\frac{t}{\tau_h}}\right). \tag{5.25}$$

After the initial jump, given by (5.19), the output voltage is related to the floating-gate voltage by

$$\Delta V_{out} = \frac{C_1 + C_2 + C_w}{C_2}\Delta V_{fg}. \tag{5.26}$$

Figure 5.10 shows measured AFGA output-voltage responses to several square-wave inputs. Figure 5.10a shows the responses of two unity-gain AFGAs with different capacitor values to the same square-wave input. As in the low-frequency case, the high-frequency response of the AFGA is asymmetric: the downgoing step response approaches its steady state linearly with time, and the upgoing step response approaches its steady state logarithmically with time. The initial jump in the downgoing step is due to capacitive feedthrough. From these data, it is evident that decreasing C_1 and C_2 without changing C_L will decrease the amount of capacitive feedthrough. Figure

5.10b shows the voltage responses, to a small input step, for two AFGAs with gains of 1 and 146. The response from the unity-gain AFGA is a buffered version of the input; the high-gain AFGA shows a linear, first-order, low-pass filtered version of the input. These responses illustrate the gain–bandwidth tradeoff in the AFGA.

The linear 3V output swing in the high-gain response of Fig. 5.10b raises this question: What determines the linear range of an AFGA? One criterion for linearity is that ΔV_{fg} be sufficiently small such that the factor $\left(\exp\left(-\frac{\kappa \Delta V_{fg}}{U_T}\right) - 1\right)$ in (5.20) can be approximated by $-\frac{\kappa \Delta V_{fg}}{U_T}$. This criterion implies that the floating-gate voltage must not move by more that $\frac{U_T}{\kappa}$ from its equilibrium value. The floating-gate voltage has its maximum swing in the capacitive-feedthrough regime; therefore, from (5.19), the input linear range, V_{Li}, is

$$V_{Li} = \frac{U_T}{\kappa}\left(\frac{C_1 + C_2 + C_w}{C_1}\right) B, \tag{5.27}$$

where I shall define

$$B = 1 - \frac{C_2^2}{(C_1 + C_2 + C_w)(C_L + C_2)}. \tag{5.28}$$

For amplifiers with gains greater than or equal to 1, which requires that C_1 be greater than C_2, B is bounded between $\frac{1}{2}$ and 1 for all C_1, C_2, C_W, and C_L. Further, if the AFGA is driving a C_L that is at least as big as C_1, B is bounded between $\frac{3}{4}$ and 1. Consequently, B can be considered a correction term.

I express the output linear range, V_{Lo}, in terms of the input linear range, V_{Li}, by

$$V_{Lo} = \frac{U_T}{\kappa}\left(\frac{C_1 + C_2 + C_w}{C_2}\right) B, \tag{5.29}$$

which is V_{Li} times the amplifier gain, C_1/C_2. The output linear range scales with the amplifier gain. By increasing C_w, I reduce the change in the floating-gate voltage, thereby increasing the amplifier's output linear range. The AFGA's gain from input to output in the passband is

$$\frac{V_{out}}{V_{in}} = -\left(\frac{C_1}{C_2}\right)\frac{1}{1 + \frac{C_1 + C_2 + C_W}{C_2 A}} = -\left(\frac{C_1}{C_2}\right)\frac{1}{1 + \frac{\kappa V_{Lo}}{A U_T B}}, \tag{5.30}$$

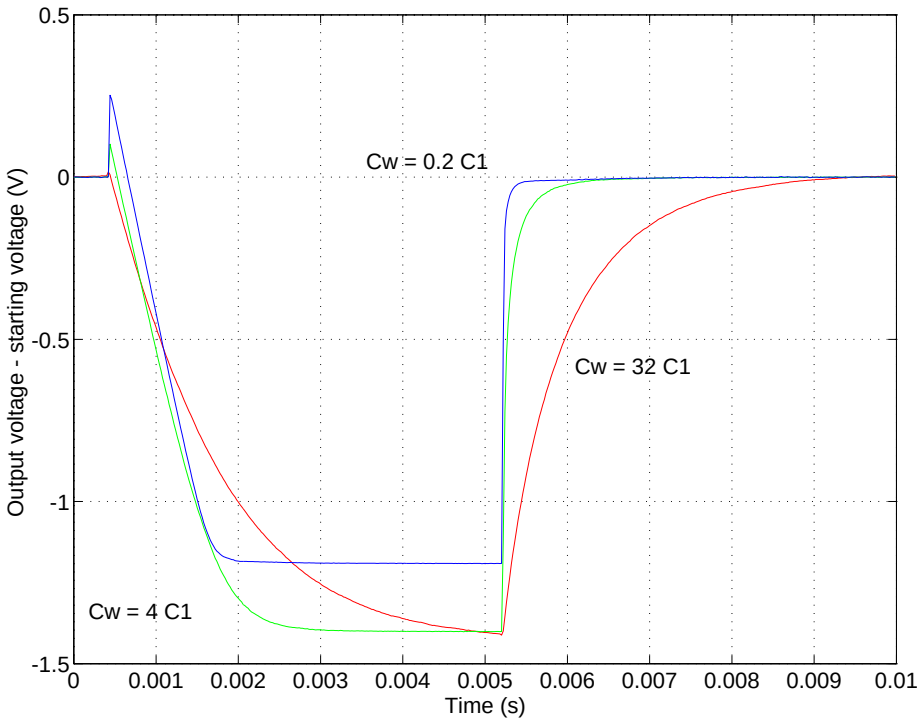


Figure 5.11: The response of three AFGAs to the same square-wave input. All three AFGAs were identical except for C_w, and were biased by the same V_τ. Increasing C_w increases the linear range, decreases the amount of capacitive feedthrough, and decreases the low-pass cutoff frequency.

where A is the gain from floating gate to output. For a sufficiently large A, the AFGA's passband gain is independent of C_w.

Figures 5.11 and 5.12 show measured data demonstrating how τ_h and linear range scale with C_w for unity-gain AFGAs. For a unity-gain AFGA—that is for $C_1 = C_2$—the expressions for τ_h and input linear range are

$$\tau_h = \frac{U_T(C_1 + C_L)}{\kappa I_\tau}\left(2 - \frac{C_1}{C_1 + C_L} + \frac{C_w}{C_1}\right), \tag{5.31}$$

and

$$V_{Li} = \frac{U_T}{\kappa}\left(2 - \frac{C_1}{C_1 + C_L} + \frac{C_w}{C_1}\right). \tag{5.32}$$

The data in Fig. 5.12 were taken with AFGAs that had no explicitly drawn C_L;

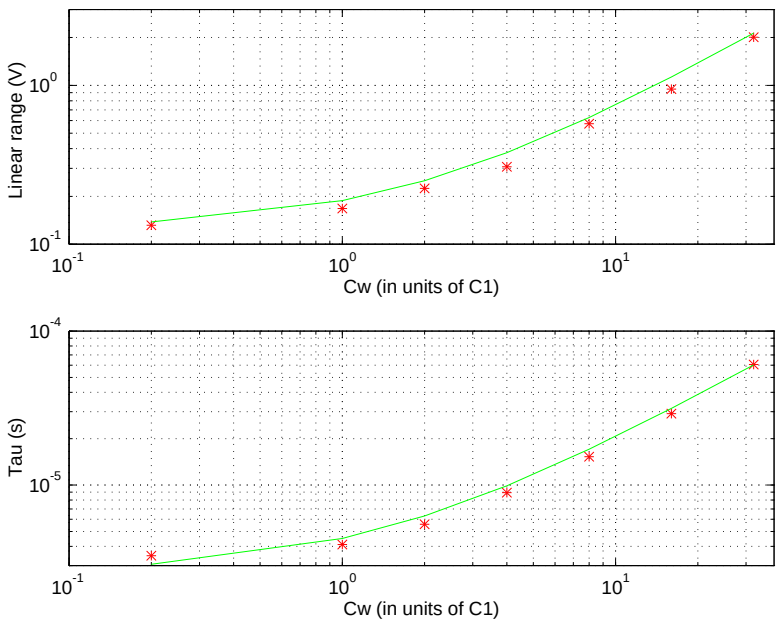


Figure 5.12: Measured linear range and τ_h for several unity-gain AFGAs for different C_w ratioed in units of C_1. The linear range fit is $V_{Li} = 0.063\text{V}\ C_w/C_1 + 0.125\text{V}$, and the τ fit is $\tau = 1.8\mu\text{s}\ C_w/C_1 + 2.7\mu\text{s}$.

the variation between the data and the linear curve fit is probably caused by the different parasitic load capacitances. Both the experimental data and the direct analytic solution of (5.22) indicate that second harmonic distortion dominates for the AFGAs; for a sine-wave input with amplitude of V_{Li}, the peak second harmonic distortion is 0.05 percent of (26dB below) the fundamental frequency response. The second harmonic distortion is maximum for frequencies just below $\frac{1}{2\pi\tau_h}$; for amplitudes at or below V_L, the second harmonic distortion is proportional to the square of the fundamental amplitude.

5.5 Frequency Response of the AFGA

To derive the AFGA frequency response, I begin with the small-signal form of

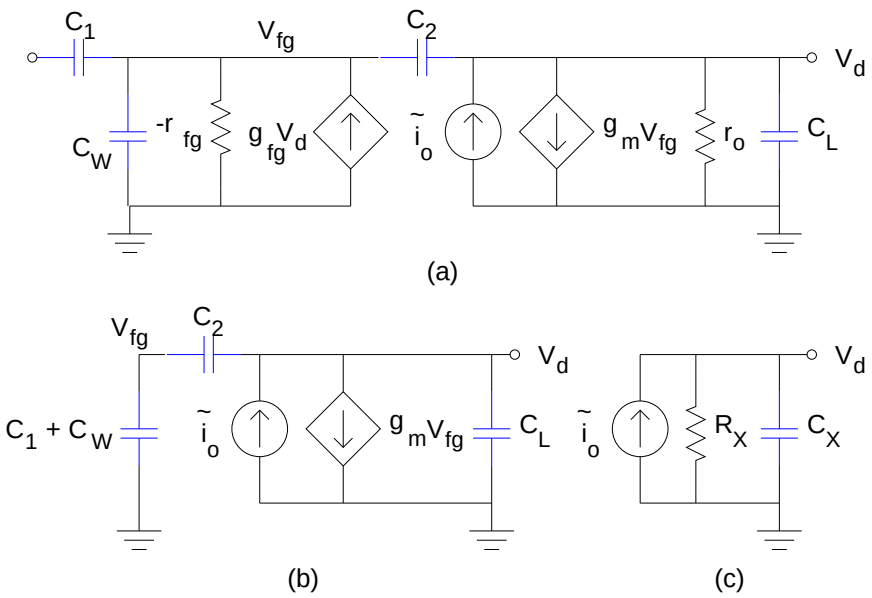


Figure 5.13: An AFGA represented as a small-signal circuit. (a) The small-signal AFGA model using the small-signal pFET model. (b) The small-signal model of the effect of the noise source in the channel on the output voltage. I have neglected the effect of the gate current, as well as the Early voltage effect, in this model. (c) A simplified small-signal model of the effect of noise. For clarity, I define $R_x = \frac{C_1+C_2+C_w}{g_m C_2}$, and $C_x = C_L + C_2\left(1 - \frac{C_2}{C_1+C_2+C_w}\right)$

(5.7) and (5.8):

$$(C_1 + C_2 + C_w)\frac{dV_{fg}}{dt} = C_1\frac{dV_{in}}{dt} + C_2\frac{dV_{out}}{dt} + \frac{I_{tun0}}{V_{inj}}\Delta V_{out},$$

$$(C_2 + C_L)\frac{dV_{out}}{dt} = C_2\frac{dV_{fg}}{dt} - \frac{\kappa I_\tau}{U_T}\Delta V_{fg}; \tag{5.33}$$

that is, I assume that the input signal is sufficiently small that I need to keep only the linear terms when we expand the exponentials. A small-signal input changes V_{out} by less than V_{inj}, due to the injection nonlinearity in the low-frequency regime, and change V_{fg} by less than $\frac{U_T}{\kappa}$, due to the transistor nonlinearity in the high-frequency regime. We can also obtain (5.33) by analyzing the small-signal circuit in Fig. 5.13a. I first discuss the response in the low- and high-frequency regimes, and then present the general solution.

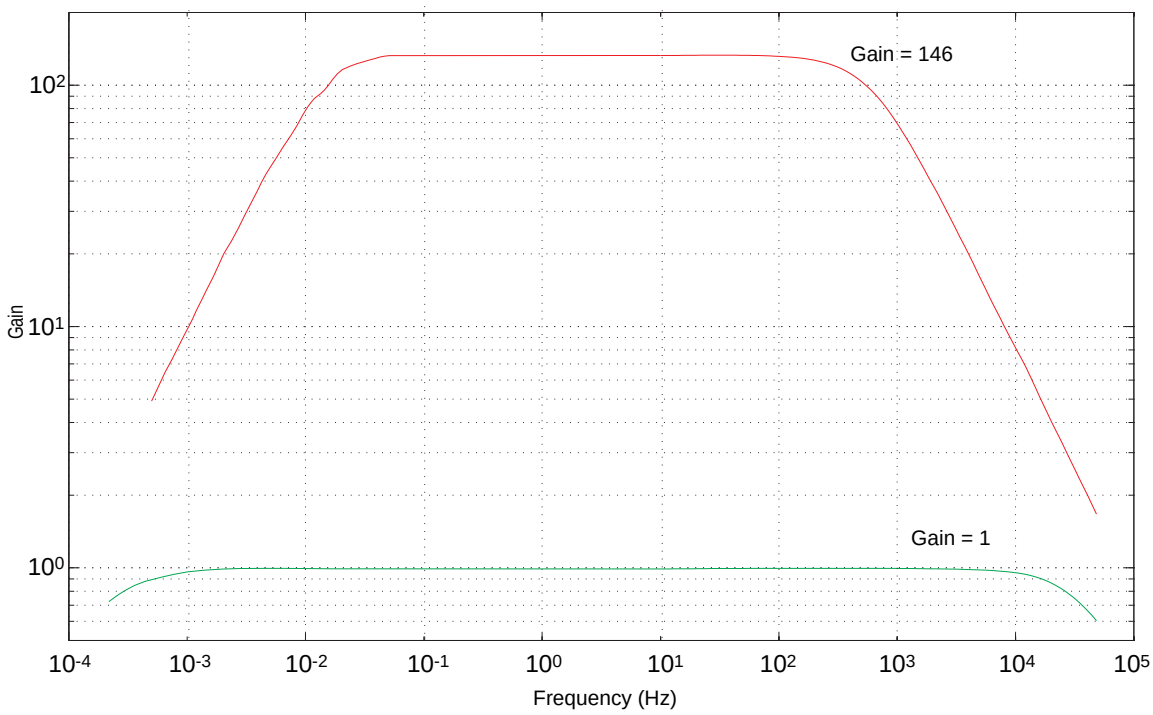


Figure 5.14: Frequency response for two AFGAs with different gains. For both the high- and low-gain AFGA, $C_1 + C_2$ is approximately constant. For the high-gain AFGA, τ_l is 20mHz, and τ_h is 600Hz; for the low-gain AFGA, τ_l is 300μHz and τ_h is 40kHz. The ratio of τ_h and τ_l between the two AFGAs are equal to one-half of the ratio of the gains; the ratio is consistent with a constant $C_1 + C_2$.

For low-frequency inputs, I approximate (5.33) as

$$\tau_l \frac{C_1}{C_2} \frac{dV_{in}}{dt} + \tau_l \frac{dV_{out}}{dt} = -\Delta V_{out}, \tag{5.34}$$

for which the resulting frequency response is

$$\frac{V_{out}(s)}{V_{in}(s)} = -\frac{C_1}{C_2} \frac{s\tau_l}{1 + s\tau_l}. \tag{5.35}$$

Figure 5.14 shows the measured AFGA frequency response: for the high-gain AFGA, τ_l is 20mHz; for the low-gain AFGA, τ_l is 300μHz. The high-gain AFGA has a gain of 146; the low-gain AFGA has unity gain.

For high-frequency inputs, I can simplify (5.33) by assuming input frequencies

much larger than $\frac{1}{2\pi\tau_l}$; I write the result as

$$\frac{V_{out}}{V_{in}} = -\frac{C_1}{C_2}\frac{1-\tau_{h2}s}{1+\tau_h s}. \tag{5.36}$$

This transfer function includes the effects of parasitic and load capacitances. The response in (5.36) is the transfer function of a first-order system; because we use capacitive feedback, the AFGA is stable for any value of closed-loop gain. As we can see in Fig. 5.14, $\frac{1}{2\pi\tau_h}$ is 500Hz for the high-gain AFGA, and is 40kHz for the low-gain AFGA.

To obtain the response for all frequencies, we can take the Laplace transform of (5.33):

$$s\left(C_1+C_2+C_w\right)V_{fg} = sC_1V_{in} + \left(sC_2 + \frac{I_{tun0}}{V_{inj}}\right)V_{out},$$

$$s\left(C_2+C_L\right)V_{out}(s) = \left(sC_2 + \frac{\kappa I_\tau}{U_T}\right)V_{fg}. \tag{5.37}$$

We can solve (5.37) to obtain

$$\frac{V_{out}(s)}{V_{in}(s)} = -\frac{C_1}{C_2}\frac{1-\tau_{h2}s}{1+\tau_h s+\frac{1}{\tau_l s}}, \tag{5.38}$$

where $\tau_l, \tau_h, \tau_{h2}$ are as defined previously.

When considering the frequency response of the AFGA, it is natural to consider the output-voltage spectrum for no input—that is, the output-voltage noise from the amplifier. Figures 5.15 and 5.16 show AFGA output-voltage spectra for a fixed, voltage-source input. For low frequencies, $1/f$ noise is dominant; for high frequencies, thermal noise dominates. The AFGA attenuates the $1/f$ noise below the low-frequency cutoff. Figure 5.15 shows that we can reduce the $1/f$ noise by increasing V_{tun}, and thereby decreasing τ_l. Figure 5.16 shows a comparison among a high-gain AFGA, a unity-gain AFGA, and a follower-connected transconductance amplifier. The transconductance amplifier is the wide-range amplifier described previously [82]; it has transistors larger than those of the AFGAs, resulting in the lower $1/f$ noise. The AFGAs used a constant tunneling current; because the noise spectrum of the unity-

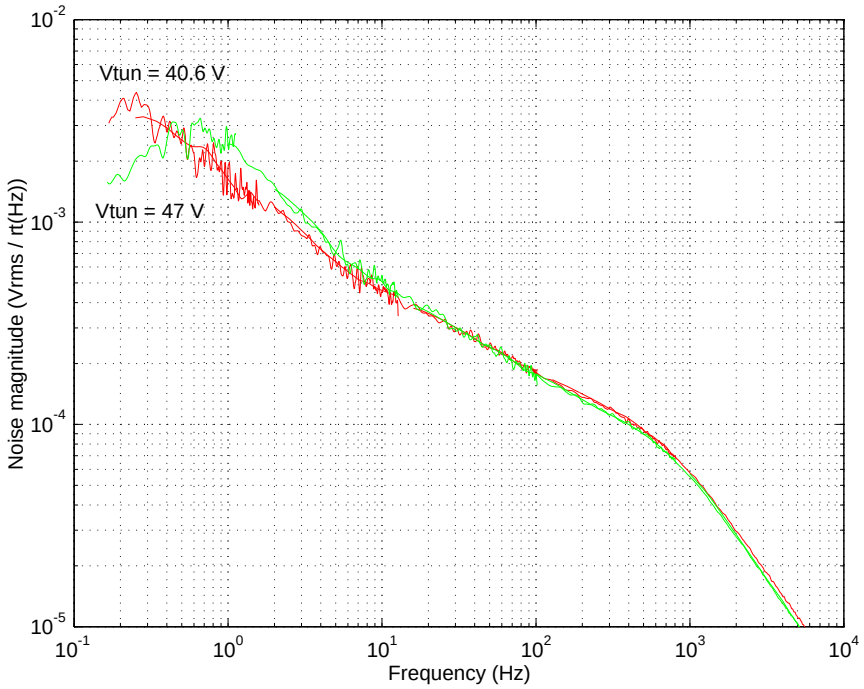


Figure 5.15: Output noise spectrum of an AFGA with a gain of 146 for two different tunneling voltages (V_{tun}) and a constant input. The high-frequency cutoff eliminates $1/f$ noise at frequencies below 1 / $2\pi\tau_l$. The spectrum was taken for a bias current of 80nA, which corresponds to a V_τ of 0.73V.

gain AFGA is not appreciably different from that of the transconductance amplifier, we conclude that the tunneling and injection processes do not contribute significantly to the noise levels.

Let us investigate how changing the AFGA design will change the amount of output noise. Following [88], we can model the thermal noise component, $\hat{i}_o$, of a subthreshold MOSFET's channel current by

$$\frac{\hat{i}_o^2}{\Delta f} = \frac{2}{\kappa} q U_T g_m. \tag{5.39}$$

Because the AFGA's output comprises both an nFET and a pFET, the total thermal-noise current derives from two parallel noise sources. I want to find the output-referred voltage noise, which I obtain from the simplified small-signal circuit of Fig. 5.13(b). I can further simplify the small-signal circuit of Fig. 5.13(b) to that

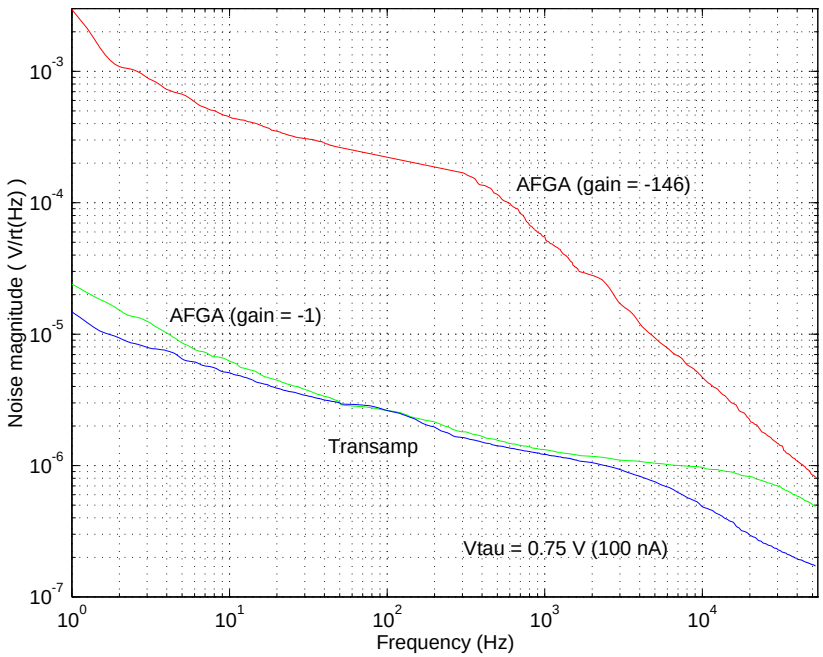


Figure 5.16: Comparison of a high-gain AFGA with a unity-gain AFGA and with a generic follower-connected differential amplifier. All three amplifiers had the same V_τ voltage, and had the same bias current. The sums of C_1 and C_2 are the same for the two AFGAs.

shown in Fig. 5.13(c), by noting that I can relate V_{fg} to V_{out} by a capacitive divider. From this simpler circuit, we can express the signal power of the output-referred voltage noise, $\hat{V}_{out}^2$, as

$$\hat{V}_{out}^2 = \left(\frac{C_1 + C_2 + C_w}{C_2 g_m}\right)^2 \frac{\hat{i}_o^2}{1 + (\omega\tau_h)^2}, \tag{5.40}$$

where τ_h is as defined in Section 5.4. From this expression, we can calculate the total output-noise power as

$$\hat{V}_{out}^2 = \frac{4}{\kappa} q U_T g_m \left(\frac{C_1 + C_2 + C_w}{C_2 g_m}\right)^2 \int_0^\infty \frac{1}{1 + (\omega\tau_h)^2} df, \tag{5.41}$$

which, when we use (5.24), evaluates to

$$\hat{V}_{out}^2 = \frac{qU_T}{\kappa B}\frac{C_1 + C_2 + C_w}{C_2(C_L + C_2)}, \tag{5.42}$$

where the correction term, B, is as defined in (5.28). The total output-noise power is roughly proportional to C_w, and is inversely proportional to C_L.

Now, I would like to calculate the AFGA dynamic range. I shall define dynamic range, DR, as the ratio of the maximum possible linear output swing to the total output-noise power. With this definition, which is equivalent to that given in[89], I express the AFGA dynamic range as

$$DR = \frac{V_{Lo}^2}{2\hat{V}_{out}^2} = \frac{\kappa}{2q}V_{Lo}(C_L + C_2)B^2, \tag{5.43}$$

which is similar to the form for dynamic range for the wide-linear-range amplifier, as derived in [89]. The dynamic range varies inversely with C_2; therefore a high-gain amplifier will have a larger dynamic range than will the low-gain amplifier for the same values of C_1, C_w, and C_L.

5.6 Steady-State Output-Voltage Dependence on the Output Signal

This section discusses the dependence of the steady-state output voltage on the input signal amplitude for input frequencies in the AFGA's passband. Figure 5.17 shows measurements of the minimum and maximum output voltages versus the output amplitude. For small input amplitudes, the minimum and maximum output voltages deviate symmetrically from the steady-state voltage, but for large input amplitudes, most of the change in the output voltage is due to an increasing maximum output voltage. In general, the steady-state output voltage remains within about V_{inj} of the minimum of the signal.

To analyze this effect, I decompose the output voltage into components that

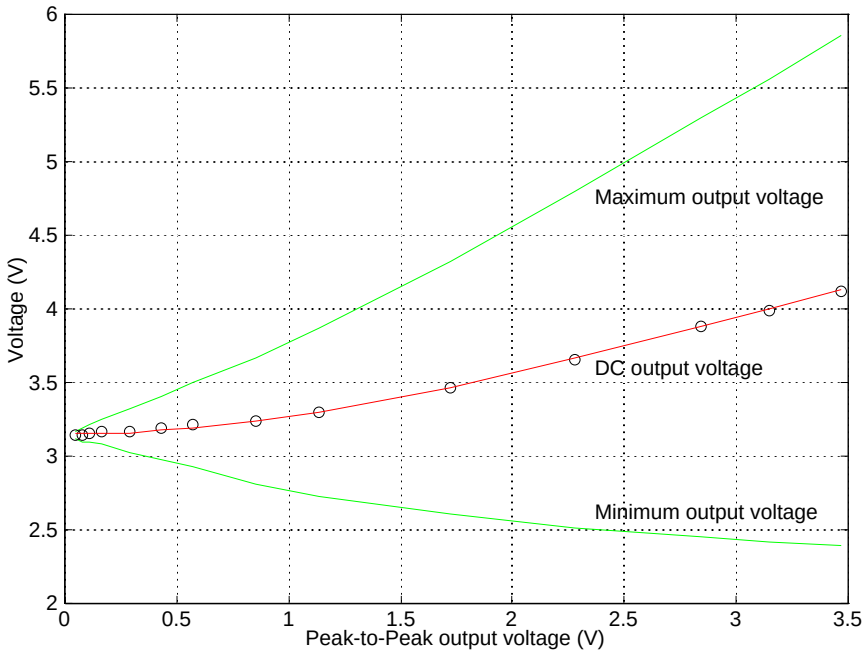


Figure 5.17: Minimum and maximum output voltages versus the peak-to-peak output-voltage amplitude. The frequency of the input sine wave was 100Hz; the AFGA had a gain of 146. For small input amplitudes, the minimum and maximum output voltages symmetrically deviate from the steady-state voltage; for large input amplitudes, however, the DC output voltage follows the maximum output voltage. The DC voltage was fit to the function $0.5\ln(\mathrm{I}_0(V_{dc}\ /\ 1.0\mathrm{V}\ ))$, which is equal to (5.53) with $V_{inj} = 500\mathrm{mV}$.

change at fast and slow rates. As in Chapter 3, I assume that we can express the output voltage as a sum of variables that represent the fast and slow rates; that is,

$$\Delta V_{out} = \Delta \hat{V}_{out} + \Delta \bar{V}_{out}, \tag{5.44}$$

where $\Delta \hat{V}_{out}$ represents the fast-timescale behavior, and is the amplified version of ΔV_{in} ($\Delta \hat{V}_{out} \approx -\frac{C_1}{C_2}\Delta V_{in}$), and $\Delta \bar{V}_{out}$ represents the slow-timescale behavior. With this formulation, we can integrate (5.44) over many periods at the fast timescale, but still make only a small change in the slow-timescale output voltage. I shall define $E[\cdot]$ as the average of a time-varying signal, $x(t)$, over a time interval, T, that is much shorter than the slow timescale, but much longer than one period at the fast

timescale:

$$E[x(t)] = \frac{1}{T}\int_0^T x(t)dt. \tag{5.45}$$

By this definition,

$$E\left[\frac{dV_{in}}{dt}\right] \to 0, E\left[\frac{dV_{out}}{dt}\right] \to \frac{d\bar{V}_{out}}{dt}. \tag{5.46}$$

The resulting equation in $\Delta\bar{V}_{out}$ from (5.11) is

$$C_2\frac{d\bar{V}_{out}}{dt} = I_{tun0}\left(E\left[e^{-\frac{\Delta V_{out}}{V_{inj}}}\right] - 1\right). \tag{5.47}$$

We need to express $E\left[e^{-\frac{\Delta V_{out}}{V_{inj}}}\right]$ in terms of the fast and slow variables:

$$E\left[e^{-\frac{\Delta V_{out}}{V_{inj}}}\right] = e^{-\frac{\Delta \bar{V}_{out}}{V_{inj}}}Q, \tag{5.48}$$

where

$$Q = E\left[e^{-\frac{\Delta \hat{V}_{out}}{V_{inj}}}\right]. \tag{5.49}$$

I rewrite (5.47) as

$$C_2\frac{d\bar{V}_{out}}{dt} = I_{tun0}\left(Qe^{-\frac{\Delta \bar{V}_{out}}{V_{inj}}} - 1\right). \tag{5.50}$$

From the analysis in Section 5.3, the solution to (5.50) is

$$\Delta\bar{V}_{out} = V_{inj}\ln\left(Q + (e^{\frac{\bar{V}_{out}(0^+)}{V_{inj}}} - Q)e^{-\frac{t}{\tau}}\right), \tag{5.51}$$

where the steady-state solution for $\Delta\bar{V}_{out}$ is

$$\Delta\bar{V}_{out} = V_{inj}\ln\left(E\left[e^{-\frac{\Delta \hat{V}_{out}}{V_{inj}}}\right]\right). \tag{5.52}$$

The AFGA always adapts its floating-gate charge such that the minimum of the output signal remains at the equilibrium output voltage.

Now, let us consider the output-voltage behavior as a function of the input-signal amplitude, for a sinusoidal input. I define the amplified input signal as $\Delta\hat{V}_{out} =$

$A\sin(\omega t)$; for this output signal, the steady-state voltage is

$$\Delta\bar{V}_{out} = V_{inj}\ln\left(\int_{\omega t=0}^{2\pi} e^{-\frac{A}{V_{inj}}\sin(\omega t)}d(\omega t)\right) = V_{inj}\ln\left(\mathrm{I}_0\left(\frac{A}{V_{inj}}\right)\right), \tag{5.53}$$

where $\mathrm{I}_0(\cdot)$ is the modified Bessal function of zero$_{th}$ order. Figure 5.17 shows measured minimum and maximum output voltages versus the output signal amplitude for a sine-wave input.

5.7 Other AFGA Effects

5.7.1 Model of the Above-Threshold AFGA

The operation of an autozeroing floating-gate amplifier with above threshold bias currents is similar to the subthreshold behavior in three important respects. First, those effects that depend on electron tunneling remain the same, because tunneling is not a function of the MOSFET channel current. Second, the injection current is still the exponential of the drain voltage. Third, the low-frequency dynamics remain unchanged for a constant C_2, because the channel current is held fixed by feedback.

The pFET hot-electron injection model changes for above-threshold bias currents in two ways. First, the source current is no longer an exponential function of the gate voltage, but rather varies quadratically with the gate voltage. Second, the injection current decreases relative to the source current, because the impact-ionization efficiency will decrease as a result of the potential drop along the channel. I modify the above-threshold injection-current model from (3.17) to be

$$\begin{aligned} I_{inj} &= I_{inj0}\left(\tfrac{V_{dd}-V_{fg}-\Delta V_{fg}+V_T}{V_{dd}-V_{fg}+V_T}\right)^2 e^{-\frac{\Delta V_d-\kappa\Delta V_g}{V_{inj}}} \\ &\approx I_{inj0}\left(1-\tfrac{2\Delta V_{fg}}{V_{dd}-V_{fg}+V_T}\right) e^{-\frac{\Delta V_d-\kappa\Delta V_g}{V_{inj}}} \\ &\approx I_{inj0}\exp\left(-\tfrac{2\Delta V_{fg}}{V_{dd}-V_{fg}+V_T}\right) e^{-\frac{\Delta V_d}{V_{inj}}}. \end{aligned} \tag{5.54}$$

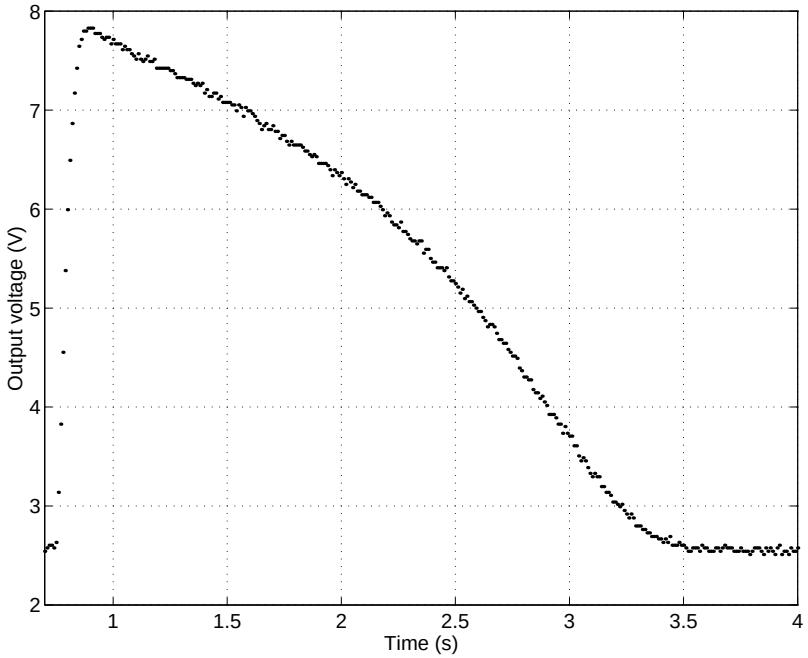


Figure 5.18: The response of an above-threshold AFGA to a downgoing step The feedback cap, C_2, of this AFGA is only the parasitic floating-gate–to–drain overlap capacitance. In the subthreshold case, the voltage linearly decreases with time; therefore, the nonlinear decrease of the output voltage for an above-threshold bias shows that the overlap capacitance changes with drain voltage.

This model changes the DC output voltage to

$$\Delta V_d = -\frac{V_{inj}}{V_x}\Delta V_{tun} + V_{inj}\frac{\kappa_n}{\kappa}\left(\frac{2}{V_{dd} - V_{fg} + V_T} - \frac{1}{V_x}\right)\Delta V_\tau. \tag{5.55}$$

Figure 5.5 shows data consistent with (5.55): the equilibrium output voltage saturates for above-threshold bias currents.

Now consider how the high-frequency behavior changes for above-threshold bias currents. For above-threshold currents, I modify (5.20) to

$$\tau_h \frac{dV_{fg}}{dt} = \tau_h 2\frac{dV_{in}}{dt} - \Delta V_{fg}\left(1 - \frac{\kappa \Delta V_{fg}}{V_{dd} - \kappa(V_{fg0} + V_{T0})}\right). \tag{5.56}$$

The above threshold definitions of τ_h and τ_{h2} are:

$$\tau_{h2} = \frac{C_1(C_2 + C_L)(V_{dd} - \kappa(V_{fg0} + V_{T0}))}{\kappa C_2 I_\tau}, \tag{5.57}$$

and

$$\tau_h = \left((C_1 + C_2 + C_w)(C_2 + C_L) - C_2^2\right) \frac{V_{dd} - \kappa(V_{fg0} + V_{T0})}{\kappa C_2 I_\tau}. \tag{5.58}$$

The higher bias currents result in a higher cutoff frequency, but also requires an increase in power dissipation. The linear input range also is larger, and now is $\frac{C_1+C_2+C_w}{\kappa C_1}(V_{dd} - \kappa(V_{fg0} + V_{T0}))$. The large-signal dynamics change for above-threshold biases. The floating-gate–to–drain overlap capacitance becomes a function of the drain voltage, adding additional dynamics to the large-signal response. Figure 5.18 shows the response of an above-threshold AFGA to a downgoing step.

5.7.2 Continuous Operation of the Tunneling Current

At this point, we might ask what happens when we do not use a continuous tunneling current in the AFGA. The constant tunneling bias current naturally eliminates the effect of DC biasing points; without the gate current, we no longer have an autozeroing amplifier. Without the autozeroing behavior, we need to add circuitry to remove the DC offset. Furthermore, there is additional $1/f$ noise, because the AFGAs high-pass behavior filters the low-frequency $1/f$ noise.

Suppose that we autozero the floating-gate amplifier only to set a particular operating point. Then, after this calibration phase, we lower the tunneling voltage and power supply to turn off the electron-tunneling and hot-electron injection processes to eliminate the gate currents. Unfortunately, the capacitive coupling to the floating gate by the tunneling junction and capacitances not referenced to V_{dd} will make potentially large changes in the output voltage. We can minimize this effect by using small tunneling junctions and by ensuring that all the capacitances (including all parasitics) that couple to the floating gate are referenced to V_{dd}.

In addition to the capacitive coupling, the charge on the floating gate will change

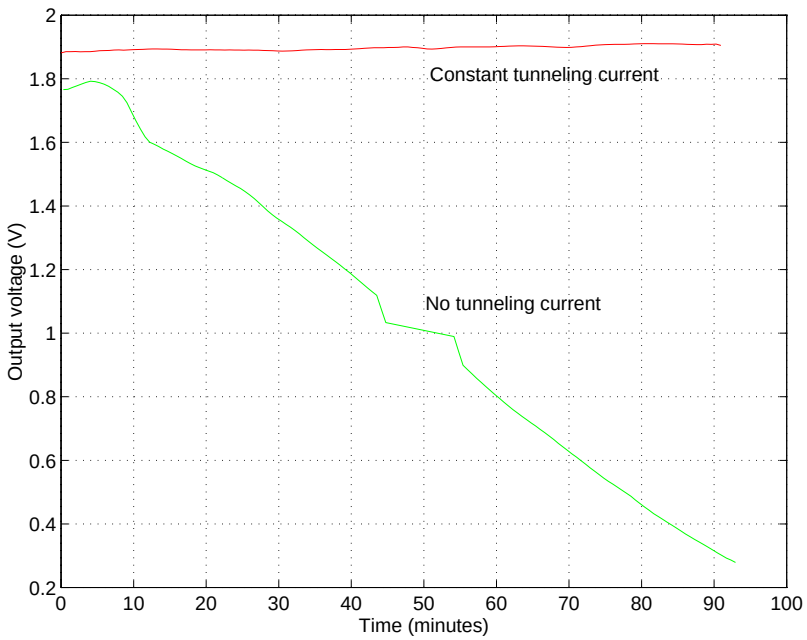


Figure 5.19: Change in the AFGA output voltage with and without a continuous tunneling current. I used the same AFGA with a gain of 146 with both experiments. The experiment for no tunneling current also required that I drop the power supply; V_{dd} was set at 5V. The trace with no tunneling current was started 5 minutes after the tunneling line was dropped.

due to electron traps in the MOS gate oxides. When we tunnel or inject electrons into SiO_2, a portion of these electrons are trapped in the oxide [90]. In addition, as more current passes through these oxides, more electron traps are created [91]. Once the oxide currents stop, some of these trapped electrons will detrap, and can find their way to the floating gate. This effect will result in a large drift in the output voltage over time for the same input bias voltage. In Fig. 5.19, I show the change in the output voltage over time for a high-gain AFGA with and without a constant tunneling current. The detrapping shows no sign of stopping until the output runs into ground; in a lower-gain device, the detrapping may eventually settle with the output voltage within the supply rails.

5.7.3 Restoration to Equilibrium when the Output Voltage Starts at a Supply Rail

Next, we might ask what happens when the output voltage starts at one of the supply rails. The output voltage starts at V_{dd} when the floating-gate voltage is too low. In this regime, there is no injection current; the tunneling current removes electrons from the floating gate, raising the floating-gate voltage. Eventually, the floating-gate voltage increases to its steady-state level, and the output voltage decreases from V_{dd}. If, on the other hand, the output voltage starts near ground, then the pFET has insufficient channel current to develop enough injection to balance the tunneling current. The current must be balanced by changes in the floating-gate voltage: In this case, the floating-gate voltage will increase, since the tunneling current exceeds the pFET injection current. Unfortunately, the pFET channel current then decreases even further, in turn decreasing the injection current, and leading to a runaway condition. The steady-state output voltage may not return to the original equilibrium level. Typically, this condition poses no problem even for reasonably large changes in the input voltage; however, we see this effect at startup or when we make large changes in V_τ. Decreasing V_{tun}, decreasing the input voltage, increasing V_τ, or increasing V_{dd} might allow the AFGA to recover from this condition.

5.8 Conclusions

The AFGA is a simple example of a large class of adaptive floating-gate MOS circuits; these circuits use tunneling and hot-electron injection to adapt the charge on floating gates to return the circuit to a baseline condition on a slow timescale. When the appropriate feedback is applied to the floating gate, this adaptation is an inherent part of the circuit's operation—no additional control circuitry is required. In the case of AFGA, I set up the feedback such that the output voltage returns to its steady-state value on a long timescale. The modulation of the pFET hot-electron injection by the output voltage provides the correct feedback to return the output voltage to

the proper operating regime.

The AFGA has four operating regimes. First, in the adaptation regime, the AFGA behaves as a high-pass filter; the timescale is set by the tunneling and injection currents. Second, in the integrating regime, the AFGA behaves as a low-pass filter; the timescale is set by the nFET bias current. Third, for timescales between the adaptation and integrating regimes, the AFGA acts as an amplifier. Fourth, at frequencies much higher than the integrating regime, the AFGA exhibits capacitive feedthrough, which can be reduced by an increase in either C_w or C_L.

The AFGA always is a first-order system, even in the presence of parasitic capacitances; therefore, the AFGA is unconditionally stable, with 90 degrees of phase margin for noninductive loads. An amplifier that has resistive feedback is at least a second-order system, but an amplifier with capacitive feedback can be a first-order system.

MOS devices and quantum processes, such as electron tunneling and hot-electron injection, are often criticized for their high $1/f$ noise. Since the AFGA's noise performance is similar in thermal and $1/f$ characteristics to that of a standard MOS amplifier, the tunneling and injection processes do not add appreciable noise to the amplifier. In addition, with a desired adaptation rate, I can reduce significantly the low-frequency noise generated in the AFGA; such a reduction cannot be obtained in a standard amplifier that has a blocking capacitor at the input. For moderate tunneling currents, the low-frequency time constant can remain nearly constant for timescales measured in years; any shift is due primarily to trapping in the tunneling oxide. I can increase the linear range by increasing C_w, and I can increase the dynamic range by increasing C_w or C_L.