Chapter 4 Continuous-Time Feedback in Floating-Gate MOS Circuits

Although Chapter 3 presented the electron-tunneling, hot-electron–injection, and multiplicative behavior of the single-transistor synapses, and derived effective learning rules of single-transistor synapses, it did not consider any specific ways that these synapses could be used in a network. This chapter considers the behaviors that emerge when single-transistor synapses are coupled together to form various continuous-time learning networks. My purpose is to understand the dynamics of the learning mechanisms naturally available in floating-gate MOS circuits (FGMOS). Chapter 5 presents the autozeroing floating-gate amplifier (AFGA), which is the first circuit application of a single-transistor synapse with continuous oxide currents.

This chapter describes the various possible negative- and positive-feedback mechanisms in continuous-time FGMOS circuits. The usefulness of negative or positive feedback depends on the application; Hebbian learning [83], for example, is a case of destabilizing positive feedback. Section 4.1 presents a new type of pFET synapse, in which the gate currents provide stabilizing feedback to the floating gate and to the drain. Section 4.2 presents the range of possible stabilizing and destabilizing feedback configurations in circuits comprising one floating-gate synapse; we include data from nFET, pFET, and source-degenerated pFET synapses. Section 4.3 presents the class of stable two-synapse circuits by showing examples of competitive and cooperative behavior between synapses; these properties extend directly to networks of many synapses. I present my conclusions in Section 4.4.

The small-signal models of the single-transistor synapse elements often shed considerable light on the dynamics of simple FGMOS circuits. Figure 4.1 shows small-signal models of the nFET and pFET synapses, where all the small-signal parameters are positively valued. Table 4.1 shows the relationships of the small-signal parame-

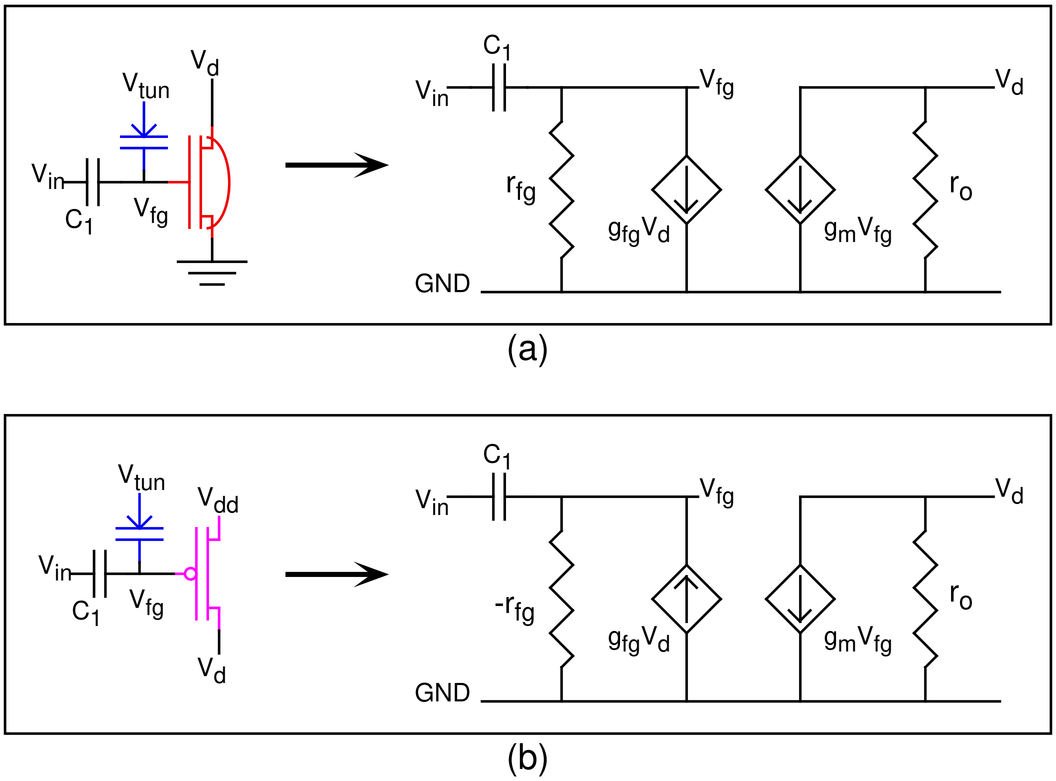

Figure 4.1: (a) Circuit diagram and small-signal model of the nFET single-transistor synapse with its source connected to ground. The small-signal model assumes a constant tunneling current and that the parameters are positive. (b) Circuit diagram and small-signal model of the pFET single-transistor synapse with its source connected to V_{dd}. The small-signal model assumes a constant tunneling current and that the parameters are positive. The small-signal resistance from floating-gate to ground is negative due to the hot-electron injection currents.

ters to the device parameters; I define $x||y$ as $\frac{xy}{x+y}$. I use the conventional definitions [81] of small-signal transconductance, g_m, and output resistance, r_o, to compute the values in Table 4.1 from (3.1). I define this transistor's maximum voltage gain, A_v, as the product $g_m r_o$. I used (3.11) and (3.16) to calculate the values of g_{fg} and r_{fg} in Table 4.1. I define g_{fg} as the change in the gate current in response to a change in drain voltage. Because only the injection current depends on the drain voltage, $g_{fg} = \frac{I_{tun0}}{V_{inj}}$. I define r_{fg} as the magnitude of the change in gate current for a change in gate voltage. The resistance from the floating gate to ground is negative for a pFET. A typical nFET value for the product $g_{fg} r_{fg}$—the gain from V_d to V_{fg}—is 1; a typical

Table 4.1: Relationships of small-signal parameters

Parameter	nFET	pFET	s-d pFET
$g_m = \left\lvert \frac{\partial I_s}{\partial V_{fg}} \right\rvert$	$\frac{\kappa_n I_{so}}{U_T}$	$\frac{\kappa_p I_{so}}{U_T}$	$\frac{\kappa_p \kappa_x I_{so}}{U_T}$
$r_o = \left\lvert \frac{\partial I_s}{\partial V_d} \right\rvert$	$\frac{V_o}{I_{so}}$	$\frac{V_o}{I_{so}}$	$\frac{V_o}{\kappa_x I_{so}}$
$A_v = g_m r_o$	$\frac{\kappa_n V_o}{U_T}$	$\frac{\kappa_p V_o}{U_T}$	$\frac{\kappa_p V_o}{U_T}$
$g_{fg} = \left\lvert \frac{\partial I_{inj}}{\partial V_d} \right\rvert$	$\frac{I_{tun0}}{V_{inj}}$	$\frac{I_{tun0}}{V_{inj}}$	$\frac{I_{tun0}}{V_{inj}}$
$r_{fg} = \left\lvert \frac{\partial (I_{tun}+I_{inj})}{\partial V_{fg}} \right\rvert$	$\frac{U_T/\kappa_p \lVert V_x}{I_{tun0}}$	$\frac{U_T/\kappa_p \lVert -V_x}{I_{tun0}}$	$\frac{U_T/\sigma \lVert V_x}{I_{tun0}}$
$A_{fg} = g_{fg} r_{fg}$	$\frac{U_T/\kappa_p \lVert V_x}{V_{inj}}$	$\frac{U_T/\kappa_p \lVert -V_x}{V_{inj}}$	$\frac{U_T/\sigma \lVert V_x}{V_{inj}}$

pFET value is 0.3.

4.1 The Source-Degenerated pFET Synapse

This section presents the source-degenerated pFET synapse, which I show in Fig. 4.2. I model the κ_x-diode element as

$$I = I_x \exp\left(-\frac{\kappa_x \Delta V}{U_T}\right), \tag{4.1}$$

where ΔV represents the change in V from the bias level, I_x is the quiescent current through the device, and κ_x is a device parameter. By equating the current through the pFET and the κ_x-diode element, and substituting this expression into (3.1), we obtain the source-degenerated pFET model equation for $\kappa_x \gg 1$, which is our region of interest:

$$I_s = I_{so} \exp\left(-\kappa_x \left(\frac{\kappa_p V_{fg}}{U_T} + \frac{V_d}{V_o}\right)\right). \tag{4.2}$$

Figure 4.3 shows the channel current through this synapse as a function of gate voltage for three sizes of κ_x; reducng κ_x decreases the change in channel current for a fixed gate-voltage swing. The κ_x element is effectively cascoded by the pFET; therefore, from (4.2), the maximum voltage gain of this transistor is $\frac{\kappa V_o}{U_T}$, which is identical to that of a non-degenerated subthreshold pFET transistor.

As in (3.3), I can separate the terminal voltages into fast and slow variables. The

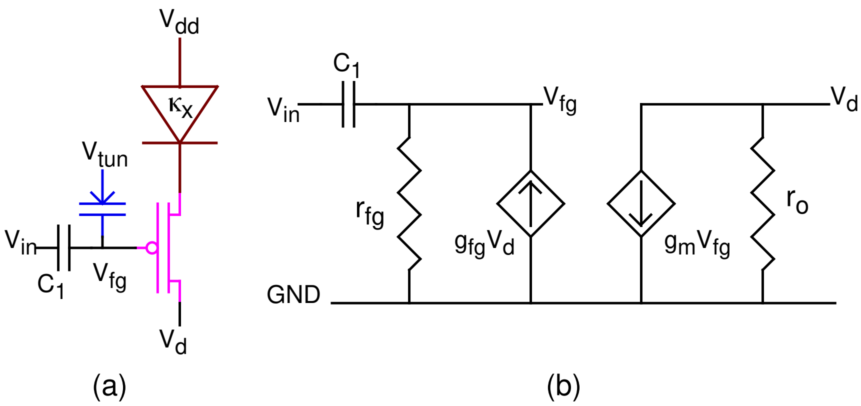

Figure 4.2: The source-degenerated pFET single-transistor synapse. (a) Circuit of the source-degenerated pFET synapse. (b) The small-signal of the source-degenerated pFET synapse, where I have defined all of the small signal quantities to be positive. From this circuit, we can see that this pFET's floating-gate currents provide stabilizing feedback to the floating-gate and drain voltages.

fast-variable definitions are identical to the pFET fast-variable definitions in (3.4) and (3.7), except that κ_p is replaced by $\kappa_p \kappa_x$; the slow-variable model is

$$-\frac{C_T U_T}{\kappa_x \kappa_p W}\frac{dW}{dt} = C_1 \frac{dV_{in}}{dt} + C_2 \frac{d\bar{V}_{out}}{dt} + I_{tun} - I_{inj}, \tag{4.3}$$

where I_{tun} and I_{inj} are the electron-tunneling and hot-electron–injection currents of the pFET.

Figures 4.4, 4.5, and 4.6 show $\frac{d}{dt}\log(I_s)$ versus the source current, I_s, for various tunneling and hot-electron injection currents. Figure 4.2 shows the equivalent small-signal circuit, and Table 4.1 presents the small-signal parameters for this source-degenerated pFET. We can express the change in the tunneling current in terms of the source current, by substituting (4.2) into (3.9):

$$I_{tun} = I_{tun0}\left(\frac{I_s}{I_{so}}\right)^{\frac{U_T}{\kappa_p \kappa_x V_x}}. \tag{4.4}$$

From Fig. 4.5, the tunneling current is nearly a constant power of I_s, and the power increases with decreasing κ_x.

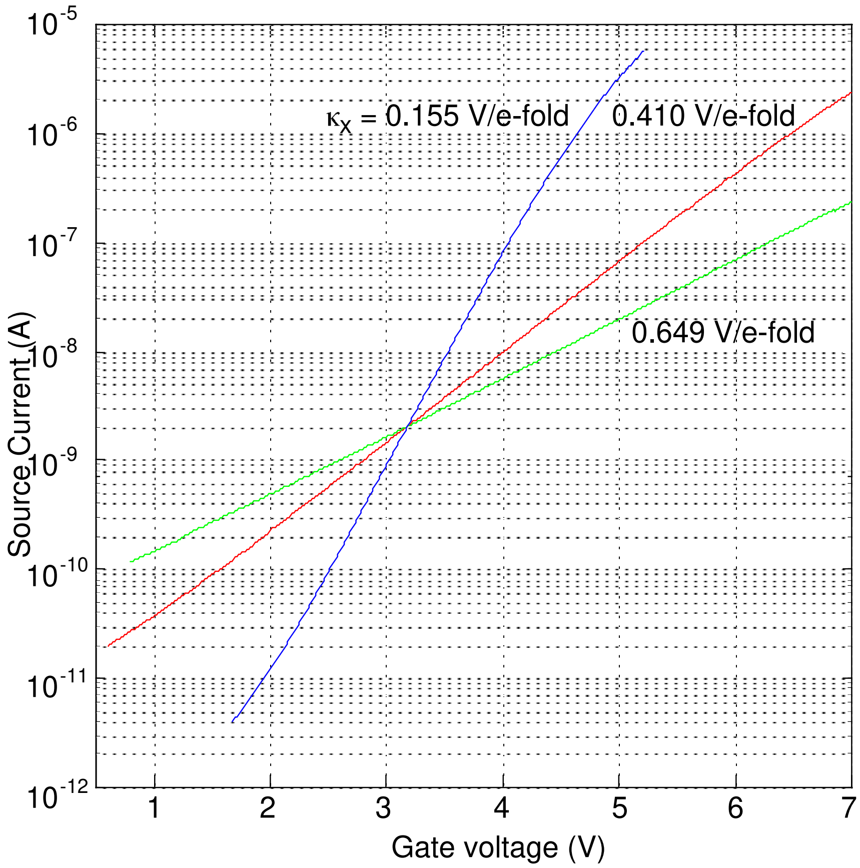

Figure 4.3: Plot of source-degenerated pFET drain current versus gate voltage for three values of κ_x. Decreasing κ_x decreases the transistor's effective gate coupling to the surface potential (due to the decreasing exponential slope).

We can derive the hot-electron injection model for this circuit by substituting the source-degenerated pFET model (4.2) into the pFET hot-electron injection model (3.16):

$$I_{inj} = I_{inj0} \exp\left(\frac{\sigma \Delta V_g}{U_T}\right) \exp\left(-\frac{\Delta V_d}{V_{inj}}\right), \tag{4.5}$$

where $\sigma = \kappa_p \left(\frac{U_T}{V_{inj}} - \kappa_x \alpha\right)$, for small κ_x. The value of κ_x strongly affects the source-current dependence of the injection current. For small κ_x, an increase in the source current requires a large increase in the source voltage, which decreases the drain-to-source voltage, and that, in turn decreases the injection current. With no feedback,

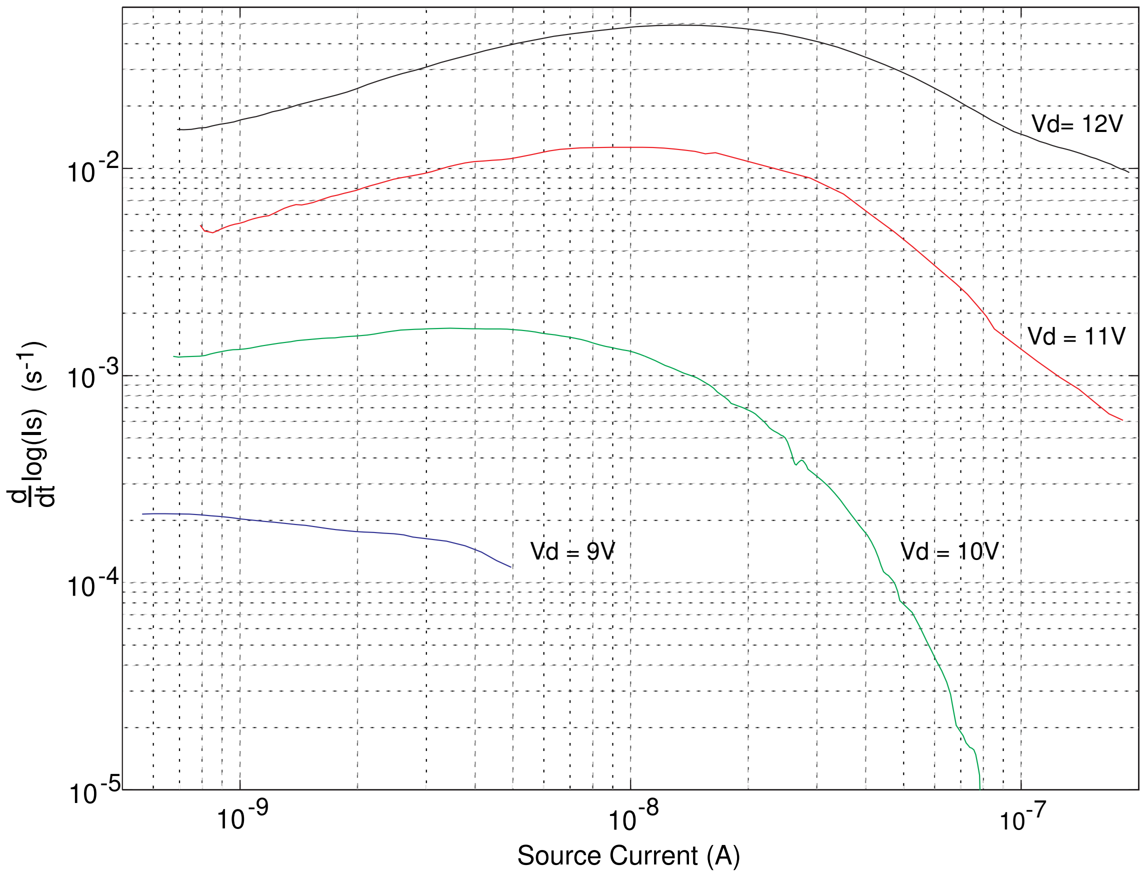

Figure 4.4: Plot of $\frac{d\log(I_s)}{dt}$ versus source current (I_s) for four different values of drain voltage in the source-degenerated pFET. The transistor has stabilizing behavior for some regions of this graph; these portions are reflected in the small signal model. The synapse goes from unstable feedback to stable feedback due to the change in the bias Φ_{dc} of the synapse; larger Φ_{dc} requires a lower κ_x for stabilizing behavior.

σ is negative; the value of κ_x at which σ changes from negative to positive is given by

$$\kappa_x = \frac{U_T}{\alpha V_{inj}}. \tag{4.6}$$

Therefore, if V_{inj} increases, κ_x must decrease by the same amount to preserve stability. By writing the injection current as a function of the source current, we get

$$I_{inj} = I_{inj0}\left(\frac{I_s}{I_{so}}\right)^{-\frac{\sigma}{\kappa_p\kappa_x}} \exp\left(-\frac{\Delta V_d}{V_{inj}}\right). \tag{4.7}$$

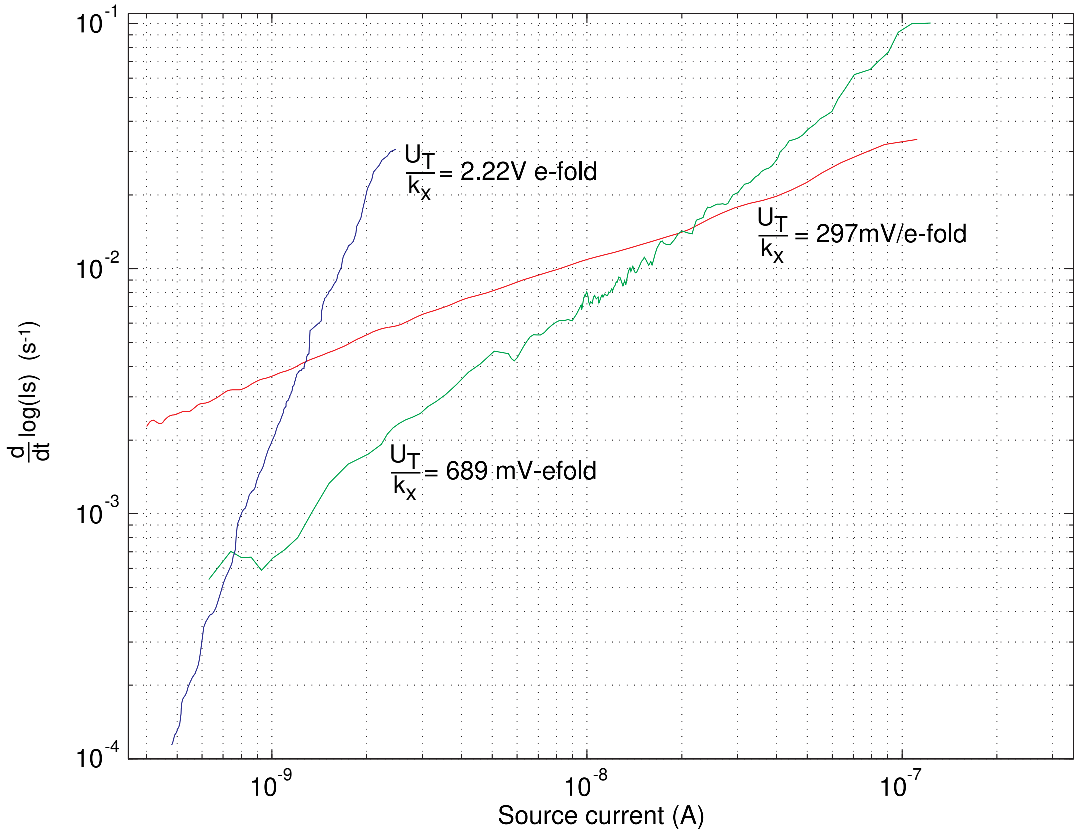

Figure 4.5: The effect of κ_x on tunneling current in the source-degenerated pFET. Plot of $\frac{d}{dt}\log(I_s)$, which is proportional to the tunneling current, as a function of I_s for three different values of κ_x. The curves are nearly straight lines, and the slope of the curves increases for a decreasing κ_x.

Figure 4.4 plots $\frac{d}{dt}\log(I_s)$, as a function of I_s for three values of drain voltage; Figure 4.6 plots $\frac{d}{dt}\log(I_s)$, as a function of I_s for three values of κ_x. The injection current is not a constant power of I_s, because V_{inj} increases when Φ_{dc} increases. An nFET synapse with a κ_x source degeneration would show similar changes in stability.

To obtain the data in Figs. 4.4 and 4.5, I set κ_x by an integrated pnp transistor and an op-amp feedback circuit; this approach gave me the freedom to investigate different values of κ_x. In an integrated synapse, I use a short-channel pFET with significant drain-induced barrier lowering (DIBL) to implement the κ_x diode-element. A transistor that strongly exhibits DIBL shows an exponential change in current for a linear change in drain voltage, as I show in Fig. 4.7. This approach may suffer from significant mismatch, because to make a FET with strong DIBL effect, one

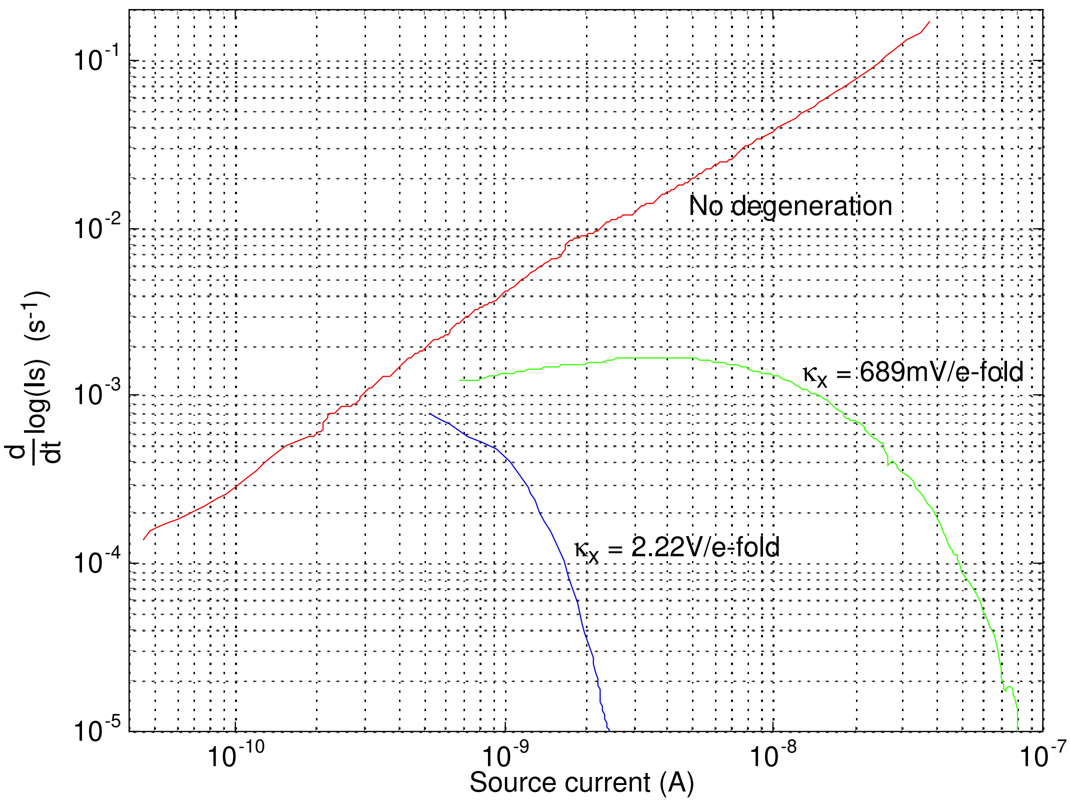

Figure 4.6: The effect of κ_x on hot-electron–injection current in the source-degenerated pFET. Plot of $\frac{d}{dt}\log(I_s)$, which is proportional to the injection current, as a function of I_s for three different values of κ_x, including $\kappa_x = 0$.

must violate the process design rules. An alternative approach is to set κ_x using a floating-gate pFET that has a floating-gate–to–drain capacitance much smaller than the total capacitance of the floating gate; however, this scheme requires a method of initializing the floating-gate charge.

4.2 Stability of Single-Synapse Circuits with Floating-Gate Feedback

This section considers simple one-synapse circuits, to illustrate the basic floating-gate feedback mechanisms. I consider synapse configurations that couple through the drain terminal; similar feedback mechanisms occur with other configurations that employ

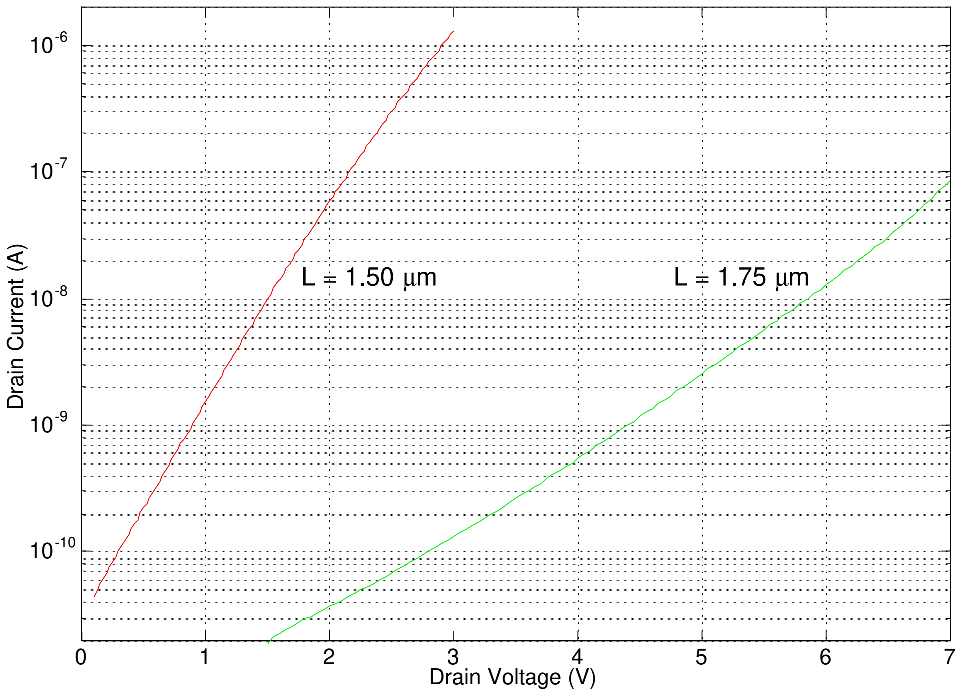

Figure 4.7: Source current versus drain voltage for two short-channel pFETs in a 2μm process with the gate and source voltages at V_{dd}. The drain voltage is measured relative to V_{dd}. The DIBL results in an exponentially increasing current for subthreshold biases; for the 1.5μm pFET, the current increases an e-fold for a 276.1mV change in the drain voltage, and for the 1.75μm pFET, the current increases an e-fold for a 627.3mV change in the drain voltage.

various combinations of the drain, source, and tunneling terminals. I only consider sufficiently long timescales such that the current through the synapse is identical to the current through the coupling FET; that is, I ignore capacitive currents at the drain and source nodes. I also assume that the synapses have nonnegligible tunneling and injection currents.

Figures 4.8 and 4.11 show the pFET and nFET circuits that comprise a single synapse with the the drains connected to current sources. Figures 4.9 and 4.12 show the pFET and nFET circuits that comprise a single synapse with the drains connected to cascode transistors. For all four circuits, equilibrium is established when the tunneling current is balanced by the injection current. Figure 4.10 shows how to simplify the small-signal models for the pFET circuits; one can similarly simplify the nFET and source-degenerated pFET circuits. Using a fixed channel current is equivalent to open-circuiting the drain terminal in the synapse's small-signal model; therefore, the effective conductance from floating gate to ground is

$$n\text{FET} : r_{fg} - (g_m r_o)\, g_{fg},$$

$$p\text{FET} : (g_m r_o)\, g_{fg} - r_{fg}. \tag{4.8}$$

Since this effective conductance is positive for pFET synapses, the configuration in Fig. 4.8 is stable. On the other hand, since this effective conductance is negative for nFET synapses, the configuration in Fig. 4.11 is unstable. When the drain voltage is fixed, the sign of r_{fg} determines the stability of this circuit; the configuration in Fig. 4.9 is unstable due to the negative r_{fg} for pFET synapses, whereas the configuration in Fig. 4.12 is stable due to the positive r_{fg} for nFET synapses. For both the pFET and nFET synapses, a particular load resistance, R_l, connected to the drain, where $R_l g_m (g_{fg} r_{fg}) = 1$, results in zero effective conductance between the floating gate and ground and is the boundary between the stable and unstable regimes. Because this formulation is valid for positive and negative resistances connected to the drain, negative drain resistance is stablizing for nFETs and destabilizing for pFETs. For sufficiently small κ_x, the source-degenerated pFET synapse has a positive conductance from floating gate to ground for all positive resistances connected to the drain terminal, as seen in Table 4.1 and Fig. 4.4. The following three subsections consider the detailed behavior of the pFET, nFET, and source-degenerated pFET circuits.

4.2.1 *p*FET Floating-Gate Circuits

Figure 4.8 shows an autozeroing floating-gate amplifier (AFGA). Chapter 5 explains how the AFGA behaves as a bandpass amplifier; here, I summarize the AFGA's adaptation properties. With capacitive feedback, the input signal is amplified by a closed-loop gain approximately equal to $-\frac{C_1}{C_2}$, where C_2 is the capacitance between the floating gate and drain. The complementary tunneling and hot-electron injection

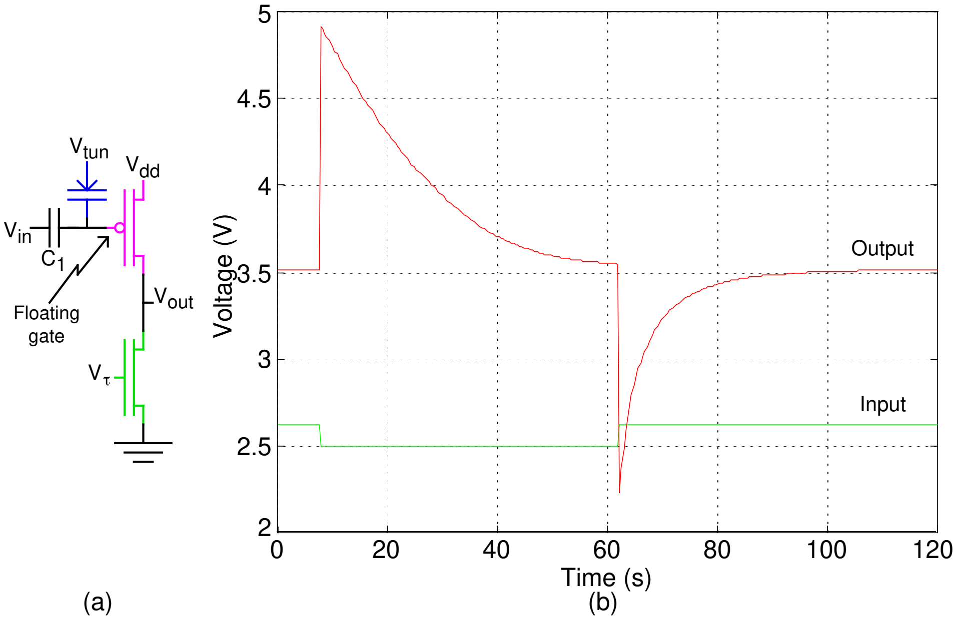

Figure 4.8: (a) The pFET voltage-adapting circuit configuration; this circuit is the autozeroing floating-gate amplifier (AFGA). (b) Response of the AFGA to an upgoing and a downgoing step input. The adaptation in response to an upward step results from electron tunneling; the adaptation in response to a downward step results from pFET hot-electron injection. This amplifier has a gain of 11.2, and I_{tun0} is 50fA.

processes adjust the floating-gate charge such that the amplifier's output voltage returns to a steady-state value on a slow time scale. If the output voltage is below its equilibrium value, then the injection current exceeds the tunneling current, decreasing the charge on the floating gate, and, in turn, raising the output voltage back toward its equilibrium value. If the output voltage is above its equilibrium value, then the tunneling current exceeds the injection current, increasing the charge on the floating gate, and, in turn, lowering the output voltage back toward its equilibrium value.

Because the amplifier has a large open-loop gain, if we are to keep the output voltage between the supply rails, the floating-gate voltage must be confined to a swing of only a few millivolts. A nearly constant floating-gate voltage implies a constant tunneling current ($I_{tun} = I_{tun0}$), and implies that the source current ($I_s = I_{so}$) is

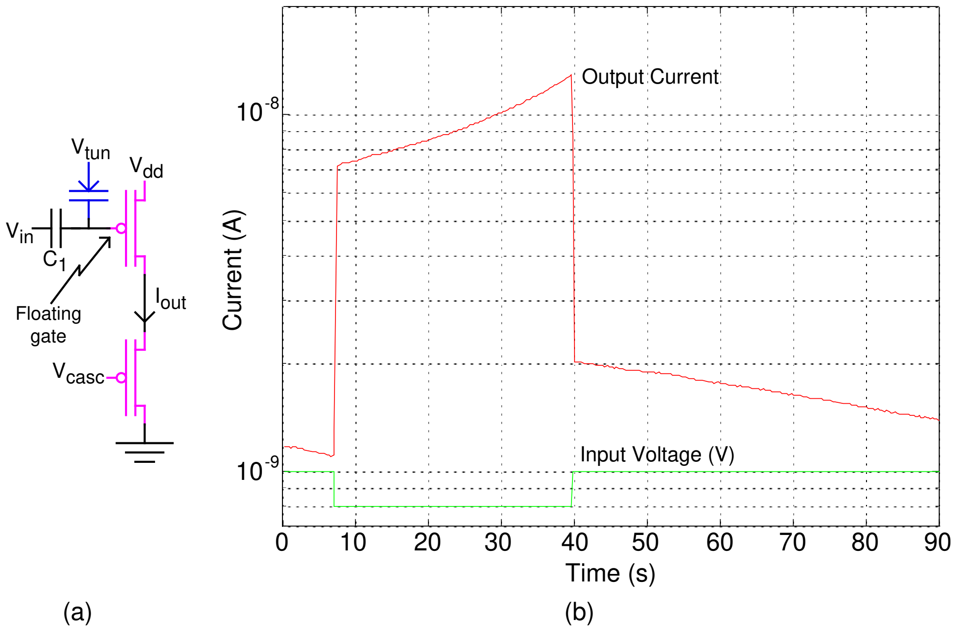

Figure 4.9: (a) The pFET current-adapting circuit configuration. (b) Response of the current-adapting pFET synapse to an upgoing and a downgoing step input. This circuit configuration is unstable.

equal to the nFET source current. Therefore, $W = 1$, and (3.7) simplifies to

$$C_2 \frac{dV_{out}}{dt} = -C_1 \frac{dV_{in}}{dt} + I_{tun0} \left(\exp\left(-\frac{\Delta V_{out}}{V_{inj}} \right) - 1 \right). \tag{4.9}$$

As I show in Chapter 5, (4.9) is a linear, first-order differential equation in X, where I define $X = \exp\left(\frac{\Delta V_{out}}{V_{inj}}\right)$. The trajectories of (4.9) converge to the steady state at $\Delta V_{out} = 0$. Figure 4.8 shows the circuit response to an upgoing and a downgoing input step; between the step changes in V_{in}, the output voltage converges back toward equilibrium, as expected from stabilizing feedback.

Figure 4.9 shows the pFET synapse circuit with its drain connected to a cascode transistor; the cascode configuration nearly fixes the drain voltage. If the output current is above its equilibrium value ($W = 1$), then the injection current exceeds the tunneling current, decreasing the floating-gate voltage, and further increasing the output current. If the output current is below its equilibrium value, then the

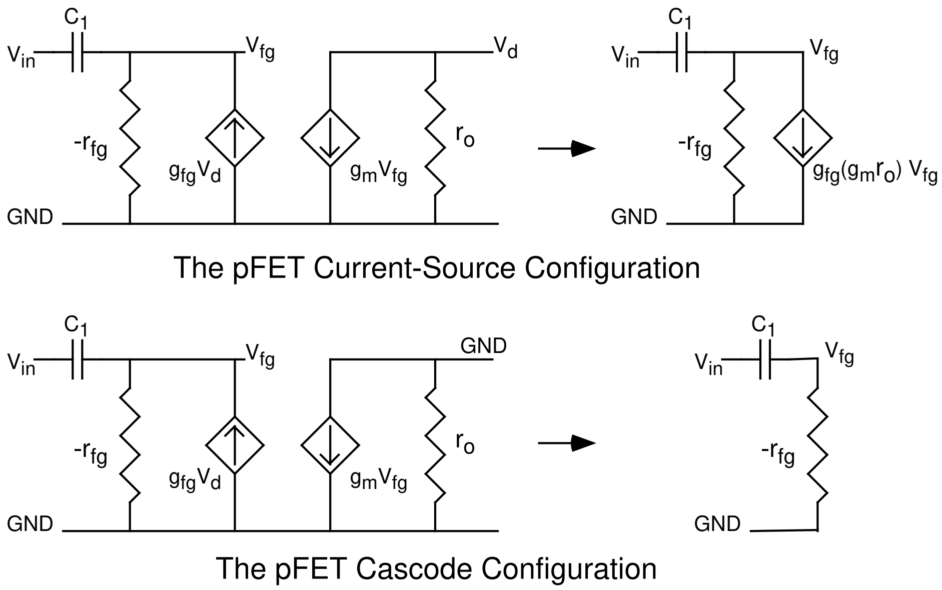

Figure 4.10: Simplification of small-signal models for the pFET single-transistor circuits; the nFET and source-degenerated pFET synapse circuits are simplified similarly. The top figure shows the simplified small-signal model for the drain connected to a cascode transistor. The bottom figure shows the simplified small-signal model for the drain connected to a current source. This circuit is unstable because of the negative resistance from floating-gate to ground.

tunneling current exceeds the injection current, increasing the floating-gate voltage, and further decreasing the output current. Because drain voltage is fixed, we can simplify (3.7) to

$$\frac{C_T U_T}{\kappa_p I_{tun0}} \frac{dW}{dt} = W \frac{C_1}{I_{tun0}} \frac{dV_{in}}{dt} - W^{1-\frac{U_T}{\kappa_p V_x}} + W^{1+\alpha}. \tag{4.10}$$

The trajectories of this differential equation converge toward $W = 0$ and diverge away from $W = 1$; this behavior is consistent with destabilizing positive feedback. Figure 4.9 shows the circuit response to input steps near the steady-state current; between the step changes in V_{in}, the output current diverges away from the equilibrium current.

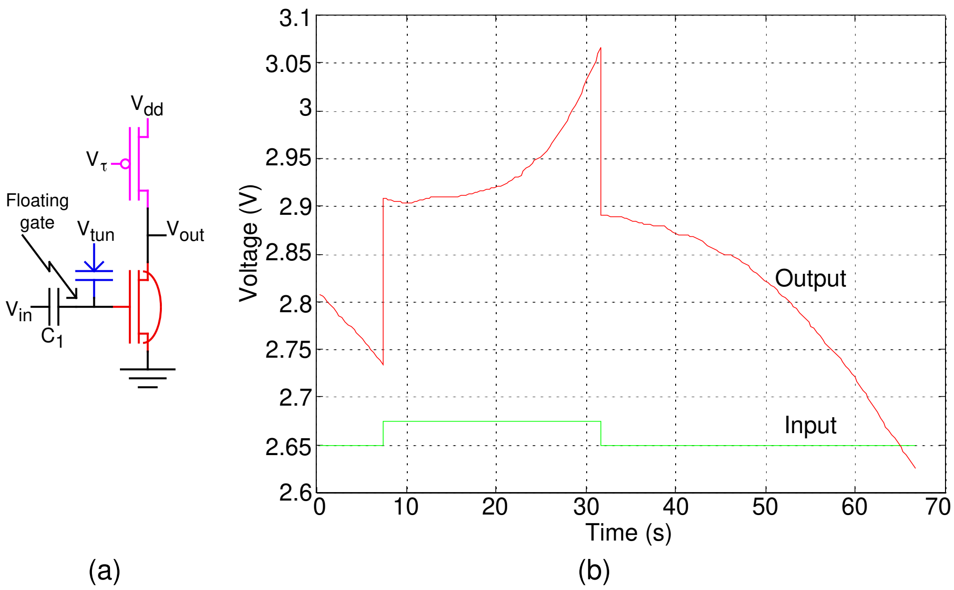

Figure 4.11: (a) The nFET voltage-adapting circuit configuration. (b) Response of the voltage-adapting nFET synapse to an upgoing and a downgoing step input. This circuit configuration is unstable.

4.2.2 nFET Floating-Gate Circuits

Figure 4.11 shows the nFET synapse with its drain connected to a current source. As with the AFGA, the source and tunneling currents are nearly constant, and W is fixed at 1. If the output voltage is above its equilibrium value ($\Delta V_{out} = 0$), then the injection current exceeds the tunneling current, decreasing the charge on the floating-gate, and further increasing the output voltage. If the output voltage is below its equilibrium value, then the tunneling current exceeds the injection current, increasing the charge on the floating-gate, and further decreasing the output voltage. The governing equation is

$$C_2 \frac{dV_{out}}{dt} = -C_1 \frac{dV_{in}}{dt} + I_{tun0} \left(\exp\left(\frac{\Delta V_{out}}{V_{inj}} \right) - 1 \right), \tag{4.11}$$

where the trajectories of this differential equation diverge away from the steady state at $\Delta V_{out} = 0$; this behavior is consistent with destabilizing positive feedback. Figure

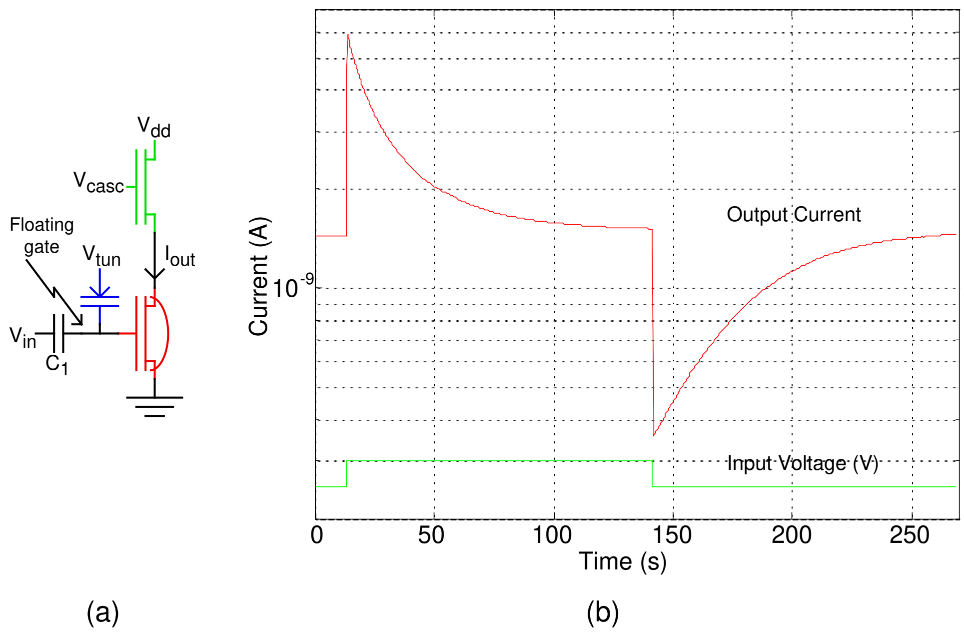

Figure 4.12: (a) The nFET current-adapting circuit configuration. (b) Response of the current-adapting nFET synapse to an upgoing and a downgoing step input. This circuit configuration is stable.

4.11 shows the circuit response to input steps near the steady-state voltage; between the step changes in V_{in}, the output voltage moves away from the equilibrium voltage.

Figure 4.12 shows the nFET synapse circuit configuration with a fixed drain voltage. If the output current is above its equilibrium value ($W = 1$), then the injection current exceeds the tunneling current, decreasing the floating-gate voltage, and in turn decreasing the output current. If the output current is below its equilibrium value, then the tunneling current exceeds the injection current, increasing the floating-gate voltage, and in turn increasing the output current. Because the drain voltage of the nFET synapse is fixed, I obtain from (3.7) that

$$\frac{C_T U_T}{\kappa_n I_{tun0}} \frac{dW}{dt} = W \frac{C_1}{I_{tun0}} \frac{dV_{in}}{dt} + W^{1-\frac{U_T}{\kappa_n V_x}} - W^{1+\alpha}; \tag{4.12}$$

the trajectories of this equation converge toward $W = 1$ and diverge away from $W = 0$; this behavior is consistent with stabilizing negative feedback. Figure 4.12 shows the circuit response to input steps near the steady-state voltage; between the

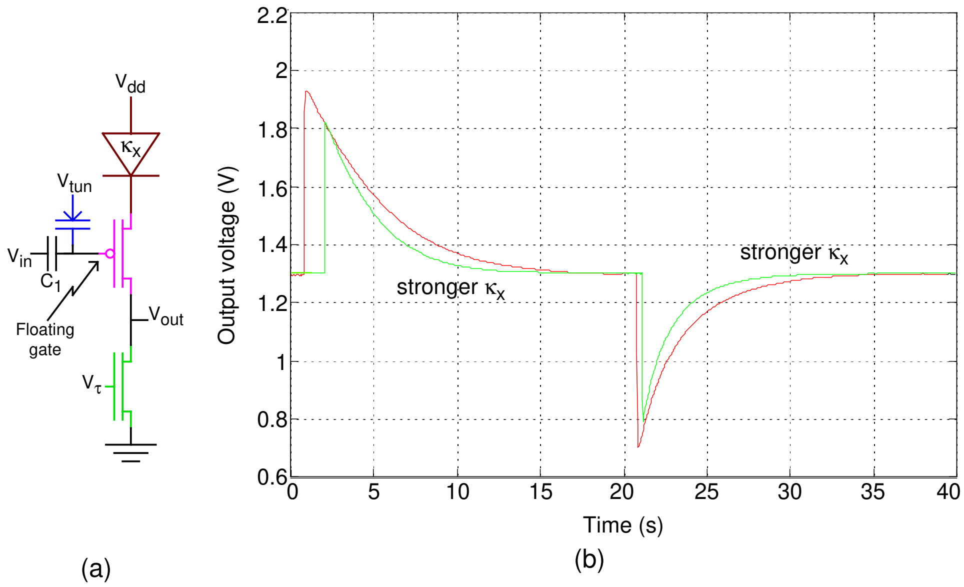

Figure 4.13: The behavior of the voltage autozeroing circuit using a source-degenerated pFET synapse. Unlike the nFET synapse, this circuit converges to its steady-state voltage. (a) Circuit diagram. (b) Response of this circuit to an upgoing and a downgoing step input for two different values of κ_x. The circuit behavior does not change for different channel currents if the bias drain–to–source voltage is fixed.

step changes in V_{in}, the output current converges toward the equilibrium current. This circuit is an autozeroing transconductance amplifier, because the output current always returns to the same equilibrium level.

4.2.3 Source-Degenerated pFET Floating-Gate Circuits

Figure 4.13 shows the source-degenerated pFET synapse with its drain connected to a current source. As in the AFGA case, the source and tunneling currents are nearly constant, and W is fixed at 1. Because the circuit returns to equilibrium by changing its drain voltage, the qualitative behavior is identical to that of the AFGA. The governing equation is

$$C_2 \frac{dV_{out}}{dt} = -C_1 \frac{dV_{in}}{dt} + I_{tun0} \left(\exp\left(\frac{\Delta V_{out}}{V_{inj}} \right) - 1 \right), \tag{4.13}$$

where the trajectories of this differential equation converge toward the steady state at

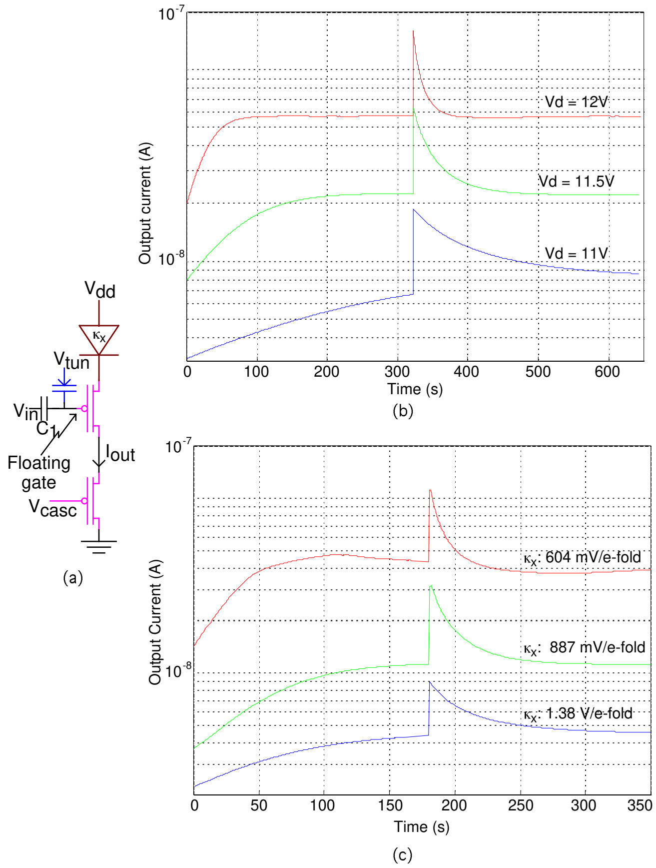

Figure 4.14: The behavior of the current autozeroing circuit using a source-degenerated pFET synapse. Unlike the pFET synapse, this circuit converges to its steady-state current. (a) Circuit diagram. (b) Response of this circuit to an upgoing and a downgoing step input for three values of drain voltage. (c) Response of this circuit to an upgoing and a downgoing step input for three different values of κ_x.

$\Delta V_{out} = 0$; this behavior is consistent with stabilizing negative feedback. The source voltage is almost constant for this low-frequency regime, because the source current is almost constant. Figures 4.13(b) shows the circuit response to input steps near the steady-state voltage; between the step changes in V_{in}, the output current converges toward its equilibrium voltage.

Figure 4.14 shows the source-degenerated pFET synapse with its drain connected to a cascode transistor; this configuration is also stable. For the current autozeroing configuration to be stable, the hot-electron injection current must decrease for an increasing change in the source-current; the stable behavior in both source-degenerated circuits illustrates the changes in the source-current dependence on the hot-electron injection current from a pFET synapse. If the output current exceeds its equilibrium value ($W = 1$), then the injection current exceeds the tunneling current, causing both the floating-gate voltage and source voltage to decrease. For a sufficiently small κ_x, the change in the pFET's drain-to-source voltage decreases the injection current more than the amount by which the increasing source current increases the injection current. Decreasing the injection current increases the output current, and that, in turn, returns the output current back to equilibrium. If the output current is below its equilibrium value, then the tunneling current exceeds the injection current, increasing both the floating-gate voltage and the pFET's source voltage. For a sufficiently small κ_x, the change in drain-to-source voltage will increase the injection current more than the amount by which the decreasing source current decreases the injection current. Increasing the injection current decreases the output current, and that, in turn, returns the output current back to equilibrium. Because the drain voltage of the synapse is fixed as in Fig. 4.9, I obtain from (3.7) that

$$\frac{C_T U_T}{\kappa_n I_{tun0}} \frac{dW}{dt} = W \frac{C_1}{I_{tun0}} \frac{dV_{in}}{dt} + W^{1+\frac{U_T}{\kappa_x \kappa_p V_x}} - W^{1+\frac{\sigma}{\kappa_p \kappa_x}}; \tag{4.14}$$

the trajectories of this equation converge toward $W = 1$ and diverge away from $W = 0$, and are consistent with negative feedback. Figure 4.14 shows the circuit response to an input step near the steady-state voltage for various κ_x and drain voltages; between the step changes in V_{in}, the output current converges toward its equilibrium current. For the pFET and nFET synapses, only one of the two circuits is stable, but both source-degenerated pFET synapse configurations are stable. The positive r_{fg} stabilizes the cascoded-drain circuit, and the open-drain conductance, $r_{fg} + (g_m r_o) g_{fg}$, stabilizes the circuit when the drain is connected to a current source.

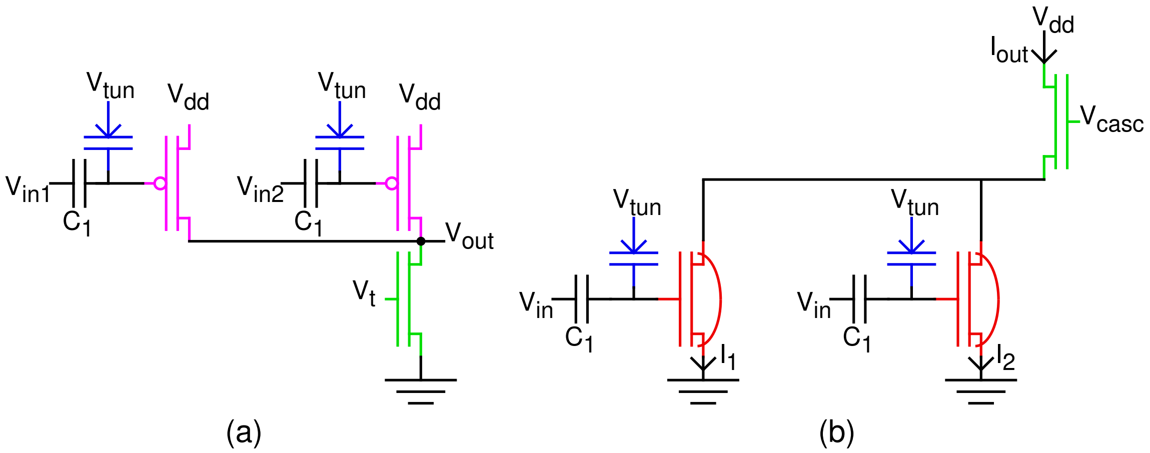

Figure 4.15: (a) Circuit with two pFET synapses coupled at the drain with a current source. (b) Circuit with two nFET synapses coupled at the drain with a cascode transistor.

Table 4.2: Values of A and B for the three synapses

Synapse	A	B
pFET	$W_1^{1+\alpha} + W_2^{1+\alpha}$	$W_1^{1+\frac{U_T}{\kappa_p V_x}} + W_2^{1+\frac{U_T}{\kappa_p V_x}}$
nFET	$W_1^{1+\alpha} + W_2^{1+\alpha}$	$W_1^{1-\frac{U_T}{\kappa_n V_x}} + W_2^{1-\frac{U_T}{\kappa_n V_x}}$
s-d pFET	$W_1^{1-\sigma} + W_2^{1-\sigma}$	$W_1^{1+\frac{U_T}{\kappa_x \kappa_p V_x}} + W_2^{1+\frac{U_T}{\kappa_x \kappa_p V_x}}$

4.3 Networks of Two Coupled Synapses

Where the previous section explored the possible behaviors of circuits comprising a single synapse transistor, this section considers the interaction between synapses coupled though their drain terminals. These networks show both competitive and cooperative behavior between synapses. I only use the stable circuit configurations from the previous section, since it is difficult to illustrate the behavior of circuits that have no stable operating point. I consider, in turn, the stable two-synapse circuits for the pFET, the nFET, and the source-degenerated pFET synapses. This section considers the circuit responses for a constant input voltage, because I want to analyze the relaxation of the synaptic currents.

Figures 4.15 and 4.16 show the multiple-synapse circuits that we are considering.

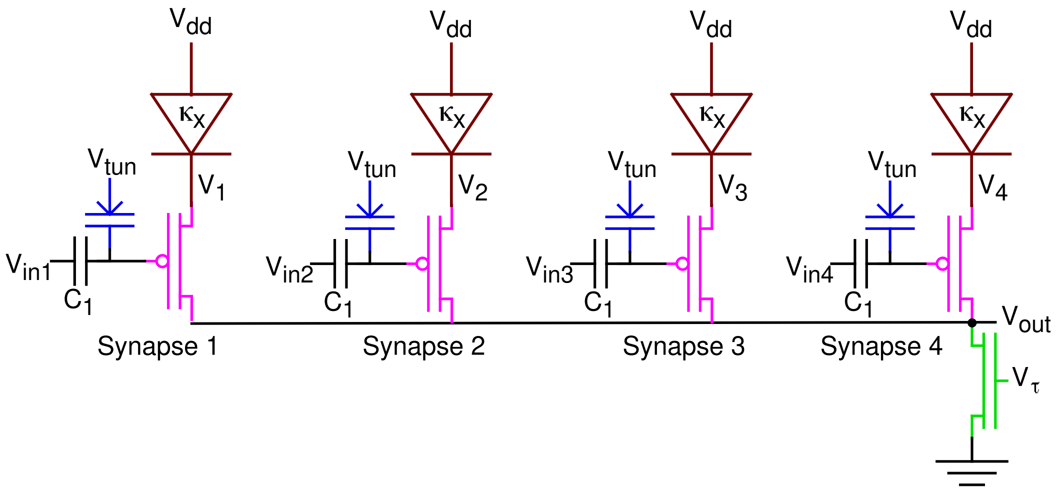

Figure 4.16: Circuit diagram of the four-input source-degenerated pFET synapse.

First, I want to show that the output voltages (V_{out}) and synapse currents ($I_{so}W$) return to their equilibrium values; the single- and multiple-synapse cases are similar in that V_{out} values return to their original steady states. The pFET synapse channel currents are constrained by a current source, which I define to be the sum of the bias currents in each synapse ($2I_{so}$); therefore, the sum of the two weights (W_1, W_2) is equal to 2. For a positive step into the gate of either synapse, V_{out} decreases, causing both transistors to inject more electrons onto their floating gates; consequently, the transistors source more current, and V_{out} increases. From the slow-variable definitions in (3.7), I model the output voltage for the traditional pFET synapse and the source-degenerated pFET synapse as

$$\frac{C_2}{I_{tun0}}\frac{dV_{out}}{dt} = Ae^{-\frac{\Delta V_{out}}{V_{inj}}} - B, \tag{4.15}$$

where A and B are functions of W_1, W_2, as defined in Table 4.3. A and B are always positive and vary slowly; as a result both equations are qualitatively identical to the output-voltage equation of the AFGA. The ΔV_{out} trajectories converge to the circuit's steady state. The nFET synapses are constrained by the cascode transistor; therefore, $\Delta V_{out} = -U_T \ln((W_1 + W_2)/2)$ for $C_2 = 0$. We differentiate this expression

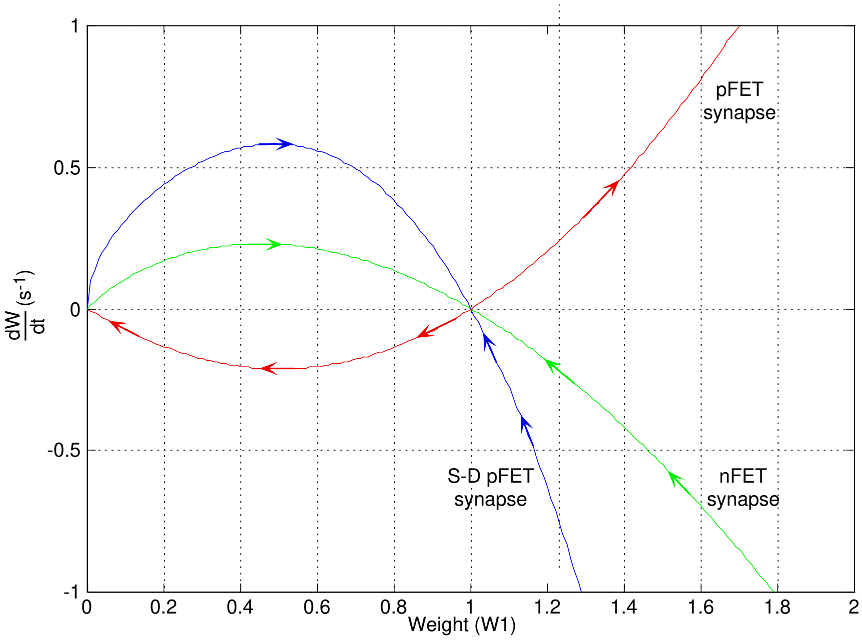

Figure 4.17: Plot of the time-derivative of W versus W for the nFET, pFET, and source-degenerated pFET synapses. The arrows show the directions that the differential equations will take. This figure shows that the nFET and source-degenerated synapses will stabilize to the $W = 1$ steady state, while the pFET synapse will diverge from the $W = 1$ steady state.

and substitute the slow-variable definitions in (3.7) to get the output voltage for the nFET synapse:

$$\frac{C_T + \kappa_n C_2}{\kappa_n I_{tun0}} \frac{dV_{out}}{dt} = B - Ae^{\frac{\Delta V_{out}}{V_{inj}}}. \tag{4.16}$$

Again A and B are positive, so the ΔV_{out} trajectories of (4.16) converge to the circuit's steady state, as in the pFET cases in (4.9) and (4.13).

Once the output voltage has reached equilibrium, the synapses act like coupled current autozeroing circuits; the behavior of the cascoded drain circuit for a particular synapse flavor determines the stability between synapses of that flavor. A constant output voltage requires that the sum of the synapses' weights be a constant. Because ΔV_{out} converges to 0 as $t \to \infty$, the stability of the weights is determined by the circuit behavior at $\Delta V_{out} = 0$. In practice, ΔV_{out} usually reaches its equilibrium before the weights reach their equilibria, and the weight adaptation does not affect

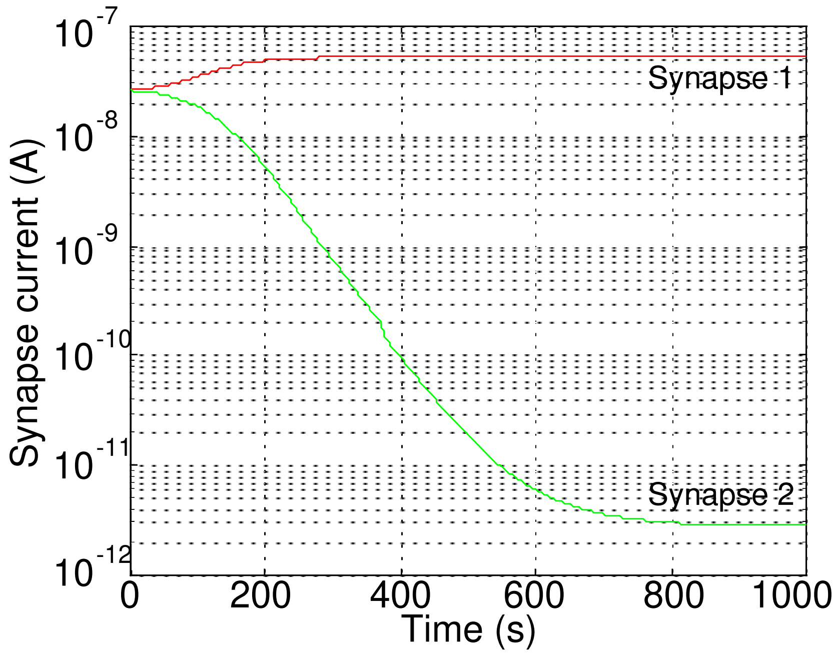

Figure 4.18: The behavior of coupled pFET synapses for fixed inputs. Even though the synapse currents initially start near each other, I_1 wins and I_2 loses. I_2 decreases as a linear exponential in time due to the constant tunneling current at the floating gate. The measured I_2 saturates due to the surrounding leakage currents; the floating gate continues to increase with time.

V_{out} once it has reached equilibrium. When ΔV_{out} has not converged to equilibrium, the behavior of the weights is similar qualitatively to the case when ΔV_{out} has reached equilibrium. In the following paragraphs, I discuss the stability of all three circuits; Fig. 4.17 illustrates qualitatively the stability of all three circuits by plotting $\frac{dW}{dt}$ versus W. I assume, without loss of generality, that $W_1 < W_2$, because the circuit behavior is symmetric in W_1 and W_2.

First, I consider the long-time behavior of the classic pFET synapse once $\Delta V_{out} = 0$. Figure 4.18 shows measured data of two synapse currents once $\Delta V_{out} = 0$. When W_2 is greater than W_1, the first synapse injects less than the second, further increasing the ratio of W_2 to W_1. Since the sum of the channel current is fixed, the first synapse takes more of the bias current and the current of the second synapse decreases; therefore, the second synapse's current steadily drops to zero. This behavior

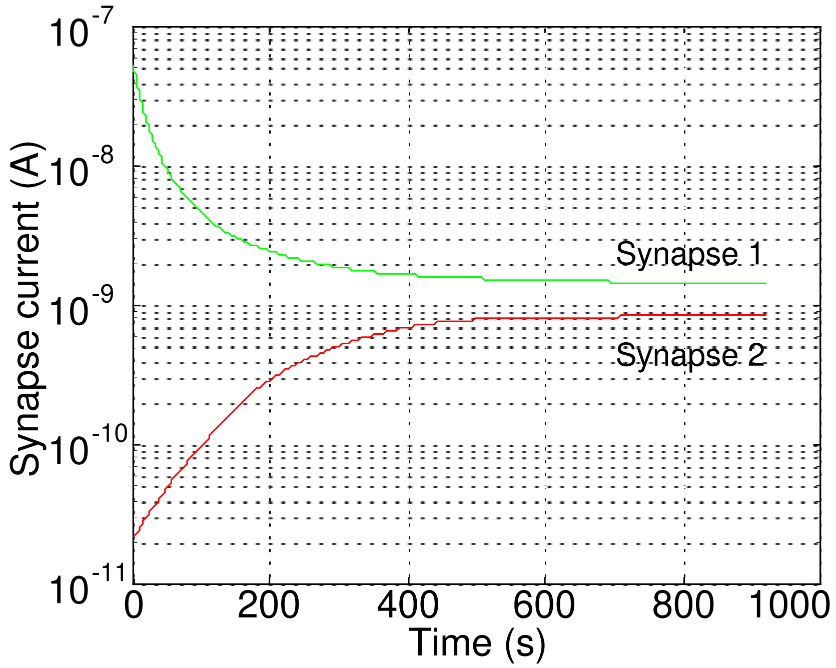

Figure 4.19: The behavior of coupled nFET synapses for fixed inputs. Even though the synapse currents initially start orders of magnitude apart from each other, both currents eventually converge to nearly the same steady-state level.

can be modeled for zero inputs as

$$\frac{C_T U_T}{\kappa_p I_{tun0}} \frac{dW_1}{dt} = W_1^{1+\frac{U_T}{\kappa_p V_x}} \left(W_1^{\alpha - \frac{U_T}{\kappa_p V_x}} - 1 \right). \tag{4.17}$$

Since I assumed that $W_2 > W_1$, the W_1 trajectories of this equation diverge from 1 and converge to 0. Figure 4.18 shows that, if the two starting weights are equal, over time one weight will decrease to 0 and the current in the other synapse will be equal to the bias current. If the losing weight is brought slightly above the winning weight, what was the losing synapse will now be the winner. The pFET synapses compete with each other for the bias current; in some sense, this circuit displays winner-take-all behavior in the weight space. This behavior is typical of a continuous-time normalizing Hebbian network; after a period of time, we cannot reuse these synapses without significantly altering this circuit.

Next, I consider the long-time behavior of the nFET synapses once $\Delta V_{out} = 0$.

The two nFET synapses are coupled with a cascode connection to the common drain terminal, which pins the drain voltage. A nearly fixed drain voltage means that the synapses are only weakly coupled through the drain; I could achieve stronger coupling with a negative-resistance circuit. If W_1 is smaller than W_2, the first synapse injects less than the second, differentially increasing the floating-gate voltages, and resulting in a larger W_1 and smaller W_2. I model the nFET synapse behavior as

$$\frac{C_T U_T}{\kappa_n I_{tun0}} \frac{dW_1}{dt} = W_1^{1-\frac{U_T}{\kappa_n V_x}} \left(1 - W_1^{1+\frac{U_T}{\kappa_n (V_x || -V_{inj})}}\right). \tag{4.18}$$

The W_1 trajectories of this equation diverge from 0 and converge to 1. Because the sum of the channel current is fixed, the first synapse takes a larger fraction of the total current. The weights of the two synapses converge to the steady state $W_1 = W_2$. Figure 4.19 shows that, if the two starting weights are different, then, over time, the two weights will converge to the same value.

Third, I consider the long-time behavior of the source-degenerated pFET synapse once $\Delta V_{out} = 0$. I model the source-degenerated pFET synapse for constant inputs as

$$\frac{C_T U_T}{\kappa_p \kappa_x I_{tun0}} \frac{dW_1}{dt} = W_1^{1-\frac{\sigma}{\kappa_p \kappa_x}} \left(1 - W_1^{\frac{U_T}{\kappa_x \kappa_p V_x} + \frac{\sigma}{\kappa_p \kappa_x}}\right). \tag{4.19}$$

Since I assumed that $W_2 > W_1$, the W_1 trajectories of this equation diverge from 0 and converge to 1. This circuit shows stablizing feedback between the two synapses, because the current autozeroing configuration for a single synapse was stable. Also, the threshold for stability is the point at which the exponent of the second term in W_1 is equal to 0; this condition can be expressed as

$$\kappa_x = \frac{U_T}{\kappa_p V_x || V_{inj}}, \tag{4.20}$$

for small κ_x. Figure 4.20 shows the stable response of a four-input source-degenerated pFET synapse network. Since all synapses of the four-synapse circuit converge to equilibrium, we can see one example that these synapse properties extend to multiple synapses.

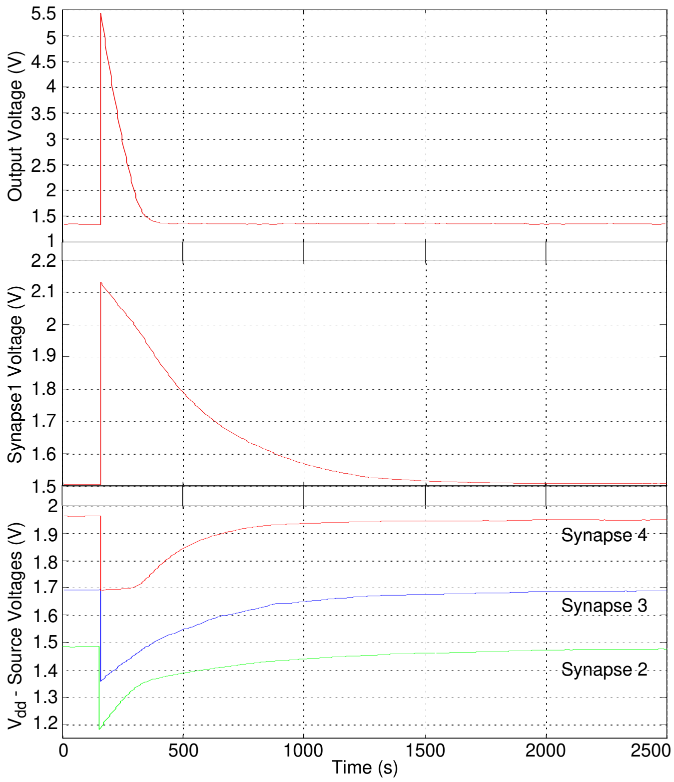

Figure 4.20: Output voltage and synapse voltage (V_1, V_2, V_3, V_4) responses due to an input step applied to the first synapse. This figure shows that the stabilizing behavior for two synapses is extendible to multiple synapses.

4.4 Conclusions

I have characterized and modeled the dynamics of nFET and pFET single-transistor synapses operating in continuous-time circuits. The dynamic behavior of a single synapse can be characterized from that synapse's response in both a constant-current configuration and a constant-voltage configuration. For a pFET synapse, the constant-current configuration is stable, because the floating-gate feedback from its drain is stable. For an nFET synapse, the constant-voltage configuration is stable, because the floating-gate feedback from its floating gate is stable. The pFET synapse's constant-voltage configuration and the nFET-synapse's constant-current configuration are unstable circuits. I presented a new type of pFET synapse where degenerating the source results in gate currents providing stabilizing feedback in both configurations.

I characterized and modeled the dynamics of two coupled single-transistor synapses, where the sum of the weights converges to a steady state. The two pFET synapses compete for the available bias current; the synapse starting with the larger channel current will eventually supply all the bias current. The two nFET synapses cooperate for the entire available channel current; regardless of the starting position, the two synapses converge to nearly equal channel currents. Since the gate currents of the source-degenerated pFET synapse provide stabilizing feedback to the floating-gate and drain, the weights of coupled source-degenerated pFET synapses converge to nearly equal channel currents, as they do in the nFET synapses. These properties extend directly to multiple synapses.