Analog Integrated Circuits and Signal Processing, 9, 167?? (1996)

Translinear Circuits Using Subthreshold Floating-Gate MOS Transistors

BRADLEY A. MINCH, CHRIS DIORIO, PAUL HASLER, AND CARVER A. MEAD
bminch@pcmp.caltech.edu
Physics of Computation Laboratory, California Institute of Technology, Pasadena, CA, 91125

Abstract. We describe a family of current-mode circuits with multiple inputs and multiple outputs whose output currents are products and/or quotients of powers of the input currents. These circuits are made up of multiple-input floating-gate MOS (FGMOS) transistors operating in the subthreshold regime. The powers are set by capacitor ratios; hence, they can be quite accurate. We analyze the general family of such circuits and present experimental data from several members that we fabricated in a standard 2μm double-poly p-well process through MOSIS.

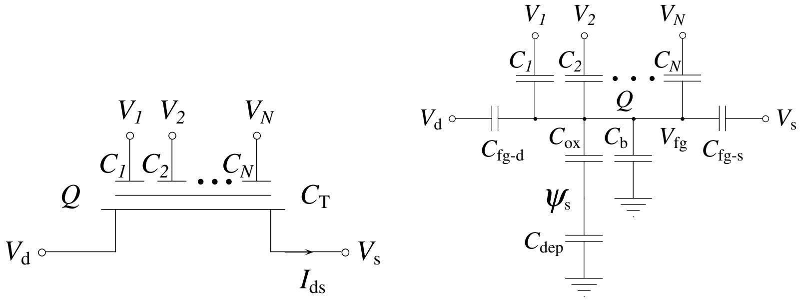
1. Introduction

Information processing using analog VLSI systems has recently become the subject of much interest and active research [1], [2]. In particular, the current-mode approach is the focus of much attention [3]. In this paradigm, the quantities of interest are represented by currents, whereas the circuit voltages are thought of as playing only an incidental role. Among the vast array of nonlinear operations required to perform current-mode signal processing, the class consisting of products, quotients, powers, and roots is particularly useful.

We have long known that we can obtain such nonlinearities by logging the input quantities, taking appropriate weighted sums and differences of the resulting logged quantities, and antilogging them back into the original signal domain [4]. Several circuits have been reported that operate according to this principle. In [5]–[7], the authors present current-mode circuits with various power-law transfer characteristics, in which the logging and antilogging are done through the exponential current/voltage relationship of the bipolar transistor, whereas the weighted summation is accomplished via a resistive divider. In [8], van der Gevel and Kuenen present a one-quadrant current multiplier, in which the logging and antilogging are done through the exponential current/voltage relationship of the subthreshold MOS transistor, whereas the weighted summation is accomplished via the capacitive divider formed between the MOS transistor's gate and its back-gate (i.e., substrate). In this paper, we describe a family of multiple-input, multiple-output current-mode circuits that also embodies this general principle.

We can also implement current-mode products, quotients, powers, and roots using translinear (TL) circuits [9], [10]. Consequently, the question of the relationship between translinear circuits and the family of the circuits just described arises naturally. Indeed, the circuits presented in this paper and the circuits of [5]–[8] *are* translinear circuits if the class of translinear circuits is extended to include circuits with loops that have voltage drops across elements that do not have exponential current/voltage relationships. We can analyze these circuits by applying the reformulated translinear principle of Hart [11]. However, the derivation developed in this paper results in a procedure for analyzing any particular circuit that is simple compared to that using Hart's translinear principle directly. Our analysis procedure also applies to the class of circuits implemented with bipolar transistors and resistive dividers that generalizes the power-law circuits of [5]–[7].

Floating-gate MOS (FGMOS) transistors have been used to great advantage in analog and digital VLSI systems as long-term, non-volatile storage devices. The quantity of charge stored on the insulated gate of this device has been used both as a free parameter that is adapted to increase the precision of analog circuits [12]–[14], and as a weight value in neural-network hardware im-



(a) (b)

Fig. 1. (a) Circuit symbol for an N-input native FGMOS transistor. (b) Capacitive-divider model of an N-input native FGMOS transistor.

plementations [15]–[18]. Shibata and Ohmi [19] recently proposed a marvelous new way of using floating-gate MOS transistors, in which multiple control gates capacitively couple into a floating gate, establishing its voltage as a weighted sum of the input voltages via a capacitive voltage divider. The channel current of the floating-gate transistor is a nonlinear function of the floating-gate voltage. In [19], these compound devices were dubbed neuron MOS (neuMOS or νMOS) transistors, based on a loose analogy between the function performed by these devices and by cells in the nervous system. A simple above-threshold model is derived in [19], and several interesting applications are discussed. Yang and Andreou develop a corresponding subthreshold model in [20], [21].

The family of circuits described in this paper uses the exponential current/voltage characteristic of the subthreshold FGMOS transistor, as well as the weighted summation afforded by the capacitive voltage divider, to compute products and/or quotients of powers of the input currents. The powers are set by capacitor ratios; hence, we can make them accurate by careful design techniques [22]. The charge stored on the floating gates in the circuits provide electronically adjustable, nonvolatile scale factors for the output currents. We have developed techniques for reliably controlling the floating-gate charge which is crucial if these circuits are to be of any practical use [18], [23].

2. Subthreshold FGMOS Transistor Model

The model of subthreshold operation of the N-input FGMOS transistor presented in this section is similar to that developed in [20]. It is included mainly to provide a starting point for the analysis of the family of current-mode circuits taken up in Section 3.2; consequently, we give only a brief sketch of the model derivation here.

A circuit symbol for an N-input native (i.e., substrate) FGMOS transistor is shown in Fig. 1a. The voltage on the n^{th} control gate, V_n, couples into the floating gate with a capacitance C_n. Now, if a net charge Q is stored on the floating gate, we can calculate the floating-gate voltage, V_{fg}, with the aid of the capacitive-divider model depicted in Fig. 1b. Without loss of generality, we measure all voltages relative to the substrate, and take the substrate to be the zero of potential. Applying conservation of charge to the floating node, we obtain

$$\begin{aligned} Q = C_{\text{ox}}(V_{\text{fg}} - \psi_{\text{s}}) + C_{\text{b}}V_{\text{fg}} - \sum_{n=1}^{N} C_n(V_n - V_{\text{fg}}) \\ -C_{\text{fg}-\text{s}}(V_{\text{s}} - V_{\text{fg}}) - C_{\text{fg}-\text{d}}(V_{\text{d}} - V_{\text{fg}}), \end{aligned} \tag{1}$$

where ψ_{s} is the surface potential in the channel; V_{s} and V_{d} are the source and drain voltages, respectively; C_{ox} is the gate-oxide capacitance; C_{dep} is the capacitance of the depletion layer beneath the channel; C_{b} is the parasitic capacitance from the floating gate to the substrate; and $C_{\text{fg}-\text{s}}$ and $C_{\text{fg}-\text{d}}$ are the parasitic overlap capacitances coupling the floating gate to the source and drain, respectively. Rearranging Eq. 1 and solving for V_{fg} yields

$$\begin{aligned} V_{\mathrm{fg}} = \frac{C_{\mathrm{ox}}}{C_{\mathrm{T}}^{*}}\psi_{\mathrm{s}} + \frac{Q}{C_{\mathrm{T}}^{*}} + \sum_{n=1}^{N}\frac{C_n}{C_{\mathrm{T}}^{*}}V_n \\ + \frac{C_{\mathrm{fg-s}}}{C_{\mathrm{T}}^{*}}V_{\mathrm{s}} + \frac{C_{\mathrm{fg-d}}}{C_{\mathrm{T}}^{*}}V_{\mathrm{d}}, \end{aligned} \tag{2}$$

where $C_{\mathrm{T}}^{*} \equiv C_{\mathrm{ox}} + C_{\mathrm{b}} + \sum_{n=1}^{N} C_n + C_{\mathrm{fg-s}} + C_{\mathrm{fg-d}}$. As in [1], we write

$$\psi_{\mathrm{s}} \approx \psi_0 + \kappa V_{\mathrm{fg}}, \tag{3}$$

where $\kappa \equiv \frac{C_{\mathrm{ox}}}{C_{\mathrm{ox}}+C_{\mathrm{dep}}}$. Substituting Eq. 2 into Eq. 3 and rearranging, we obtain

$$\begin{aligned} \psi_{\mathrm{s}} = \frac{C_{\mathrm{T}}^{*}}{C_{\mathrm{T}}}\psi_0 + \frac{\kappa Q}{C_{\mathrm{T}}} + \kappa\sum_{n=1}^{N}\frac{C_n}{C_{\mathrm{T}}}V_n \\ + \kappa\frac{C_{\mathrm{fg-s}}}{C_{\mathrm{T}}}V_{\mathrm{s}} + \kappa\frac{C_{\mathrm{fg-d}}}{C_{\mathrm{T}}}V_{\mathrm{d}}, \end{aligned} \tag{4}$$

where $C_{\mathrm{T}} \equiv (C_{\mathrm{ox}}||C_{\mathrm{dep}}) + C_{\mathrm{b}} + \sum_{n=1}^{N} C_n + C_{\mathrm{fg-s}} + C_{\mathrm{fg-d}}$.

In subthreshold, current flows in the MOS channel primarily by diffusion, so the drain current is given by

$$I_{\mathrm{ds}} = -WqD\frac{\partial N}{\partial x},$$

where W is the channel width, q is the charge of an electron, D is the diffusion coefficient of channel electrons, and $N(x)$ is the electron concentration along the channel. Because no carriers are lost in the channel, the carrier concentration is a linear function of position along the channel,

$$\begin{aligned} I_{\mathrm{ds}} &= -WqD\tfrac{N_{\mathrm{d}}-N_{\mathrm{s}}}{L} \\ &= qDW\frac{N_0\exp\left\{\frac{\psi_{\mathrm{s}}-V_{\mathrm{s}}}{U_{\mathrm{T}}}\right\} - N_0\exp\left\{\frac{\psi_{\mathrm{s}}-V_{\mathrm{d}}}{U_{\mathrm{T}}}\right\}}{L} \\ &= qD\tfrac{W}{L}N_0\exp\left\{\tfrac{\psi_{\mathrm{s}}}{U_{\mathrm{T}}}\right\} \\ &\quad \times\left(\exp\left\{-\tfrac{V_{\mathrm{s}}}{U_{\mathrm{T}}}\right\} - \exp\left\{-\tfrac{V_{\mathrm{d}}}{U_{\mathrm{T}}}\right\}\right). \end{aligned} \tag{5}$$

Substituting Eq. 4 into Eq. 5 yields

$$\begin{aligned} I_{\mathrm{ds}} &= I_0\exp\left\{\tfrac{\kappa Q}{C_{\mathrm{T}}U_{\mathrm{T}}}\right\}\exp\left\{\tfrac{\kappa}{C_{\mathrm{T}}U_{\mathrm{T}}}\sum_{n=1}^{N}C_nV_n\right\} \\ &\quad \times\exp\left\{\tfrac{\kappa C_{\mathrm{fg-d}}V_{\mathrm{d}}}{C_{\mathrm{T}}U_{\mathrm{T}}}\right\}\exp\left\{\tfrac{\kappa C_{\mathrm{fg-s}}V_{\mathrm{s}}}{C_{\mathrm{T}}U_{\mathrm{T}}}\right\} \\ &\quad \times\left(\exp\left\{-\tfrac{V_{\mathrm{s}}}{U_{\mathrm{T}}}\right\} - \exp\left\{-\tfrac{V_{\mathrm{d}}}{U_{\mathrm{T}}}\right\}\right), \end{aligned} \tag{6}$$

where $I_0 \equiv qD\frac{W}{L}N_0\exp\left\{\frac{C_{\mathrm{T}}^{*}\psi_0}{C_{\mathrm{T}}U_{\mathrm{T}}}\right\}$, Q is the net charge stored on the floating gate, U_{T} is the thermal voltage $\frac{kT}{q}$, and C_{T} is the total capacitance seen by the floating gate.

Now, if the source of the FGMOS transistor is at ground and the drain voltage is more than a few U_{T} above ground, the transistor will be saturated and Eq. 6 reduces to

$$\begin{aligned} I_{\mathrm{ds}} &= I_0\exp\left\{\tfrac{\kappa Q}{C_{\mathrm{T}}U_{\mathrm{T}}}\right\}\exp\left\{\tfrac{\kappa}{C_{\mathrm{T}}U_{\mathrm{T}}}\textstyle\sum_{n=1}^{N}C_nV_n\right\} \\ &\quad \times\exp\left\{\tfrac{\kappa C_{\mathrm{fg-d}}V_{\mathrm{d}}}{C_{\mathrm{T}}U_{\mathrm{T}}}\right\}. \end{aligned}$$

Further, if we neglect the parasitic overlap capacitance between the floating gate and drain, we have

$$I_{\mathrm{ds}} = I_0\exp\left\{\frac{\kappa Q}{C_{\mathrm{T}}U_{\mathrm{T}}}\right\}\exp\left\{\frac{\kappa}{C_{\mathrm{T}}U_{\mathrm{T}}}\sum_{n=1}^{N}C_nV_n\right\}. \tag{7}$$

Equation Eq. 7 will be the starting point for the analysis of the next section. We shall return to the matter of neglecting the parasitic overlap capacitance between the floating gate and drain in the discussion section.

3. Subthreshold FGMOS Translinear Circuits

In this section, we shall analyze subthreshold FGMOS translinear circuits in two different ways. First, we shall examine a simple circuit and analyze it using the usual technique involving translinear loops. Then, we shall develop a general analysis technique which is more suited to analyze the circuits under consideration.

3.1. Analysis Using Standard TL Principle

Consider the circuit shown in Fig. 2. There are two input FGMOS transistors, M_1 and M_2, and one output FGMOS transistor, M_3. The drain of M_1 couples into its own floating gate through two capacitors each of which has a capacitance C. Likewise the drain of M_2 couples into its own floating gate through two capacitors each of which has a capacitance C. The drains of M_1 and M_2 each couple into the floating gate of M_3 through a single capacitor of capacitance C. The first input current, I_1 is sourced into the drain of M_1,

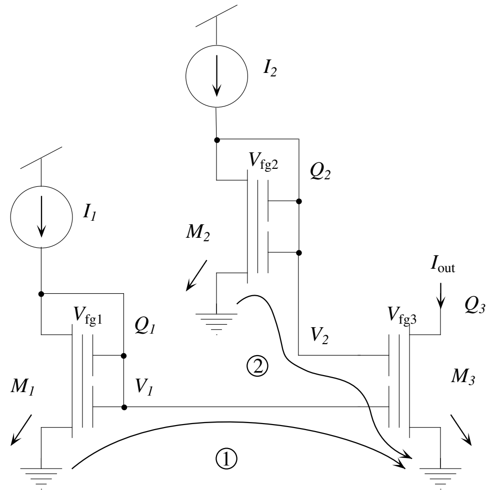


Fig. 2. Subthreshold FGMOS translinear circuit. The first input current, I_1 is sourced into the drain of transistor M_1, causing the drain voltage, V_1, to form. The drain of M_1 couples into its own floating gate through two capacitors, each having a capacitance of C. Likewise, the second input current, I_2, is sourced into the drain of transistor M_2, causing drain voltage, V_2, to form. The drain of M_2 also couples into its own floating gate through two capacitors (again, each with capacitance C). The circuit makes a single output current, I_{out}, in transistor M_3 by summing V_1 and V_2 through capacitors of equal size (again, each with capacitance C) to form V_{fg3}. Q_1, Q_2, and Q_3 are the net charge stored on the floating gates of transistors M_1, M_2, and M_3, respectively. Two translinear loops are shown.

causing the drain voltage, V_1, to form. Likewise, the second input current, I_2, is sourced into the drain of M_2, causing drain voltage, V_2, to form. The circuit makes a single output current, I_{out}, in M_3 by summing V_1 and V_2 on the floating gate of M_3. Q_1, Q_2, and Q_3 are the net charge stored on the floating gates of transistors M_1, M_2, and M_3, respectively. V_{fg1}, V_{fg2}, and V_{fg3} are the floating-gate voltages of transistors M_1, M_2, and M_3, respectively.

We will analyze the circuit of Fig. 2 using Hart's reformulated translinear principle [11]. Kirchoff's voltage law (KVL) applied around loop 1 implies that

$$V_{\mathrm{fg1}} + (V_1 - V_{\mathrm{fg1}}) + (V_{\mathrm{fg3}} - V_1) - V_{\mathrm{fg3}} = 0,$$

which, in turn, implies that

$$V_{\mathrm{fg3}} = V_{\mathrm{fg1}} + (V_{\mathrm{fg3}} - V_{\mathrm{fg1}}). \tag{8}$$

If the FGMOS transistors are operating in subthreshold, I_1 is related to V_{fg1} by

$$I_1 = I_0 \exp\left\{\frac{\kappa V_{\mathrm{fg1}}}{U_{\mathrm{T}}}\right\}, \tag{9}$$

and I_{out} is related to V_{fg3} by

$$I_{\mathrm{out}} = I_0 \exp\left\{\frac{\kappa V_{\mathrm{fg3}}}{U_{\mathrm{T}}}\right\}. \tag{10}$$

Substituting Eq. 9 and Eq. 10 into Eq. 8 and rearranging, we obtain

$$I_{\mathrm{out}} = I_1 \exp\left\{\frac{\kappa(V_{\mathrm{fg3}} - V_{\mathrm{fg1}})}{U_{\mathrm{T}}}\right\}. \tag{11}$$

Applying the same procedure around loop 2, we obtain

$$I_{\mathrm{out}} = I_2 \exp\left\{\frac{\kappa(V_{\mathrm{fg3}} - V_{\mathrm{fg2}})}{U_{\mathrm{T}}}\right\}. \tag{12}$$

Multiplying Eq. 11 and Eq. 12 together, we obtain

$$I_{\mathrm{out}}^2 = I_1 I_2 \exp\left\{\frac{\kappa(2V_{\mathrm{fg3}} - (V_{\mathrm{fg1}} + V_{\mathrm{fg2}}))}{U_{\mathrm{T}}}\right\}. \tag{13}$$

Applying the capacitive-divider relationship (Eq. 2) to each of the floating gates in turn, we obtain

$$\begin{aligned} V_{\mathrm{fg1}} &= \tfrac{2C}{C_{\mathrm{T}}} V_1 + \tfrac{Q_1}{C_{\mathrm{T}}}, \\ V_{\mathrm{fg2}} &= \tfrac{2C}{C_{\mathrm{T}}} V_2 + \tfrac{Q_2}{C_{\mathrm{T}}}, \\ V_{\mathrm{fg3}} &= \tfrac{C}{C_{\mathrm{T}}} V_1 + \tfrac{C}{C_{\mathrm{T}}} V_2 + \tfrac{Q_3}{C_{\mathrm{T}}}, \end{aligned}$$

from which we calculate

$$2V_{\mathrm{fg3}} - (V_{\mathrm{fg1}} + V_{\mathrm{fg2}}) = \frac{1}{C_{\mathrm{T}}}(2Q_3 - (Q_1 + Q_2)). \tag{14}$$

Substituting Eq. 14 into Eq. 13 and taking the square root of both sides, we obtain

$$I_{\mathrm{out}} = \sqrt{I_1 I_2} \exp\left\{\frac{\kappa}{C_{\mathrm{T}} U_{\mathrm{T}}}(Q_3 - \frac{1}{2}(Q_1 + Q_2))\right\}.$$

So, the circuit of Fig. 2 is a two-input geometric-mean circuit. The output current is scaled by a constant coefficient involving the charge on the floating gates. Note that this coefficient is unity if $Q_1 = Q_2 = Q_3$.

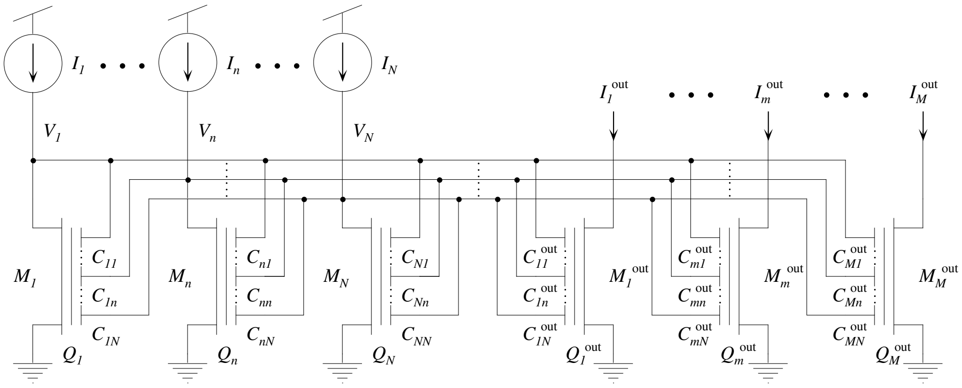


Fig. 3. Schematic of a generalized FGMOS translinear circuit. There are N input transistors labeled M_1 through M_N and M output transistors labeled M_1^{out} through M_M^{out}. N input currents ($I_1, \ldots, I_N$) are sourced into the drains of the N input transistors, causing N drain voltages ($V_1, \ldots, V_N$) to develop that will depend on the $N \times N$ input connectivity matrix, $\mathbf{C}$. C_{nk} is a measure of the strength of the capacitive coupling between the drain of transistor M_k and the floating gate of transistor M_n. The circuit forms M output currents ($I_1^{\text{out}}, \ldots, I_M^{\text{out}}$) by combining the N drain voltages according to the $M \times N$ output connectivity matrix, $\mathbf{C}^{\text{out}}$. C_{mn}^{out} is a measure of the strength of the capacitive coupling between the drain of transistor M_n and the floating gate of transistor M_m^{out}.

We can use Hart's reformulated translinear principle in a similar manner to analyze any particular circuit in the class under consideration, but it is evident from the analysis just presented that this procedure could be very cumbersome for more complicated circuits. Consequently, in Section 3.2, we shall develop an analysis procedure that is more systematic and relatively straightforward to use.

3.2. General Formulation

Consider the circuit depicted in Fig. 3. There are N input FGMOS transistors labeled M_1 through M_N, and M output FGMOS transistors labeled M_1^{out} through M_M^{out}. Charges $Q_1, \ldots, Q_N$ are stored on the floating gates of transistors M_1 through M_N, respectively. Likewise, the charges $Q_1^{\text{out}}, \ldots, Q_M^{\text{out}}$ are stored on the floating gates of transistors M_1^{out} through M_M^{out}, respectively. The drain of transistor M_n couples into the floating gate of transistor M_k through capacitor C_{kn}, and into the floating gate of transistor M_m^{out} through capacitor C_{mn}^{out}. If there is no connection between the drain of transistor M_n and the floating gate of transistor M_k, C_{kn} is zero. Likewise, if there is no connection between the drain of transistor M_n and the floating gate of transistor M_m^{out}, C_{mn}^{out} is zero. Together, the elements C_{kn} constitute an $N \times N$ input connectivity matrix, $\mathbf{C}$. Likewise, the elements C_{mn}^{out} make up an $M \times N$ output connectivity matrix, $\mathbf{C}^{\text{out}}$. The elements of $\mathbf{C}$ and $\mathbf{C}^{\text{out}}$ do not need to be actual capacitances; they can be any values that are proportional to the actual capacitances (e.g., areas, relative areas, number of identical capacitors), as long as consistency is maintained.

N input currents ($I_1, \ldots, I_N$) are sourced into the drains of transistors M_1 through M_N, respectively. As a result, drain voltages ($V_1, \ldots, V_N$) will develop that depend on the input connectivity matrix, $\mathbf{C}$. The circuit forms M output currents ($I_1^{\text{out}}, \ldots, I_M^{\text{out}}$) in the transistors M_1^{out} through M_M^{out} by combining the N drain voltages through the output connectivity matrix $\mathbf{C}^{\text{out}}$. We shall show that the m^{th} output current is given by

$$I_m^{\text{out}} = K_m \prod_{n=1}^{N} I_n^{\Lambda_{mn}}, \tag{15}$$

where

$$\Lambda_{mn} \equiv \sum_{k=1}^{N} C_{mk}^{\text{out}} C_{kn}^{-1} \tag{16}$$

(or, equivalently, $\mathbf{\Lambda} \equiv \mathbf{C}^{\text{out}}\mathbf{C}^{-1}$) and

$$K_m \equiv \exp\left\{ \frac{\kappa}{C_{\text{T}} U_{\text{T}}} \left(Q_m^{\text{out}} - \sum_{n=1}^{N} \Lambda_{mn} Q_n\right) \right\}. \tag{17}$$

In other words, the m^{th} output current is a product of powers of the N input currents; I_n factors into I_m^{out} raised to the power Λ_{mn}. We shall also show that each of the rows of $\mathbf{\Lambda}$ sums to unity (i.e., $\sum_{n=1}^{N} \Lambda_{mn} = 1$) so the dimensions of Eq. 15 are correct. Finally, we shall show that the constant of proportionality is unity if the same quantity of charge is stored on each of the floating gates; that is,

$$I_m^{\text{out}} = \prod_{n=1}^{N} I_n^{\Lambda_{mn}}.$$

In the analysis that follows, we shall assume that all FGMOS transistors are perfectly matched. In particular, the parameters I_0, κ, and C_{T} are the same for all FGMOS transistors in the circuit. This condition also requires that each of the rows of $\mathbf{C}$ and $\mathbf{C}^{\text{out}}$ sum to the same constant. That is, for all n and m,

$$\sum_{k=1}^{N} C_{nk} = \sum_{k=1}^{N} C_{mk}^{\text{out}} \equiv C.$$

Also, we shall assume that the input connectivity matrix, $\mathbf{C}$, has an inverse, $\mathbf{C}^{-1}$.

After a sufficiently long time, Kirchoff's current law (KCL) applied at the drain of the n^{th} input transistor implies that the n^{th} sourced current, I_n, will equal the channel current of the n^{th} input FGMOS transistor; that is,

$$I_n = I_0 \exp\left\{\frac{\kappa Q_n}{C_{\text{T}} U_{\text{T}}}\right\} \exp\left\{\frac{\kappa}{C_{\text{T}} U_{\text{T}}} \sum_{k=1}^{N} C_{nk} V_k\right\}.$$

After rearranging, taking logarithms, and solving for V_k, we obtain

$$V_k = \frac{C_{\text{T}} U_{\text{T}}}{\kappa} \sum_{n=1}^{N} C_{kn}^{-1} \log \frac{I_n}{I_0} - \sum_{n=1}^{N} C_{kn}^{-1} Q_n. \tag{18}$$

The m^{th} output current is given by

$$I_m^{\text{out}} = I_0 \exp\left\{\frac{\kappa Q_m^{\text{out}}}{C_{\text{T}} U_{\text{T}}}\right\} \exp\left\{\frac{\kappa}{C_{\text{T}} U_{\text{T}}} \sum_{k=1}^{N} C_{mk}^{\text{out}} V_k\right\}. \tag{19}$$

Substituting Eq. 18 into Eq. 19, we obtain

$$\begin{aligned} I_m^{\text{out}} &= I_0 \exp\left\{\tfrac{\kappa}{C_{\text{T}} U_{\text{T}}}\left(Q_m^{\text{out}} - \sum_{n=1}^{N}\sum_{k=1}^{N} C_{mk}^{\text{out}} C_{kn}^{-1} Q_n\right)\right\} \\ &\quad \times \exp\left\{\sum_{n=1}^{N}\sum_{k=1}^{N} C_{mk}^{\text{out}} C_{kn}^{-1} \log \tfrac{I_n}{I_0}\right\}. \end{aligned} \tag{20}$$

If we apply the definitions of Λ_{mn} (Eq. 16) and K_m (Eq. 17), Eq. 20 becomes

$$\begin{aligned} I_m^{\text{out}} &= I_0 K_m \exp\left\{\sum_{n=1}^{N} \Lambda_{mn} \log \tfrac{I_n}{I_0}\right\} \\ &= I_0 K_m \prod_{n=1}^{N} \exp\left\{\log \left(\tfrac{I_n}{I_0}\right)^{\Lambda_{mn}}\right\} \\ &= I_0 K_m \prod_{n=1}^{N} \left(\tfrac{I_n}{I_0}\right)^{\Lambda_{mn}}. \end{aligned}$$

Thus, we have that

$$I_m^{\text{out}} = I_0^{\left(1-\sum_{n=1}^{N} \Lambda_{mn}\right)} K_m \prod_{n=1}^{N} I_n^{\Lambda_{mn}}.$$

It can be shown (see Appendix A) that the quantity $\sum_{n=1}^{N} \Lambda_{mn} = 1$, if, as we have assumed, all FGMOS transistors are identical and the input connectivity matrix, $\mathbf{C}$, has an inverse. Thus, we have that

$$I_m^{\text{out}} = K_m \prod_{n=1}^{N} I_n^{\Lambda_{mn}}.$$

If $Q_m^{\text{out}} = Q_n \equiv Q$, we have that

$$\begin{aligned} K_m &= \exp\left\{\tfrac{\kappa Q}{C_{\text{T}} U_{\text{T}}}\left(1 - \sum_{n=1}^{N} \Lambda_{mn}\right)\right\} \\ &= 1. \end{aligned}$$

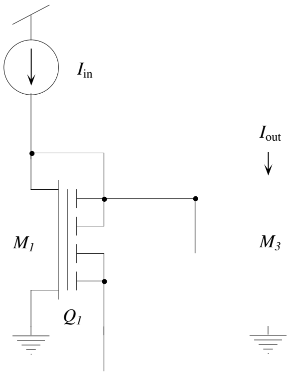
So, we have that

$$I_m^{\text{out}} = \prod_{n=1}^{N} I_n^{\Lambda_{mn}},$$

which is what we set out to show.

4. Experimental Results

In this section, we present experimental data from several subthreshold FGMOS translinear circuits


I_{in}
I_{out}
M_1
M_3
Q_1