Continuous-Time Feedback in Floating-Gate MOS Circuits

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Abstract— **We present the negative- and positive-feedback circuit configurations of continuous-time floating-gate MOS circuits. We start by reviewing the dynamics of our pFET and nFET single-transistor synapses. We present the range of possible stabilizing and destabilizing types of feedback in circuits with one floating-gate synapse, including data from nFET and pFET synapses. We then show examples of competitive and cooperative behavior in multiple-synapse circuits. We present experimental data from circuits fabricated in the 2μm nwell CMOS process available through MOSIS; we see similar experimental effects in 1.2μm and 0.5μm processes.**

A silicon synapse must satisfy two requirements in as dense and power-efficient implementation as possible. First, it must compute the product of the input multiplied by the synapse strength, or the weight of the synapse [1-5]. Second, it must locally implement a learning rule for modifying the weight on the floating gate; in our case, the form of this rule depends on how various *error signals* are fed back to the floating gate synapse. The nature of this feedback is the focus of this paper. The usefulness of negative or positive feedback depends on the application; Hebbian learning, for example, is a case of destabilizing positive feedback.

This paper considers the behaviors that emerge when single-transistor synapses are coupled together to form various continuous-time adaptive networks. Our purpose is to understand the dynamics of the learning mechanisms naturally available in floating-gate MOS circuits. The starting point is our models of the channel current, electron-tunneling current, and hot-electron–injection current of nFET and pFET floating-gate synapses. We present experimental data from circuits fabricated in the 2μm nwell CMOS process available through MOSIS; we have seen similar scaled results in the 1.2μm and 0.5μm processes available through MOSIS. We have characterized and modeled the dynamics of nFET and pFET single-transistor synapses operating in continuous-time circuits. This work builds the framework to consider floating-gate circuits not only as memory elements, but as continuous-time circuit elements computing at several timescales.

I. Single-Transistor Synapses

Figure 1 shows the circuit models for the nFET and pFET single-transistor synapses, respectively. We show the layout and cross section for the pFET device elsewhere in this journal [5]. Because the input signals are capacitively coupled to the floating gate, we model voltage and current swings around the circuit's steady-state values. We

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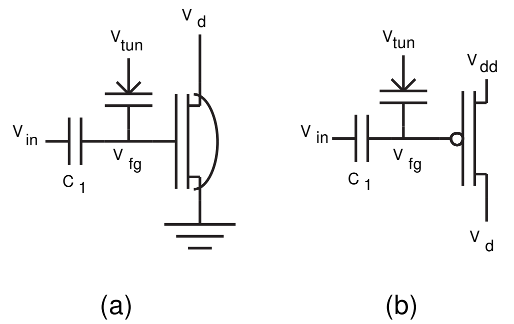


Fig. 1. (a) Circuit diagram of the nFET single-transistor synapse with its source connected to ground. (b) Circuit diagram of the pFET single-transistor synapse with its source connected to V_{dd}. For our discussion, we will assume non-negligable amounts of electron-tunneling and hot-electron-injection current in these nFET and pFET transistors.

consider the single-transistor synapse operating with subthreshold channel currents. Many of the behaviors extend qualitatively to above-threshold operation, but as is true of the AFGA [3], the quantitative behaviors do not. We describe the subthreshold nFET or pFET channel current in saturation, I_s, for a change in the FET's floating-gate voltage, ΔV_{fg}, and drain-to-source voltage, ΔV_{ds}, around a bias current, I_{so}, as [6]

$$\begin{aligned} \text{nFET:} \quad & I_s = I_{so} \exp\left(\frac{\kappa_n \Delta V_{fg} - \Delta V_s}{U_T}\right) \exp\left(\frac{\Delta V_{ds}}{V_A}\right), \\ \text{pFET:} \quad & I_s = I_{so} \exp\left(\frac{\Delta V_s - \kappa_p \Delta V_{fg}}{U_T}\right) \exp\left(-\frac{\Delta V_{ds}}{V_A}\right), \end{aligned} \tag{1}$$

where κ_p is the fractional change in the pFET surface potential due to a change in ΔV_{fg}, κ_n is the fractional change in the nFET surface potential due to a change in ΔV_{fg}, V_A is the Early voltage of the nFET or pFET, and U_T is the thermal voltage, $\frac{kT}{q}$. In (1), we use a modified form of the Early voltage expression that is consistent with classical formulations for large V_A, and more closely models the behavior for small V_A. We showed previously that the Early voltage decreases at large drain-to-source voltages due to impact ionization in the drain-to-channel depletion region [3]. We assume that all the floating-gate devices are matched. We model the floating-gate behavior by equating the currents at the floating gate:

$$C_T \frac{dV_{fg}}{dt} = C_1 \frac{dV_{in}}{dt} + C_2 \frac{dV_d}{dt} + I_{tun} - I_{inj} \tag{2}$$

where I_{tun} and I_{inj} are the floating-gate currents due to electron tunneling and hot-electron injection, which we will discuss in subsection I-A and I-B. We define C_T as the

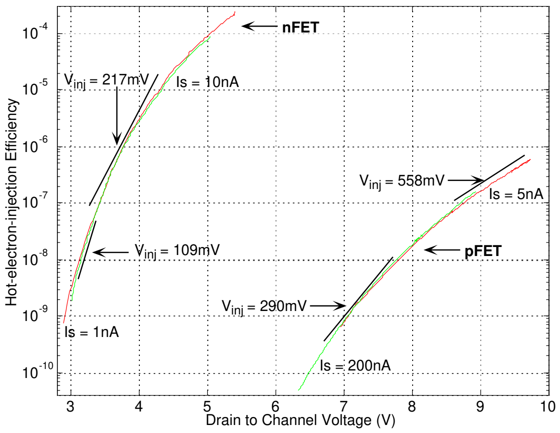


Fig. 2. nFET and pFET Hot-electron injection efficiency ($\frac{I_{inj}}{I_s}$) versus Φ_{dc} for two values of source current. The two different source current values are nearly equal, which is consistent with injection efficiency being independent of source current. We show the linearized slope (V_{inj}) on this exponential scale for two Φ_{dc} biases. The slope of both curves on this exponential scale decrease with increasing Φ_{dc}. The moderately doped nFET substrate ($1 \times 10^{17} cm^{-3}$) increases the efficiency of the nFET hot-electron–injection process by increasing the electric field in the channel.

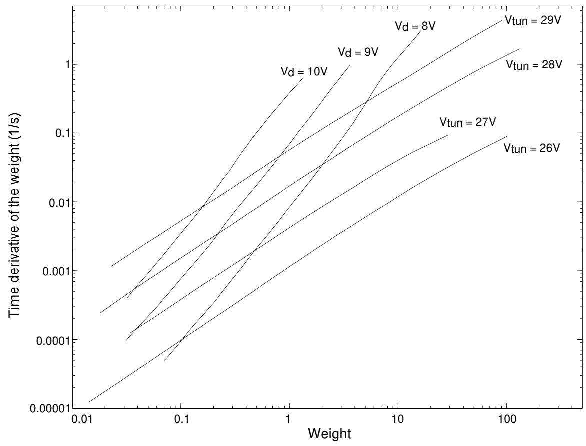


Fig. 3. Plot of $\frac{dI_s}{dt}$ as a function of I_s for four different tunneling and three different drain voltages. This measurement gives the floating-gate weight update rule as a function of I_s. Plotting the data in this way shows the power-law dependence of channel current on the floating-gate current. We measured this injection (tunneling) data by starting the synapse at a low (or high) source current. The source-current bias for this synapse was 10nA. For a pFET synapse, the tunneling voltages are referenced to V_{dd}.

total amount of capacitance connected to the floating gate, and C_2 as the capacitance between floating gate and drain (which is not explicitly drawn for clarity).

A. Electron Tunneling

We use electron tunneling to remove electrons from floating gates; we present more detailed discussions elsewhere [1], [3] as well as in this journal issue [?]. As we showed elsewhere, we approximate the tunneling current for a fixed bias on the tunneling line by

$$I_{tun} = I_{tun0} e^{(\Delta V_{tun} - \Delta V_{fg})/V_x}, \quad (3)$$

where V_x is a parameter related to the quiescent tunneling and floating-gate voltages, ΔV_{tun} is the change in the tunnneling voltage, and ΔV_{fg} is the change in the floating-gate voltage from the quiescent floating-gate voltage [3], [5]. For our operating conditions, a typical value of V_x is $1V$ with the 42nm oxide used in the $2.0\mu m$ Orbit process. For a fixed source voltage, we express the tunneling current in terms of this floating-gate transistor's source current by substituting (1) into (3):

$$\text{nFET}: I_{tun} = I_{tun0} \left(\frac{I_s}{I_{so}} \right)^{-\frac{U_T}{\kappa_n V_x}},$$

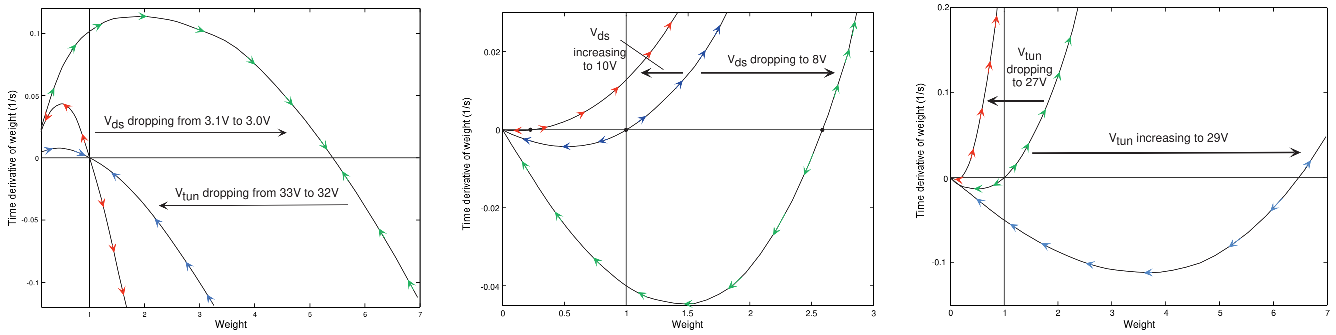
$$\text{pFET}: I_{tun} = I_{tun0} \left(\frac{I_s}{I_{so}} \right)^{\frac{U_T}{\kappa_p V_x}}. \quad (4)$$

B. Hot-Electron Injection

We use hot-electron injection to add electrons to floating gates [1], [3]. If we are to inject an electron onto a floating gate, the MOSFET must have a high-electric-field region ($>10\text{V}/\mu m$) to accelerate channel electrons to energies above the silicon–silicon-dioxide barrier, and in that region the oxide electric field must transport the electrons that surmount the barrier to the floating gate. We present elsewhere more detailed discussions of nFET hot-electron injection [1], [3]., and we present elsewhere [2], [?], [3] and in this journal issue [5] more detailed discussions of pFET hot-electron injection. Figure 2 shows the nFET and pFET hot-electron injection efficiency, $\frac{I_{inj}}{I_s}$, as a function of Φ_{dc} for two different source currents. We raise the nFET threshold voltage to permit hot-electron injection with subthreshold channel currents. We use a p-type implant ($1 \times 10^{17} cm^{-3}$) to guarantee that the oxide electric field will transport electrons to the floating gate [1]. The nFET's substrate implant results in higher electric fields in its drain-to-channel region compared with the electric fields in the pFET; therefore, the nFET's hot-electron–injection efficiency is much larger than the pFET's injection efficiency for an equivalent Φ_{dc}. Impact ionization provides the source of electrons for pFET hot-electron injection, and is proportional to the source current [2], [3]. As seen in Fig. ??b, f_2 is approximately linear over a 1V change in Φ_{dc}; therefore, around a quiescent level of Φ_{dc}, the injection current will e-fold for a Φ_{dc} increase of V_{inj}. Figure 2 also illustrates the nFET and pFET V_{inj} parameters and their range of validity. As we derived previously [1], [2], the hot-electron injection current as a function of terminal voltages and currents using this linear model is

$$\begin{aligned} \text{nFET:} \quad & I_{inj} = I_{inj0} \left(\frac{I_s}{I_{s0}} \right)^{\alpha} \exp\left(\frac{\Delta V_d}{V_{inj}} \right), \\ \text{pFET:} \quad & I_{inj} = I_{inj0} \left(\frac{I_s}{I_{s0}} \right)^{\alpha} \exp\left(-\frac{\Delta V_d}{V_{inj}} \right), \end{aligned} \quad (5)$$

where I_{inj0} is the quiescent tunneling current, and α is $1 - \frac{U_T}{V_{inj}}$. A typical nFET value of α is 0.70, and a typical



(a) (b) (c)

Fig. 4. Experimental measurements of the time-derivative of W versus W for the nFET and pFET synapses. The arrows show the direction that the differential equation will take. (a) nFET synapse Measurements. This synapse will stabilize to the $W = 1$ steady state; the weight is defined around a bias current of 9nA. We show the effect of changing the drain-voltage bias and the tunneling-voltage bias on the weight value. (b) pFET synapse measurements for three different drain-voltage biases, and a xxV tunneling voltage. The weight is defined around a bias current of 20nA. This synapse will diverge from the $W = 1$ steady state. Increasing the drain-voltage bias decreases the steady-state weight value; decreasing the drain-voltage increases the steady-state weight value. (c) pFET synapse measurements for three different tunneling-voltage biases, and a xxV drain-to-source voltage. The weight is defined around a bias current of roughly 8nA. Increasing the tunneling-bias voltage increases the steady-state weight value, because more current is necessary for the injection current to balance the larger tunneling current. Decreasing the tunneling-voltage decreases the steady-state weight value.

pFET value of α is 0.90; both values are consistent with typical values of V_{inj}.

C. Dynamical Equations for Floating-Gate Devices

To analyze the adaptation behavior in FGMOS circuits, we often decompose our variables into components that change at fast and slow rates. The fast-rate variables represent the rapid changes due to the input signals; the slow-rate variables represent the floating-gate charge (the synapse weights). In other discussions, we have presented the complete expansion of these two timescales [3], [4], [5], in particular to analyze the effect of sinusoidal inputs on the slow-timescale dynamics [5]. In this discussion, we are only investigating the effects of the slow-rate variables, thereby simplifying the analysis shown elsewhere [4], [5]. For this paper, we define the weight of each floating-gate synapse, W, as the source current normalized by a bias current, I_{so}, or $W = I_s/I_{so}$. Further, we will assume that our gate inputs allow us to apply a step-function input to these weights.

We want to derive a dynamical model in terms of each transistor's weight value. The time derivative of W

$$\frac{dV_{fg}}{dt} = \frac{U_T}{\kappa_n W}\frac{dW}{dt} \tag{6}$$

for the nFET synapse. By substituting $\frac{dV_{fg}}{dt}$ in (6), we obtain the dynamical equations for slow timescales as

$$\begin{aligned} \text{nFET:} \quad & \frac{U_T C_T}{\kappa_n W}\frac{dW}{dt} = C_1\frac{dV_{in}}{dt} + C_2\frac{dV_d}{dt} + I_{tun} - I_{inj}, \\ \text{pFET:} \quad & -\frac{U_T C_T}{\kappa_p W}\frac{dW}{dt} = C_1\frac{dV_{in}}{dt} + C_2\frac{dV_d}{dt} + I_{tun} - I_{inj}, \end{aligned} \tag{7}$$

where I_{tun} is the electron tunneling current, and I_{inj} is the hot-electron injection current. Including the model for gate currents, we model the weight dynamics of an nFET synapse as

$$\frac{U_T C_T}{\kappa I_{tun0}}\frac{dW}{dt} = \frac{C_2 W}{I_{tun0}}\frac{dV_d}{dt} + W^{1-\frac{U_T}{\kappa_n V_x}} - W^{1+\alpha} e^{\Delta V_d/V_{inj}}, \tag{8}$$

and we model the weight dynamics of a pFET synapse as

$$-\frac{U_T C_T}{\kappa I_{tun0}}\frac{dW}{dt} = \frac{C_2 W}{I_{tun0}}\frac{dV_d}{dt} + W^{1+\frac{U_T}{\kappa_p V_x}} - W^{1+\alpha} e^{-\Delta V_d/V_{inj}}. \tag{9}$$

In Fig. 3, we plot the derivative of W versus W to illustrate the dependence of source current on the floating-gate currents for tunneling dynamics and for injection dynamics.

The more intuitive and useful part of this analysis is not the characterization type plots shown in Fig. 3 [3], [1], but looking at experimental data of $\frac{dW}{dt}$ versus W when using both tunneling current and hot-electron injection currents. In these cases, equilibrium occurs when the tunneling current exactly balances the injection current, but it may be either stable or unstable. Figure 4 shows experimental measurements verifying the dynamic behavior described by (8) and (9) for a fixed input and drain voltage for typical parameter values.) We see that the $W = 1$ equilibrium for the nFET synapse is stable, but that the $W = 1$ equilibrium for the pFET synapse is unstable. Figure 4 shows measurements of the time-derivative of W versus W for the nFET synapse for three bias conditions. The arrows show the direction that the differential equation will take. This figure shows that the nFET synapse will stabilize to the $W = 1$ steady state. This figure also shows the effect of changing the drain-voltage bias and the tunneling-voltage bias on the weight value. Figures 4b,c shows measurements of the time-derivative of W versus W for the pFET synapse for different tunneling-voltage and drain-voltage bias conditions. Figure 4 shows that an increasing the drain-voltage bias results in a lower equilibrium weight value. When the drain voltage increases, the weight will decrease, because less current (smaller weight) is required to balance

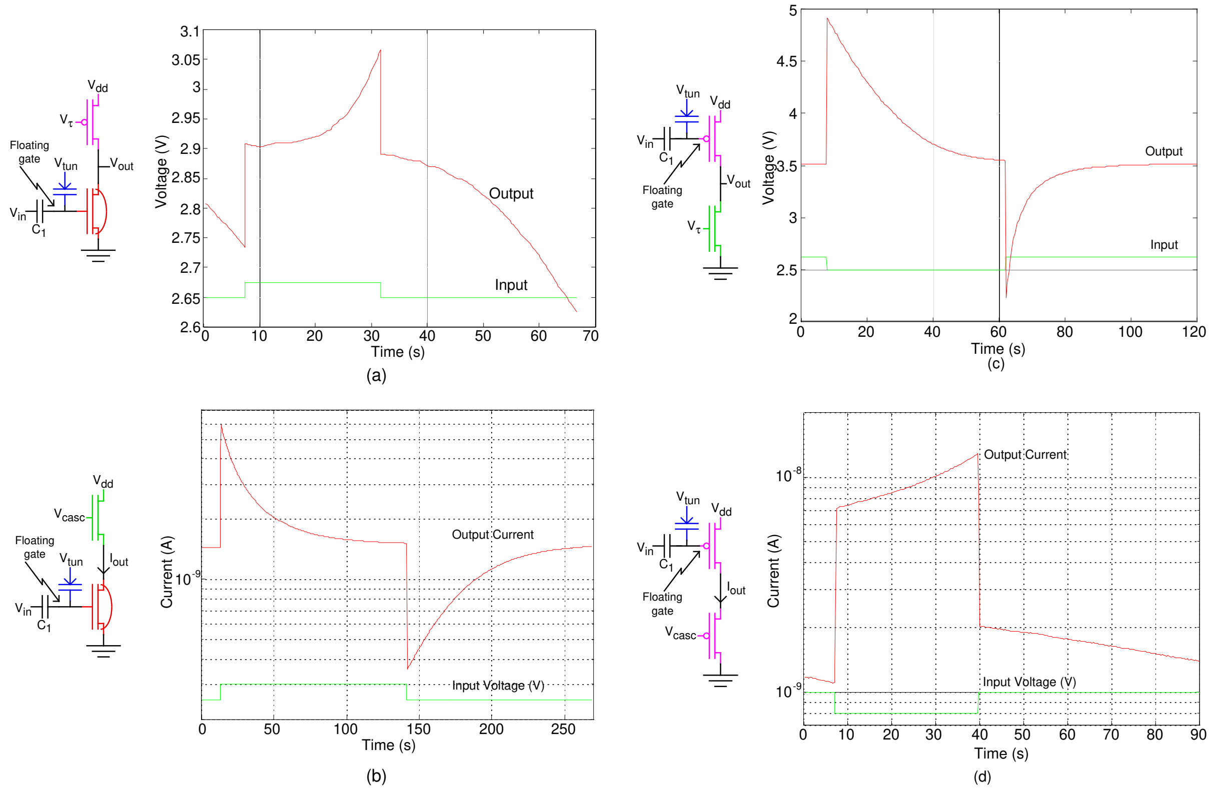


Fig. 5. Experimental measurements of dynamics fo circuits comprising a single nFET or pFET synapse. (a) The nFET voltage-adapting circuit configuration and its response to an upgoing and downgoing step input. The circuit configuration is unstable. (b) The nFET current-adapting circuit configuration and its response to an upgoing and downgoing step input. The circuit configuration is stable. (c) The pFET voltage-adapting circuit configuration, and its response to an upgoing and downgoing step input. This circuit is the autozeroing floating-gate amplifier (AFGA). The adaptation in response to an upward step results from electron tunneling; the adaptation in response to a downward step results from pFET hot-electron injection. This amplifier had a gain of 11.2, and I_{tun0} is $50fA$. (d) The pFET current-adapting circuit configuration, and its response to an upgoing and downgoing step input. The circuit configuration is unstable.

the roughly constant tunneling current. Figure 4 shows that an increasing the tunneling-voltage bias results in a higher equilibrium weight value. When the tunneling voltage increases, the weight will increase, because the more current (larger weight) is required to balance the increase in tunneling current.

II. Dynamics of Single-Synapse Circuits

We wil illustrate the basic floating-gate feedback mechanisms by considering the class of circuits composed of one synapse. We will restrict our discussion to synapse dynamics that depend only on the drain and floating-gate terminals; similar feedback mechanisms occur with other configurations that employ various combinations of the drain, source, and tunneling terminals.

The dynamic behavior of a single synapse can be characterized from that synapse's response in both a constant-current configuration and a constant-voltage configuration. Figure 5 shows the pFET and nFET circuits comprising a single synapse: first the circuits with the the drain connected to a current source, and second the circuits with the drain connected to a cascode transistor. Figure 9 shows how to simplify the small-signal models for the pFET circuits; we can similarly simplify the nFET circuits. We assume that the synapses have nonnegligible tunneling and injection currents. Figure 5 shows the pFET and nFET circuit responses to an upgoing and downgoing input step. For a pFET synapse, the constant-current configuration is stable, because the type of floating-gate feedback from its drain is stable. The autozeroing floating-gate amplifier (AFGA) is based on the stability of this configuration [2]. For an nFET synapse, the constant-voltage configuration is stable, because the type of floating-gate feedback from its floating gate is stable. The pFET synapse's constant-voltage configuration and the nFET-synapse's constant-current configuration are unstable circuits. For all four circuits, equilibrium is established when the tunneling current is balanced by the injection current.

From (8) and (9), we can analyticaly predict the behaviors in Fig. 5. First, consider the nFET and pFET circuits in the constant-current configuration. In both cases, the source current is fixed at I_{so} (W = 1). As a result, (1) governs the relationship between V_{fg} and V_d as

$$\frac{-\kappa_p \Delta V_{fg}}{U_T} - \frac{\Delta V_d}{V_o} = 0 \rightarrow \frac{\Delta V_d}{\Delta V_{fg}} = \frac{\kappa V_o}{U_T}; \qquad (10)$$

because the typical voltage gain (A_v) is 1000, the floating-gate voltage is nearly fixed. The tunneling current is held

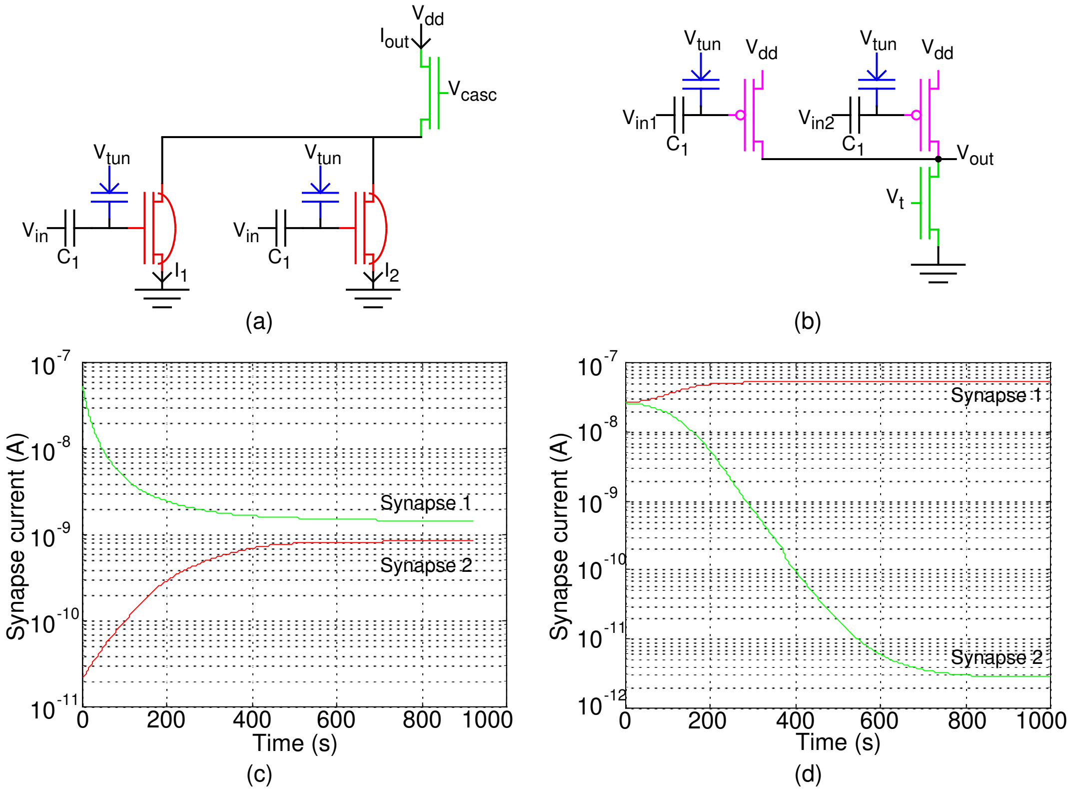


Fig. 6. Experimental of the behavior of coupled nFET and pFET synapses for fixed inputs. (a) Circuit of the two nFET synapses coupled at the drain with a cascode transistor. (b) Circuit of the two pFET synapses coupled at the drain with a current source. (c) The synapse current variation with time when the currents initially start far apart from each other. Both currents eventually converge to their steady state levels. (d) The synapse current variation with time when the currents initially start near each other. I_1 wins and I_2 loses, where I_2 decreases as a linear exponential in time due to the constant tunneling current at the floating gate. The measured I_2 saturates due to the surrounding leakage currents; the floating gate continues to increase with time.

constant at I_{tun0} because of the constant floating-gate voltage. Using these simplifications results in the model:

$$\text{nFET}: C_2 \frac{dV_{out}}{dt} = I_{tun0}\left(e^{\Delta V_{out}/V_{inj}} - 1\right),$$

$$\text{pFET}: C_2 \frac{dV_{out}}{dt} = I_{tun0}\left(e^{-\Delta V_{out}/V_{inj}} - 1\right). \qquad (11)$$

In the case of the AFGA, we previously showed that equations of this form can be solved analytically [2], [3]. The trajectories of the pFET equation converge to the steady state at $\Delta V_{out} = 0$, but the trajectories of the nFET equation diverge away from the steady state at $\Delta V_{out} = 0$.

Second, consider the nFET and pFET circuits in the constant-voltage configuration. Because the drain voltage of the pFET and nFET synapses are fixed by the cascode transistor, we simplify (8) and (9) to

$$\text{pFET}: \frac{C_T U_T}{\kappa_p I_{tun0}} \frac{dW}{dt} = -W^{1+\frac{U_T}{\kappa_p V_x}} + W^{1+\alpha},$$

$$\text{nFET}: \frac{C_T U_T}{\kappa_n I_{tun0}} \frac{dW}{dt} = W^{1-\frac{U_T}{\kappa_n V_x}} - W^{1+\alpha}. \qquad (12)$$

We can see the dynamics by rewriting these equations as

$$\text{nFET}: \frac{C_T U_T}{\kappa_n I_{tun0}} \frac{dW_1}{dt} = W_1^{1-\frac{U_T}{\kappa_n V_x}} \left(1 - W_1^{1+\frac{U_T}{\kappa_n (V_x || - V_{inj})}}\right),$$

$$\text{pFET}: \frac{C_T U_T}{\kappa_p I_{tun0}} \frac{dW_1}{dt} = W_1^{1+\frac{U_T}{\kappa_p V_x}} \left(W_1^{\alpha - \frac{U_T}{\kappa_p V_x}} - 1\right). \qquad (13)$$

As in the fixed channel-current case, these two equations are very similar. The trajectories of the nFET differential equation converge toward $W = 1$ and diverge away from $W = 0$, but the trajectories of the pFET differential equation converge toward $W = 0$ and diverge away from $W = 1$. We call the nFET circuit an autozeroing transconductance amplifier, because the output current always returns to the same equilibrium level.

III. Networks of Two Coupled Synapses

This section considers the interaction of two synapses coupled though their drain or source terminals. Figure 6 shows the circuits with two drain-coupled nFET synapses and with two drain-coupled pFET synapses. We consider only the stable circuit configurations, because it is difficult to illustrate the behavior of circuits that have no stable operating point. The nFET synapses are constrained by the cascode transistor. The two nFET synapses cooperate for the entire available channel current; regardless of the starting position, the two synapses converge to nearly equal channel currents. The pFET synapse channel currents are constrained by a current source, which we define to be the sum of the bias currents in each synapse. The two pFET synapses compete for the available bias current; the synapse starting with the larger channel current will eventually supply all the bias current. These properties extend directly to multiple synapses.

The output voltage (V_{out}) in both circuits returns to its equilibrium value. If we model each synapse by (8) or (9) and add the two equations for the two synapse weights (W_1 and W_2), we get equations which model the output voltage:

$$\text{nFET}: \frac{C_T + \kappa_n C_2}{\kappa_n I_{tun0}} \frac{dV_{out}}{dt} = B_1 - A e^{\frac{\Delta V_{out}}{V_{inj}}}.$$

$$\text{pFET}: \frac{C_2}{I_{tun0}} \frac{dV_{out}}{dt} = A e^{-\frac{\Delta V_{out}}{V_{inj}}} - B_2, \qquad (14)$$

where $A = W_1^{1+\alpha} + W_2^{1+\alpha}$, $B_1 = W_1^{1-\frac{U_T}{\kappa_p V_x}} + W_2^{1-\frac{U_T}{\kappa_p V_x}}$, and $B_2 = W_1^{1+\frac{U_T}{\kappa_p V_x}} + W_2^{1+\frac{U_T}{\kappa_p V_x}}$. A, B_1, and B_2 are always positive and weak functions functions of W_1, W_2; as a result both equations are qualitatively identical to the output-voltage equation of the AFGA. The ΔV_{out} trajectories converge to the circuit's steady state.

Once the output voltage has reached equilibrium, each synapse acts like its corresponding single-synapse circuit with a fixed drain voltage. For the coupled nFET circuit, Fig. 6c shows that, even if the two starting weights are orders of magnitude apart, then, over time, both weights will converge to nearly the same current. This behavior is typical of a continuous-time anti-Hebbian network. A nearly fixed drain voltage means that the synapses are only weakly coupled through the drain; we could achieve stronger coupling with a negative-resistance circuit. For the coupled pFET circuit, Fig. 6d shows that, if the two starting weights are equal, then, over time, one weight will decrease to 0 and the current in the other synapse will be equal to the bias current. If the losing weight is brought slightly above the winning weight, what was the losing synapse will now be the winner. The pFET synapses compete with each other for the bias current; in some sense, we have winner-take-all behavior in the weight space. This behavior is typical of a continuous-time normalizing Hebbian network; after a period of time, we cannot reuse these synapses without significantly altering this circuit.

Next, we describe two pFET synapses that are source-coupled. If the drain voltages are connected to a fixed potential, then the two pFET synapses will again compete for the available bias current. If the drain currents are contrained by current source transistors, as shown in Fig. 7a, then the drain voltages converge to a steady-state value. The circuit adapts the floating-gate charge such that nearly identical currents flow through each transistor in the differential pair; any mismatch is reflected in the results. For the floating-gate dynamics, we can model each leg of the differential pair having half of the total bias current, and therefore the weight of each floating-gate device would be fixed. For a fixed weight, both halves of the differential pair are described by identical equations that describe the AFGA configuration; therefore this circuit configuration

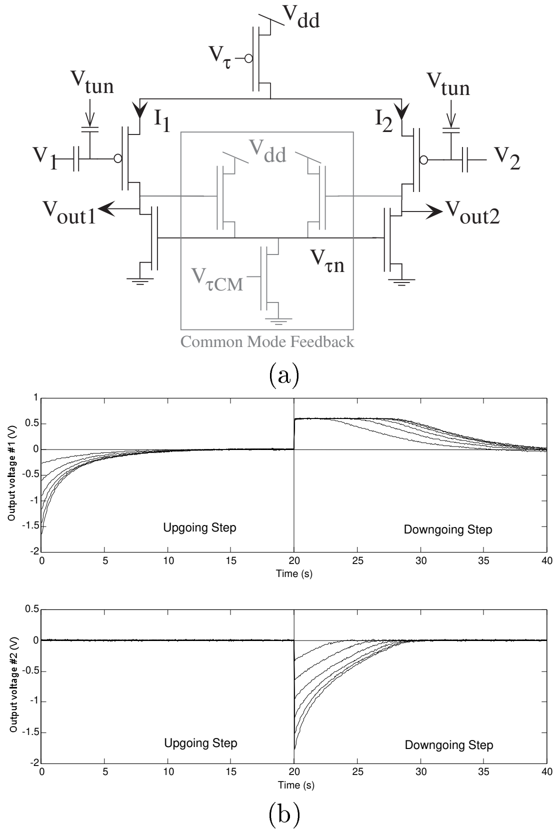


Fig. 7. Two source-coupled pFET synapses. (a) Circuit diagram of the two source-coupled pFET synapses constrained through a pFET current source. We use common-mode feedback circuit to set correct level for the nFET current source. The differential gain is limited by the ratio of input capacitance to floating-gate–to–drain capacitance, and the convergance time is dependent upon the tunneling current bias and the floating-gate–to–drain capacitance. (b) Experimental measurements of changes in the output voltages that show the stability of this circuit for several step changes in the input voltages. We applied upgoing and downgoing differential voltage steps to this circuit (2.4414mV 4.8828mV 7.3242mV 9.7656mV 12.207mV 14.648mV), and in each case the circuit returns to equilibrium. The nonlinear effects of the common-mode feedback circuit circuit is the source the asymetric step response. Even when the output voltage reaches the power-supply rails, the output voltages return to their equilibrium position. The common-mode gain was 0.0625, and the differential gain was 114. When we stop the adaptation, the circuit *remembers* the last converged state because of the differential structure; this circuit exhibited a 25mV input offset due to the mismatch in capacitive coupling when lowering voltages from adaptive range to normal operating range.

is stable. Further, if one output voltage goes to ground (and the other output voltage reaches its upper limit [6]), the *stronger* transistor will primarily tunnel back towards equilibrium, and the *weaker* transistor will primarily inject back towards equilibrium. Figure 7b shows experimental measurments illustrating the stablizing behavior two source-coupled pFET devices with their drain terminals constrained by current source transistors. We use a common-mode feedback bias circuitry (lighter drawing in Fig. 7a) to set our current sources to reasonable levels; the nFET part of the circuit is identical to a Winner-Take-All (WTA) circuit [9]. This circuit is useful for adapting offsets

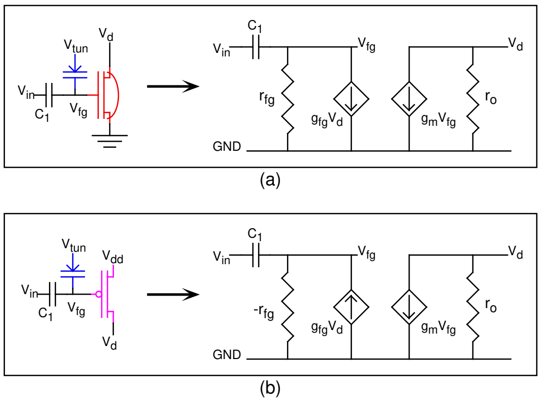


Fig. 8. (a) Circuit diagram and small-signal model of the nFET single-transistor synapse with its source connected to ground. The small-signal model assumes a constant tunneling current and that the parameters are positive. (b) Circuit diagram and small-signal model of the pFET single-transistor synapse with its source connected to V_{dd}. The small-signal model assumes a constant tunneling current and that the parameters are positive. The small-signal resistance from floating-gate to ground is negative due to the hot-electron injection currents.

in differential-pairs, as well as adapting bump-circuits [10] for use in adaptive radial-basis function networks [11].

IV. Using Small-Signal Analysis to Determine Stability of Adaptive Floating-Gate Circuits

When analyzing nonlinear dynamical systems, it is often valuable to look at the linearized form of the model. In systems of ordinary differential equations, stability is determined by the Jacobian of these equations [13]. In analyzing circuits, we use small-signal models, an analogous tool that allows graphical analysis of the dynamical system. To analyze the stability of floating-gate circuits, we want to develop a small-signal model of these floating-gate transistors, and show that the results are consistant with large-signal analysis and experimental results. We will demonstate the value of this technique analyzing previous examples: the single pFET floating-gate circuits, and the two-coupled pFET floating-gate circuit.

A. Developing the Floating-Gate FET model

Figure 8 shows small-signal models of the nFET and pFET synapses, where all the small-signal parameters are positively valued. We will extend the conventional MOSFET small-signal model [12] to include hot-electron injection and electron tunneling effects. A typical small-signal model of a subthreshold nFET or pFET would be characterized by its transconductance, g_m, output resistance, r_o, and by an open circuit to the gate terminal. For a subthreshold MOSFET, $g_m = \kappa I_{so}/U_T$, and $r_o = V_o/I_{so}$. The transistor's maximum voltage gain, $A_v = g_m r_o$.

What is not so typical is to define an input gate resistance, r_{fg}, and a transconductance connected to the floating gate, g_{fg}. We define g_{fg} as the change in the gate current in response to a change in drain voltage. Because

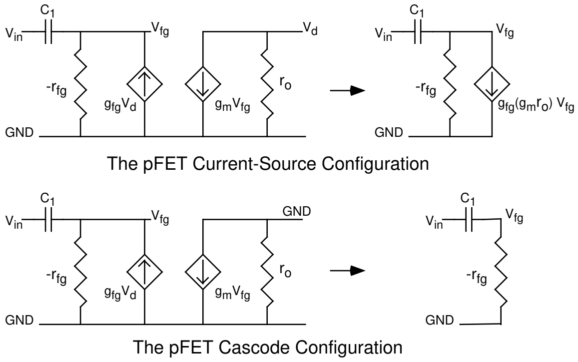


Fig. 9. Simplification of small-signal models for the pFET single-transistor circuits; the nFET synapse circuits are simplified similarly. The top figure shows the simplified small-signal model for the drain connected to a cascode transistor. The bottom figure shows the simplified small-signal model for the drain connected to a current source. This circuit is unstable because of the negative resistance from floating-gate to ground.

only the injection current depends on the drain voltage, $g_{fg} = \frac{I_{tun0}}{V_{inj}}$ for the nFET and pFET pictured in Fig. 8. We define r_{fg} as the magnitude of the change in gate current for a change in gate voltage; r_{fg} is equal to $\frac{U_T/\kappa_p || V_x}{I_{tun0}}$ for nFETs and is equal to $\frac{U_T/\kappa_p || -V_x}{I_{tun0}}$ for pFETs, where we define $x||y$ as $\frac{xy}{x+y}$. The resistance from the floating gate to ground is negative for a pFET.

B. Analysis of adaptive circuits using one floating-gate FET

Using a fixed channel current is equivalent to open-circuiting the drain terminal in the synapse's small-signal model; therefore, the effective conductance from floating gate to ground is

$$\text{nFET} : r_{fg} - (g_m r_o)\, g_{fg},$$

$$\text{pFET} : (g_m r_o)\, g_{fg} - r_{fg}. \tag{15}$$

Since this effective conductance is positive for pFET synapses, the configuration in Fig. 5c is stable. On the other hand, since this effective conductance is negative for nFET synapses, the configuration in Fig. 5a is unstable.

When the drain voltage is fixed, the sign of r_{fg} determines the stability of this circuit; the configuration in Fig. 5d is unstable due to the negative r_{fg} for pFET synapses, whereas the configuration in Fig. 5b is stable due to the positive r_{fg} for nFET synapses. For both the pFET and nFET synapses, a particular load resistance, R_l, connected to the drain, where $R_l g_m (g_{fg} r_{fg}) = 1$, results in zero effective conductance between the floating gate and ground and is the boundary between the stable and unstable regimes. Because this formulation is valid for positive and negative resistances, negative drain resistance is stablizing for nFETs and destabilizing for pFETs.

C. Analysis of the two coupled pFET system

We will next use these small signal models to analyze the two drain-coupled pFET circuit in Fig. 6. For the multi-synapse case, we have a saddle point such that only one element converges to a solution with the other synapses all diverging away towards zero. Figure 10a shows the small-signal analysis of this two floating-gate pFET circuit around the bias point where $W_1 = W_2$ ($V_{fg1} = V_{fg2}$. From the reduced circuit, we can write down the model equations

$$r_1 C \frac{dV_{fg1}}{dt} - \frac{r_1}{r_{fg}} V_{fg1} + V_{fg1} + V_{fg2} = 0,$$
$$r_1 C \frac{dV_{fg2}}{dt} - \frac{r_1}{r_{fg}} V_{fg2} + V_{fg1} + V_{fg2} = 0. \qquad (16)$$

By adding these two equations, we get

$$r_1 C \frac{d(V_{fg1} + V_{fg2})}{dt} + \left(2 - \frac{r_1}{r_{fg}}\right)(V_{fg1} + V_{fg2}) = 0. \quad (17)$$

This equation converges to zero with the timeconstant $r_1 C/(2 - \frac{r_1}{r_{fg}}$. This equation models the convergance of the drain voltage, because in this small-signal model, $V_d = A_v(V_{fg1} + V_{fg2})$, and follows the experimental results in Fig. 6. This result is not unexpected, because to first-order, $A = 2^{-\alpha}$, and $B_2 = 2^{U_T/\kappa V_x}$ in (14).

The second model equation shows that one weight diverges towards zero. By subtracting these two equations in (16), we get

$$r_{fg} C \frac{d(V_{fg1} - V_{fg2})}{dt} - (V_{fg1} - V_{fg2}) = 0 \qquad (18)$$

The difference in voltages increases without bound, and with a time constant of $r_{fg}C$. The difference gets large as a result, one floating-gate voltage converges to a stable point, and the other floating-gate voltage increases without bound. One weight converges to 1, and the other weight converges to 0. The result is one positive and one negative eigenvalue; therefore we have a saddle-node equilibrium point. A saddle point means that a value along a first eigenvector will converge to a single value, while a value along a second eigenvector will diverge away from its steady state value; this type of equilibrium value is unstable. Figure 10b shows the phase plane for the orignal system, and follows the experimental results in Fig. 6. Since $r_{fg}C$ is typically a factor hundreds smaller than $r_1 C$ (factor $= g_{fg} r_{fg} g_m r_o$), therefore $W_1 + W_2$ will converge far before the weights diverge. We see difference in timeconstants because the trajectories first move toward $W_1 + W_2$ eigenvector, and then away from $W_1 - W_2$ eigenvector towards either $(W_1, W_2) = (0,1)$ and $(W_1, W_2) = (1,0)$.

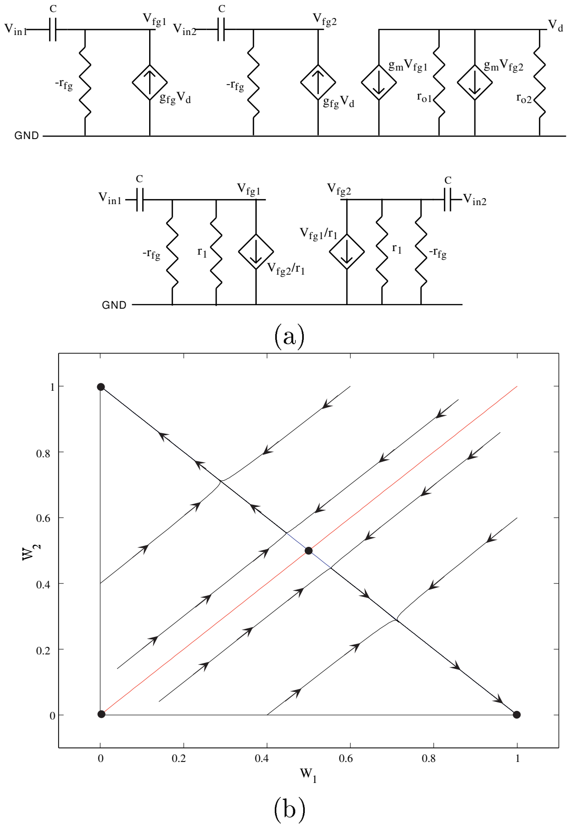


Fig. 10. Small-signal analysis of the two floating-gate pFET circuit. We first show the equivalent small-signal circuit for the pFET circuit in Fig. 6 expanded around the condition where both pFETs have equal current. We then reduce this circuit to show the dependence on V_{fg1}, V_{fg2}. This small-signal circuit exhibits a saddle-node equilibrium point. Finally, we show the resulting phase-plane for the circuit in Fig. 6, showing the saddle-node point for $(W_1, W_2) = (1/2, 1/2)$, as well as two stable points at $(W_1, W_2) = (0,1)$ and $(W_1, W_2) = (1,0)$.

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Dr. Paul Hasler's biography is on page 42 of this issue.