A Second-Order Section built from Autozeroing Floating-Gate Amplifiers

Paul Hasler, Theron Stanford, and Bradley A. Minch

Abstract— **We introduce the Autozeroing Floating-Gate Second-Order Section. We built this second-order filter where the corner frequency and Q are electronically tunable based on a classic filter topology and principles of OTA amplifiers. We built this second-order filter using three AFGAs— our floating-gate amplifier that sets its operating point by the interaction of hot-electron injection and electron-tunneling.**

We introduce the *Autozeroing Second-Order Section* (AutoSOS) in this paper, based upon our earlier work [1-4] The second-order section is the primary element to build higher-order filters, both in continuous-time and switch-capacitor circuits. Figure 1 shows the autozeroing second-order section. This circuit is based on the Diff2 second-order section [5], which in turn is based on a canonical form for a second-order section as a high-gain amplifier with feedback. This circuit uses the autozeroing floating-gate amplifier (AFGA) that we invented previously [1], [2], [3]. The AFGA does not require any clocking to eliminate offsets, as in switched-capacitor circuits [6], but utilizes an inherent combination of electron-tunneling and hot-electron–injection currents to eliminate the DC signal.

This paper illustrates how to build higher-order filters from AFGAs, as well as proving the feasibility of circuits with multiple floating-gate devices. Using AFGAs as the core filter block merges many of the benefits of switched-capacitor [6], and transconductance-amplifier or OTA [5] filters. The AFGA-based filters can tuned electronically the corner frequencies over many orders of magnitude, as in transconductance-amplifiers. Because many of the AFGA's circuit properties—bandpass gain, linear range, and dynamic range—are set by ratios of capacitors, the AFGA-based filters utilize capacitor matching as is done in switched-capacitor filters. Also, the AFGA filters its offsets, $1/f$ noise without resorting to the chopper-stabilizing clocking schemes present in switched-capacitor [6] filters.

We present data from circuits fabricated in a $2\mu m$ n-well Orbit CMOS process available through MOSIS. Typical operating values for V_{tun} were between $33V$ to $42V$; those for V_{dd} were $6V$ to $12V$. We obtain similar data in the $1.2\mu m$ n-well Orbit CMOS process, but with typical operating values for V_{tun} between $26V$ and $31V$. For processes with smaller line widths, the typical operating voltages will decrease due to the thinner gate oxide and higher substrate doping.

I. Autozeroing Floating-Gate Amplifier

Figure 2 shows the AFGA. The AFGA has four operating regimes that behave similarly for above and below threshold biases. The transfer function of the AFGA is a bandpass with widely separated timeconstants, as seen in Fig. 2b. Although we could analyze the complete problem, as in [2], we will analyze the high- and low-frequency corner frequencies independently, as is justified by the AFGA data in Fig. 2b. For an equivalent all-transistor implementation, say built from capacitively coupled current conveyers (C^4), this wide separation of timescales is not always a good assumption [7], [8]; when the timeconstants overlap, one already has interesting second-order behavior.

Dr. Hasler is with the School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA 30332-0250, phasler@ee.gatech.edu.

Mr. Stanford is with the Department of Electrical Engineering, California Institute of Technology, Pasadena, CA, 91125.

Dr. Minch is with the Department of Electrical Engineering, Cornell University, Ithica, NY.

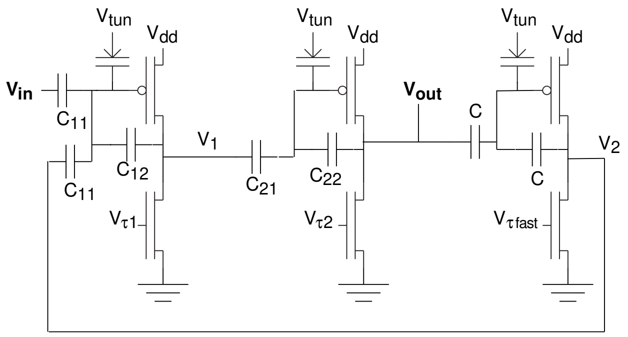


Fig. 1. Circuit diagram of the autozeroing second-order section. This circuit, which is built with three autozeroing amplifiers, shows second-order behavior that is electronically controlled.

First, the adaptation region of the AFGA is a high-pass filter at low frequencies, which is set by the tunneling and injection currents. The complementary combination of tunneling and hot-electron injection adjusts the floating-gate charge in such a way that the amplifier's output voltage returns to its steady-state value on a slow time scale. We show elsewhere that the low-frequency AFGA behavior is described by [1], [2]

$$C_2 \frac{dV_{out}}{dt} = -C_1 \frac{dV_{in}}{dt} + I_{tun0} \left(\exp\left(-\frac{\Delta V_{out}}{V_{inj}} \right) - 1 \right). \quad (1)$$

We derive the frequency response by keeping only the linear terms when we expand the exponentials and taking the Laplace transform:

$$\frac{V_{out}(s)}{V_{in}(s)} = -\frac{C_1}{C_2} \frac{s\tau_l}{1+s\tau_l}, \quad (2)$$

where τ_l is $C_2 V_{inj} \ / \ I_{tun0}$. The difference between the tunneling voltage and the pFET's floating gate voltage sets the equilibrium tunneling current, I_{tun0}, and sets the resulting corner frequency.

Second, the integrating region of the AFGA is a low-pass filter at high frequencies, which is set by the nFET bias current. We show elsewhere that the high-frequency AFGA behavior is described by [2] which we write as

$$\left(C_T C_o - C_2^2\right) \frac{dV_{fg}}{dt} = C_1 C_o \frac{dV_{in}}{dt} + C_2 I_\tau \left(e^{-\frac{\kappa \Delta V_{fg}}{U_T}} - 1 \right). \quad (3)$$

where C_T is the total capacitance connected to the floating gate ($C_T = C_1 + C_2 + C_w$), and C_o is the total capacitance connected to the output node ($C_o = C_2 + C_L$). For small signals, we linearize (3) by expanding the exponentials for the resulting simplified equation:

$$\left(C_T C_o - C_2^2\right) \frac{dV_{fg}}{dt} = C_1 C_o \frac{dV_{in}}{dt} - \frac{\kappa C_2 I_\tau}{U_T} \Delta V_{fg}. \quad (4)$$

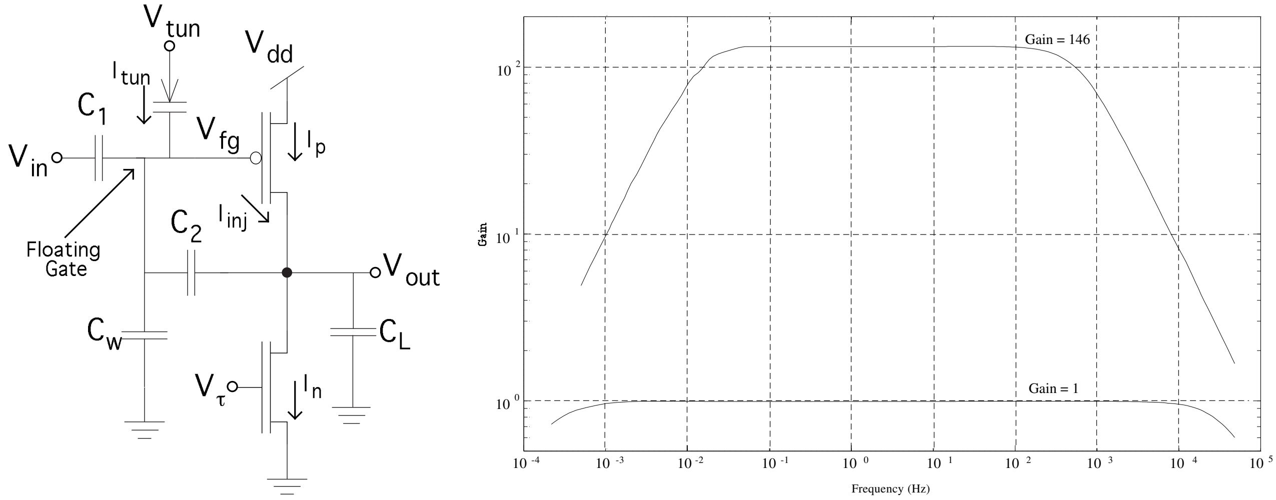
Again, we derive the frequency response by taking the Laplace transform:

$$\frac{V_{out}}{V_{in}} = -\frac{C_1}{C_2} \frac{1 - A_h \tau_h s}{1 + \tau_h s}, \quad (5)$$

where we define

$$\tau_h = \frac{\left(C_T C_o - C_2^2\right) U_T}{\kappa C_2 I_\tau}, \quad A_h = \frac{C_1 C_2}{C_T C_o - C_2^2}. \quad (6)$$

The gain from input to output due to capacitive feedthrough is A_h. This transfer function includes the effects of parasitic



(a) (b)

Fig. 2. The autozeroing amplifier that uses the hot-electron injecting pFET. (a) Circuit of The ratio of C_2 to C_1 sets the gain of this inverting amplifier. The nFET is a current source, and it sets the current through the pFET. Steady state occurs when the injection current (I_{inj}) is equal to the tunneling current (I_{tun}). The capacitance from the floating gate to ground, C_w, represents both the parasitic and the explicitly drawn capacitances. Increasing C_w will increase the linear input range of the circuit. The capacitance connected to the output terminal, C_L, is the load capacitance associated with driving other amplifiers. (b) Frequency response for two AFGAs with different gains. For both the high- and low-gain AFGA, $C_1 + C_2$ is approximately constant. For the high-gain AFGA, τ_l is 20mHz, and τ_h is 600Hz; for the low-gain AFGA, τ_l is 300μHz and τ_h is 40kHz. The ratio of τ_h and τ_l between the two AFGAs are equal to one-half of the ratio of the gains; the ratio is consistent with a constant $C_1 + C_2$.

and load capacitances. The nFET current source sets the bias current and sets the resulting corner frequency.

Third, the amplifier region of the AFGA is between the adaptation and integration regimes. With capacitive feedback, the input signal is amplified by a closed-loop gain approximately equal to $-\frac{C_1}{C_2}$. Fourth, the capacitive feedthrough region occurs at much higher frequencies than the integrating regime, which can be reduced by increasing either C_w or C_L.

The AFGA is always a first order system even in the presence of parasitic capacitances; therefore, the AFGA is always stable with 90 degrees of phase margin for non-inductive loads. Figure 2b shows the frequency response from typical high-gain and unity-gain AFGAs. Any amplifier with resistive feedback is at least a second-order system, but amplifiers with capacitive feedback can be a first-order system. For moderate adaptation rates, the low-frequency time constant remains nearly constant, and any shift is primarily due to trapping in the tunneling oxide.

The AFGA's noise performance is similar in thermal and 1/f noise characteristics to a standard MOS amplifier; the tunneling and injection processes do not add appreciable noise to the amplifier. In addition, the adaptation in the AFGA filters the low frequency noise in the AFGA, an effect which can not be obtained in a simple amplifier with a blocking capacitor at the input We can increase the linear range by increasing C_w, and we can increase the dynamic range by increasing either C_w and/or C_L [2].

II. Autozeroing Second-Order Section

Figure 1 shows the autozeroing second-order section. We will analyze this circuit at both the high- and low-frequency regions of operation. To build a simplified model of the second-order behavior, we assume that $V_2 = -V_{out}$; that is, $V_{\tau fast}$ is set at a bias current much larger than $V_{\tau 1}$ or $V_{\tau 2}$. By modifying $V_{\tau fast}$, one can achieve a third-order circuit. Similar results are found when using a C^4 based circuit [7] for each AFGA filter.

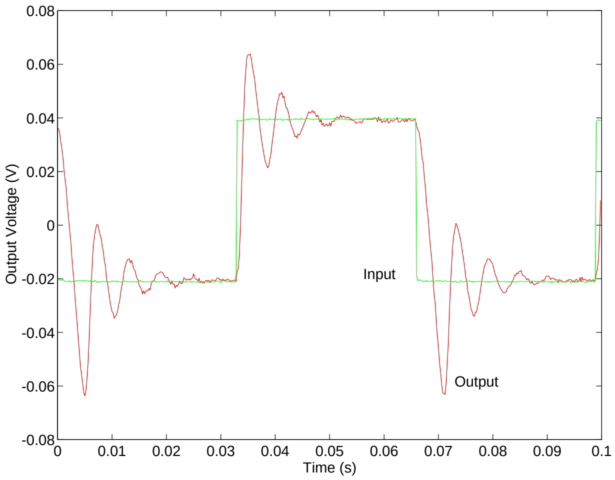


Fig. 3. Response of the autozeroing second-order section due to upgoing and downgoing input steps over a short timescale. The ringing of the output voltage is characteristic of a second-order system.

First, we consider this circuits operation due to the high-frequency operation of its AFGA circuits. We ignore (for the moment) the floating-gate currents, ignore the capacitive feedthrough effects, and assume the $V_{\tau 1}$ amplifier's gain is very large. From the AFGA analysis in the previous section, the small-signal model of the two amplifiers based upon (4) is

$$\frac{C_{T1}C_{o1} - C_{12}^2}{C_{12}} \frac{U_T}{\kappa I_{\tau 1}} \frac{dV_1}{dt} = (V_{in} + V_2), \quad (7)$$

$$\frac{C_{T2}C_{o2} - C_{22}^2}{C_{22}} \frac{U_T}{\kappa I_{\tau 2}} \frac{dV_{out}}{dt} = (V_1 + V_{out}), \quad (8)$$

where C_{T1}, C_{T2} are the total capacitances connected to each

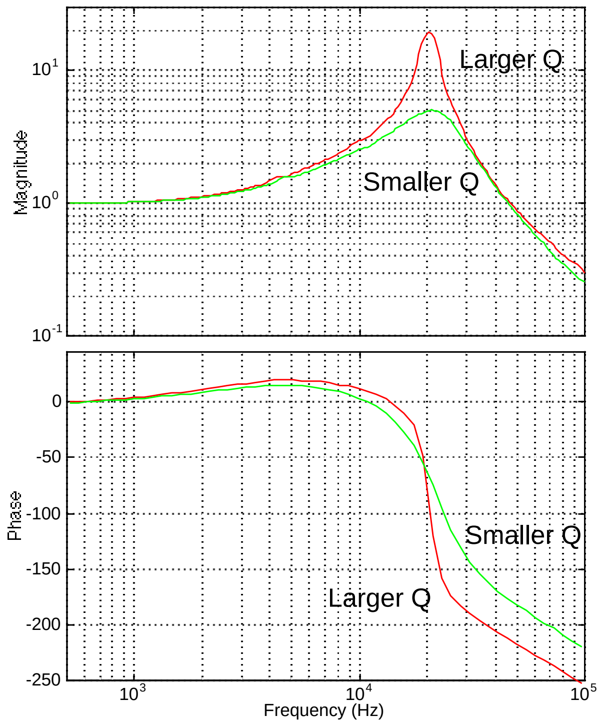


Fig. 4. Frequency response of an AutoSOS for two different bias current settings. The Larger Q case is for $V_{\tau 1} = 0.717$V and $V_{\tau 2} = 0.597$V, and the Smaller Q case is for $V_{\tau 1} = 0.677$V and $V_{\tau 2} = 0.637$V. In both cases, we changed the bias current from the model of τ and Q such that the τ of the circuit would remain constant. The effect of capacitive feedthrough for the amplifiers associated with $V_{\tau 1}$ and V_{tau2} only starts to appear at the high-frequency end of this data.

floating gate including capacitors not drawn in Fig. 1, C_{o1}, C_{o2} are the total capacitances connected to each output node including capacitors not drawn in Fig. 1, and C_{12}, C_{22} are the feedback capacitors from floating gate to output. By defining

$$\tau_1 = \frac{C_{T1}C_{o1} - C_{21}^2}{C_{12}} \frac{U_T}{\kappa I_{\tau 1}}, \text{and } \tau_2 = \frac{C_{T2}C_{o2} - C_{22}^2}{C_{22}} \frac{U_T}{\kappa I_{\tau 2}}, \quad (9)$$

we solve for the transfer function from V_{in} to V_{out} as

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{1}{1 + s\tau_1 + s^2 \tau_1 \tau_2}. \quad (10)$$

From the canonical form for the second-order section, we find that [5]

$$\tau = \sqrt{\tau_1 \tau_2}, \text{and } Q = \sqrt{\tau_1 / \tau_2}. \quad (11)$$

Figure 3 shows the step response of this autozeroing second-order section. The data show the characteristic ringing behavior of a second-order system; changing $V_{\tau 1}$ and $V_{\tau 2}$ changes τ and Q, as predicted from (11).

Figure 4 illustrates how the frequency response changes by electronically changing the τ_1 and τ_2 values in an AutoSOS; Fig. 4 shows the frequency response for two different values of τ_1 and τ_2. We tuned these values such that the product of $\tau_1 \tau_2$, and therefore τ, remained constant. In these curves, one sees an initial 20dB/decade increase just before the Q peak in both responses due to the cutoff frequency of the third amplifier, and this effect increases the amplitude at the Q peak. This response is typical of the V_1 node in an ideal second-order section. The capacitive feedthrough in the third amplifier limits the bandwidth of this effect. The high-frequency phase lag greater than

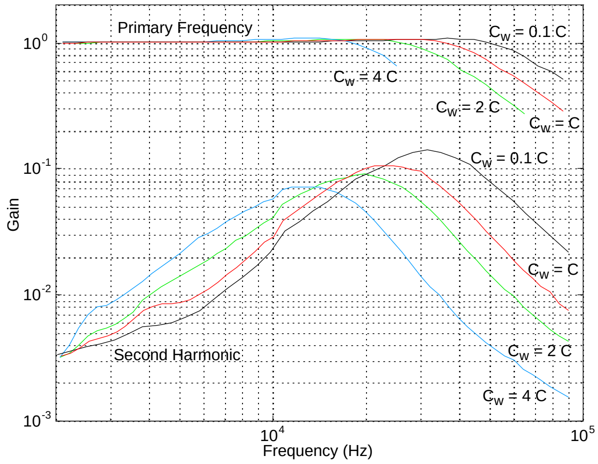


Fig. 5. Frequency response of the first and second harmonic components of AutoSOSs for four different values of C_w in all three AFGAs. C_w is the capacitance from floating gate to V_{dd} and therefore increases the overall value of C_T. Also, $C_{11} = C_{21} = C_{22}$ remained constant for all measurements. The AutoSOS was biased to have a Q slightly greater than 1. The input amplitude was much larger than the second AFGA's linear range. We see that increasing C_w linearly increases τ, but linearly decreases the peak second-harmonic response.

180 degrees occurs because we are using three amplifiers to build a second-order system.

Figure 5 shows the frequency response of the first and second harmonics from identical AutoSOSs except with different drawn sizes of C_w (C_w is the capacitance from floating gate to V_{dd}) in all three AFGAs while keeping all other capacitances constant. The second harmonic dominates the distortion of the AFGAs because our nonlinearities arise from subtracting exponential functions from constants, and therefore the distortion of the AutoSOS. The maximum second-harmonic distortion is nearly at half of the section's corner frequency. Increasing C_w has three effects:

1. τ decreases linearly with increasing C_w (which increases C_T),
2. The capacitive feedthrough from input to output decreases, and
3. Second-harmonic distortion decreases linearly with increasing C_w, because the signal level at the floating-gate is decreased by the resulting capacitive voltage divider.

Therefore, as in the AFGAs [2], the AutoSOS's linear range and dynamic range increases linearly and peak distortion decreases linearly with increasing C_w.

III. Low-Frequency Time-Response Behavior

The AFGA also has a high-pass cutoff at low frequencies; therefore coupling three of these stages with negative feedback may also produce second or third order behavior at low frequencies. Using small signal models, we can write three equations for the three AFGAs around the low-frequency corners as (assume for clarity $C = C_{11} = C_{21} = C_{22}$)

$$\frac{dV_2}{dt} = -\frac{dV_{in}}{dt} - \frac{I_{tun01}}{V_{inj}C}\Delta V_1$$

$$\frac{dV_1}{dt} = -\frac{dV_{out}}{dt} - \frac{I_{tun02}}{V_{inj}C}\Delta V_{out}$$

$$\frac{dV_2}{dt} = -\frac{dV_{out}}{dt} - \frac{I_{tun03}}{V_{inj}C}\Delta V_2 \quad (12)$$

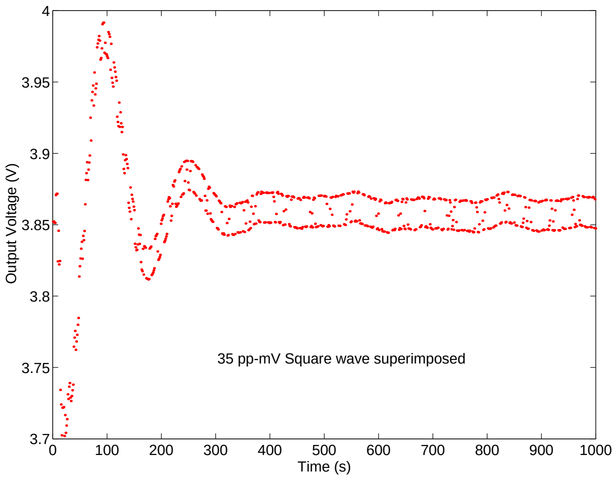


Fig. 6. Response of the autozeroing second-order section due to an upgoing input steps over a long timescale. A 1Hz square wave was superimposed on the input signal, and is preserved throughout the relaxation. This ringing behavior proves that the circuit exhibits at least second-order behavior from the AFGA corner frequencies set by the floating-gate currents.

where the equilibrium tunneling currents, $I_{tun01}, I_{tun02}, I_{tun03}$, are set by difference between their respective tunneling and pFET's floating-gate voltages, and for clarity, C_{12} is assumed negligible for this analysis. We have ignored the passband regime for the first amplifier, because it has a small effect on the low-frequency dynamics, as was true for deriving the high-frequency dynamics. Laplace transforming these equations, we solve the coupled equations for the following resulting V_2 equation:

$$V_2 = -\frac{V_{in}}{1 + \frac{I_{tun01}}{sCV_{inj}} + \frac{I_{tun01}(I_{tun02}+I_{tun03})}{s^2C^2V_{inj}^2} + O(3)}. \tag{13}$$

By comparing this equation to the low-frequency equivalent of a second-order section:

$$\frac{V_2(s)}{V_{in}(s)} = \frac{1}{1 + \frac{1}{Qs\tau} + \frac{1}{s^2\tau^2}}. \tag{14}$$

we get an effective τ and Q as

$$\tau = \frac{CV_{inj}}{sqrttun01(I_{tun02} + I_{tun03})} \text{and } Q = \sqrt{\frac{I_{tun02} + I_{tun03}}{I_{tun01}}} \tag{15}$$

Figure 6 shows the step response at a very slow timescale. The damped oscillatory behavior is due to the corner frequencies set by the tunneling currents, and is indicative of at least a second-order circuit. The low-frequency filtering in this circuit provides the basis for the design of integrated filters operating at very low frequencies less than 10Hz to frequencies below 1μHz.

IV. Acknowledgments

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