AN AUTOZEROING FLOATING-GATE AMPLIFIER WITH GAIN ADAPTATION

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ABSTRACT

Recently, we have characterized and modeled floating-gate circuits that adapt their floating-gate charge based upon statistics of the incoming signal. In this paper, we show signal-dependant adaptation in three floating-gate circuits. First, we show classic autozeroing floating-gate amplifer (AFGA) measurements of output voltage adaptation, as well as AFGA measurements of offset adaptation for large output amplitudes. Second, we measure and characterize current adaptation of a transcondutance element, where the current increases for increasing signal level. Third, we measure and characterize the amplitude and offset adaptation in a floating-gate circuit built from the first two circuits; amplitude adaptation only occurs over a finite range of input parameters and timescales.

Floating-gate circuits using continuous tunneling and injection naturally adapt the floating-gate charge in response to various applied input signals. Our previous investiagations have shown basic adapting circuits, like the autozeroing floating-gate amplifier (AFGA), that adapt away a single feature of an incoming signal [1]. Recently, we have characterized and modeled floating-gate circuits that adapt their floating-gate charge based upon statistics of the incoming signal [2]. This result is the first indication that floating-gate devices with continuous tunneling and hot-electron injection currents are capable of large-scale adaptation. This paper continues this work by showing signal-based adaptation in three floating-gate circuits. In the third circuit, we show amplitude adaptation over a finite range of input parameters and timescales.

1. ADAPTIVE FLOATING-GATE CIRCUITS

In this section, we will consider the behavior of the two continuously adapting floating-gate circuits shown in Fig. 1. These two circuits are the two key pieces making up the AFGA with gain adaptation. In the interest of clarity, our experiments and modeling will only focus on the low-frequency and passband responses, ignoring the high-frequency dynamics.

1.1. Autozeroing Floating-Gate Amplifier

We begin our examination of adaptive floating-gate pFET circuits by examining the autozeroing floating-gate amplifier (AFGA) which appears in Fig. 1a. The AFGA

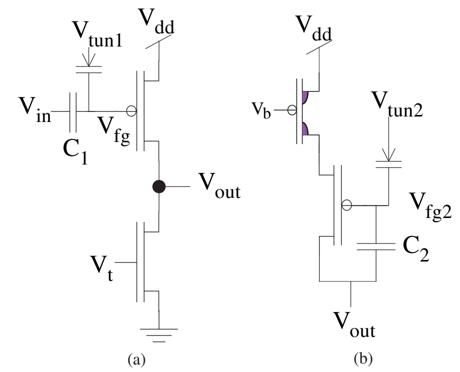

Figure 1: The two fundamental floating-gate circuit elements comprising the gain-adapting AFGA; this circuit will connect the two V_{out} nodes. For both circuit elements, steady state occurs when the injection current equals the tunneling current. (a) The autozeroing floating-gate amplifier (AFGA). (b) A source-degenerated (s-d) floating-gate pFET; the steady-state current converges back to its equilibrium level over long-timescales.

is the simplest example of an adaptive floating-gate pFET circuit. The AFGA uses tunneling and pFET hot-electron injection to adaptively set its DC operating point. The complementary tunneling and hot-electron injection processes adjust the floating-gate charge such that the amplifier's output voltage returns to a steady-state value on a slow time scale. The modulation of the pFET hot-electron injection by the output voltage provides the correct feedback to return the output voltage to the proper operating regime. The AFGA achieves a high-pass characteristic at frequencies well below 1Hz.

Figure 2 shows the response of the autozeroing floating-gate amplifier to a 1Hz sine wave superimposed on an input pulse. If the input changes on a timescale that is much shorter than the adaptation, then the output is an amplified version of the input signal. The amplifier adapts to the pulse input after an initial transient, while preserving the amplified 1Hz sine wave.

1.2. Mathematical Modeling

To model floating-gate devices employing electron tunneling and hot-electron injection, we must model the behavior of the circuits in Fig. 1 at two timescales. This analysis is

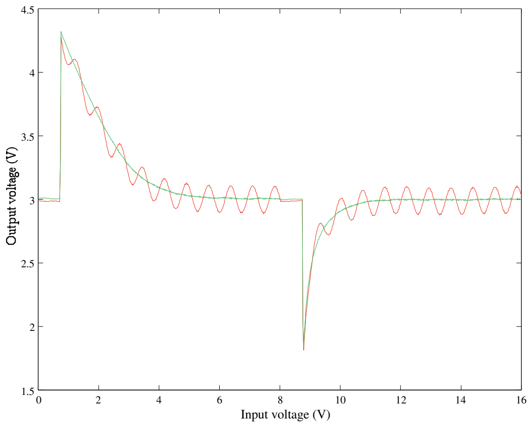

Figure 2: Response of the AFGA to two inputs: first, a volage pulse, and second, an 1Hz sinewave superimposed on an identical voltage pulse. The AFGA gain was approximately 40; the gain was limited by the floating-gate–to–drain capacitance. The 1Hz signal is amplified, but the much slower step is adapted away.

based on our general analysis of floating-gate devices that use continuous electron-tunneling and hot-electron injection currents [1, 2]. We will ignore the fast time-scale response due to bias current and load capacitor limitations. Further, we will consider circuits where we have fixed the tunneling voltage terminal to a constant bias voltage; additional dynamics are available when modifying the tunneling voltage.

In general, the governing equation for a circuit using continuous floating-gate currents originates by equating currents at the floating-gate node. The tunneling and injection currents in the device are small compared with the transistor bias current; therefore, changes in floating-gate charge occur on a much slower timescale than synapse computations. These two time scales allow us to define separate terminal voltages representing slow and fast timescale voltage changes. The fast-timescale variables represent the rapid changes due to the input signals; the slow-timescale variables represent the changes due to floating-gate charge. We express the output voltage as a sum of variables that represent the fast and slow timescales; that is,

$$\Delta V_{out} = \Delta\hat{V}_{out} + \Delta\bar{V}_{out}, \text{ and } \Delta V_{fg} = \Delta\bar{V}_{fg} + \Delta\hat{V}_{fg} \quad (1)$$

where $\Delta\hat{V}_{out}$ represents the fast-timescale behavior and $\Delta\bar{V}_{out}$ represents the slow-timescale behavior. We will assume that the input voltage(s) are zero mean, that is, they only have fast-timescale components.

The seperation of timescales allows us to seperate the floating-gate current equation into two equations: one modeling the fast dynamics and one modeling the slow dynamics. At fast timescales, we approximate the tunneling and injection currents to be negligible. With this formulation, we can integrate over many periods at the fast timescale, but still make only a small change in the slow-timescale output voltage. We assume that the input signals are ergodic so that we can use time averages for the expected value. Thus we shall define $E[\cdot]$ as the average of a time-varying signal, $x(t)$, over a time interval, T, that is much shorter than the slow timescale, but much longer than one period at the fast timescale:

$$E[x(t)] = \frac{1}{T}\int_0^T x(t)dt. \quad (2)$$

The result of this integration is an equation describing the slow timescale behavior.

For the AFGA circuit in Fig. 1a, we will derive the response assuming a fixed floating-gate voltage because we have an ideal high-gain amplifier between V_{fg} and V_{out}. At fast timescales, the change in the output voltage is described by $\Delta\hat{V}_{out} = -(C_1/C_f)\Delta V_{in}$, where C_f is the capacitance between floating-gate–and drain; the minimum capacitance is the overlap capacitance of the pFET transistor. At slow timescales, we previously showed that the equation is [3]

$$C_f\frac{d\bar{V}_{out}}{dt} = I_{tun0}\left(E\left[e^{-\frac{\Delta V_{out}}{V_{inj}}}\right] - 1\right). \quad (3)$$

where $I_{fg0}\exp(\Delta V_{out}/V_{inj})$ represents the floating-gate current due to hot-electron injection, and $-I_{fg0}$ represents the floating-gate current due to electron tunneling. V_{inj} is a drain-voltage dependent hot-electron injection device parameter [1].

Figure 1b shows the two pFET transistor circuit for the source-degenerated (s-d) floating-gate pFET. We want to derive the behavior of the channel current in response to various signals applied to V_{out}. The s-d floating-gate pFET has the unique property of converging to a stable equilibruim point if either the channel current or the drain voltage is the one free parameter [1, 2]; basic nFET and pFET floating-gate devices will converge for one of these situations but not both. The transistor between V_{dd} and the source terminal of the floating-gate pFET is a short-channel pFET with significant drain-induced barrier lowering (DIBL). The DIBL pFET introduces sufficent negative feedback by using source degeneration to achieve the stable dynamics. The resulting dependence of subthreshold channel current, I_s, around a given bias current, I_{s0}, due to a change in the floating-gate voltage, ΔV_{fg}, for the circuit in Fig. 1b is

$$I_s = I_{s0}e^{-\kappa_x\kappa\Delta V_{fg}/U_T} \quad (4)$$

where κ_x is a parameter that characterizes the sharpness of the exponential relationship of the source degenerative feedback element, κ is the coupling between the gate voltage and channel potential, and U_T is the thermal voltage.

We consider fast-timescale variables as representing the computational signals of the synapse. The pFET channel current depends upon a multiplication of the gate terminal voltage and an exponential function of the floating-gate charge, which we call the weight. Since we decomposed ΔV_{fg} into fast and slow components, applying this to (4), we get

$$I_s = I_{s0}we^{-\kappa_p\kappa_x\Delta\hat{V}_{fg}/U_T},$$
$$w = e^{-\kappa_x\kappa_p\Delta\bar{V}_{fg}/U_T}. \quad (5)$$

where the weight, w, is due to the slow-timescale floating-gate voltage. The weight is proportional to the average current at the source.

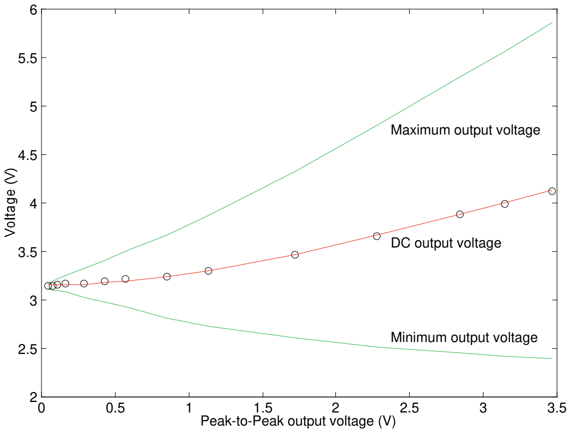

Figure 3: Minimum and maximum output voltages versus the peak-to-peak output-voltage amplitude. The frequency of the input sine wave was 100Hz; the AFGA had a gain of 146. For small input amplitudes, the minimum and maximum output voltages symmetrically deviate from the steady-state voltage; for large input amplitudes, however, the DC output voltage follows the maximum output voltage. The DC voltage was fit to (11) with $V_{inj} = 500\text{mV}$.

The slow-timescale floating-gate node voltage equation gives us the starting point for developing the weight dynamics of the synapse. The slow-timescale equation is

$$C_T \frac{d\Delta \bar{V}_{fg}}{dt} = I_{tun} - I_{inj}. \quad (6)$$

where C_T is the total capacitance connected to this floating-gate (V_{fg2}). Based on our previous tunneling-injection modeling [1], we model the difference of tunneling and injection current as

$$I_{tun} - I_{inj} = I_{fg0}\left(w^{\gamma-1} e^{(1/V_{g0} - 1/V_{inj})\Delta V_{out}} - w^{\beta-1} e^{-\Delta V_{out}/V_{g1}}\right) \quad (7)$$

where $\beta = 1 + \frac{U_T}{\kappa_x \kappa_p V_x}$, $V_{g1} = (C_T/C_2)V_x$, V_x is dependent on the bias values of tunneling voltage and floating-gate voltage, and device parameters, $V_{g0} = \frac{U_T C_T}{\kappa_p (U_T/V_{inj} - \kappa_x \alpha) C_2}$, $\gamma = 1 + \kappa_p(U_T/V_{inj} - \kappa_x \alpha)$. In equilibrium, that is at the bias point, the tunneling and injection currents are equal to this bias current; in other words, $I_{fg0} = I_{inj} = I_{tun}$ at equilibrium. Using these results with (6) and taking $E[\cdot]$ of both sides gives us the fundamental equation governing the weight dynamics of this s-d floating-gate pFET synapse as

$$\tau \frac{dw}{dt} = w^{\gamma}\left[e^{(1/V_{g0} - 1/V_{inj})\Delta V_{out}}\right] - w^{\beta}\left[e^{-\Delta V_{out}/V_{g1}}\right], \quad (8)$$

where we define $\tau = (U_T C_T)/(\kappa_x \kappa_p I_{fg0})$, and all voltages are referenced with respect to ground.

1.3. Ampitude Encoding in Floating-Gate Transistors

Figure 3 shows measurements of the minimum and maximum output voltages versus the output amplitude. For small input amplitudes, the minimum and maximum output voltages deviate symmetrically from the steady-state voltage, but for large input amplitudes, most of the change in the output voltage is due to an increasing maximum output voltage. The steady-state output voltage remains within about V_{inj} of the minimum of the signal. We see that the variance of the fast time-scale input affects the dc operating point of the circuit.

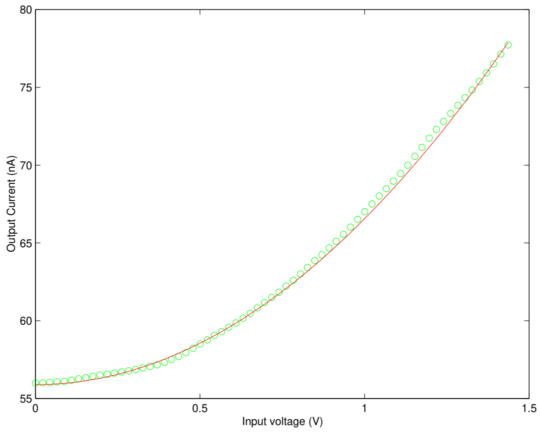

Figure 4: Measurment of steady-state channel current versus V_{out} amplitude for the s-d floating-gate pFET circuit. We also plot a curve fit to this experimental data with $V_{inj}\sqrt{\beta - \gamma} = 1.07\text{V}$.

We want to see if (3) predicts and models this particular AFGA behavior. First, we need to express $E[e^{-\Delta V_{out}/V_{inj}}]$ in terms of the fast and slow variables:

$$E\left[e^{-\Delta V_{out}/V_{inj}}\right] = e^{-\Delta \bar{V}_{out}/V_{inj}} E\left[e^{-\Delta \hat{V}_{out}/V_{inj}}\right]. \quad (9)$$

Then, using (9) to rewrite (3), the steady-state solution for $\Delta \bar{V}_{out}$ is [3]

$$\Delta \bar{V}_{out} = V_{inj} \ln\left(E\left[e^{-\Delta \hat{V}_{out}/V_{inj}}\right]\right). \quad (10)$$

The AFGA always adapts its floating-gate charge such that the minimum of the output signal remains at the equilibrium output voltage. Finally, let us consider the output-voltage behavior as a function of the input-signal amplitude , for a sinusoidal input. We define the amplified input signal as $\Delta \hat{V}_{out} = V_1 \sin(\omega t)$; for this output signal, the steady-state voltage is

$$\Delta \bar{V}_{out} = V_{inj} \ln\left(\int_{\omega t=0}^{2\pi} e^{-(V_1/V_{inj})\sin(\omega t)} d(\omega t)\right)$$
$$= V_{inj} \ln\left(\mathrm{I}_0\left(\frac{V_1}{V_{inj}}\right)\right) \approx \frac{V_1^2}{4V_{inj}}, \quad (11)$$

where $\mathrm{I}_0(\cdot)$ is the modified Bessel function of zero_{th} order. Figure 3 shows measured minimum and maximum output voltages versus the output signal amplitude for a sine-wave input. The results in (11) show that fast timescale signal statistics can affect the adaptation of the output offset voltage.

Figure 4 shows experimental measurements of steady-state channel current versus V_{out} amplitude for the circuit

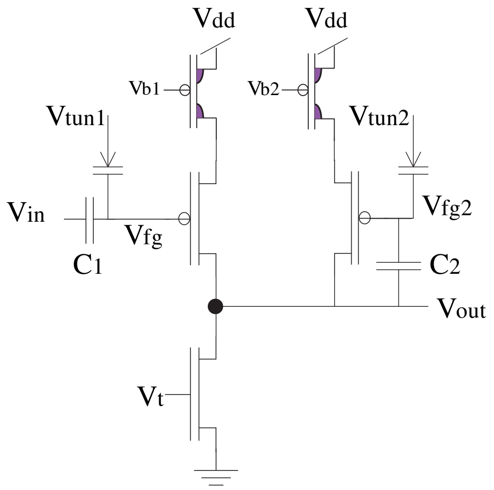

Figure 5: Circuit diagram of the gain-adapting floating-gate AFGA. The s-d pFET device adaptively sets the amplifier's output resistance based upon the output signal amplitude.

in Fig. 1b. The equilibrium current changes with amplitude. We model the equilibrium current by the steady-state solution to (8):

$$w^{\beta-\gamma} = E\left[e^{(1/V_{g0}-1/V_{inj})\Delta V_{out}}\right] / E\left[e^{-\Delta V_{out}/V_{g1}}\right]. \quad (12)$$

Since V_{g0}, V_{g1} are similar in value around 2V in our circuits, we can approximate the above solution to third order as

$$w^{\beta-\gamma} = E\left[e^{-\Delta V_{out}/V_{inj}}\right]. \quad (13)$$

By applying an input signal as $\Delta\hat{V}_{out} = V_1 \sin(\omega t)$, the weight converges to the following steady-state weight:

$$w^{\beta-\gamma} = \mathrm{I}_0\left(\frac{V_1}{V_{inj}}\right)^{1/(\beta-\gamma)} \approx \frac{V_1^2}{4V_{inj}^2(\beta-\gamma)}. \quad (14)$$

From the curve fit to the data in Fig.4, we estimate V_{inj} equal to 750mV. A larger input amplitude results in a larger steady-state channel current (or weight).

2. AFGA WITH GAIN ADAPTATION

Figure 5 shows the gain-adapting AFGA; this circuit employs two continuously adapting floating-gate devices. At fast timescales, we have two bias currents that equal I_{bias}; therefore $\Delta I_1 + \Delta I_2 = 0$. By solving this fast timescale problem and linearizing around its operating point, we get

$$\Delta V_{out} = \frac{C_1}{C_2\kappa_x}\frac{I_{bias1}}{I_{bias2}}\Delta V_{in} = \frac{C_1}{C_2\kappa_x} w \Delta V_{in} \quad (15)$$

The amplifier gain is directly dependant on the weight of the s-d pFET device, that is the ratio of the pFET bias current to the s-d pFET bias current. The parasitic floating-gate–to–drain capacitance limits the maximum gain of this amplifier.

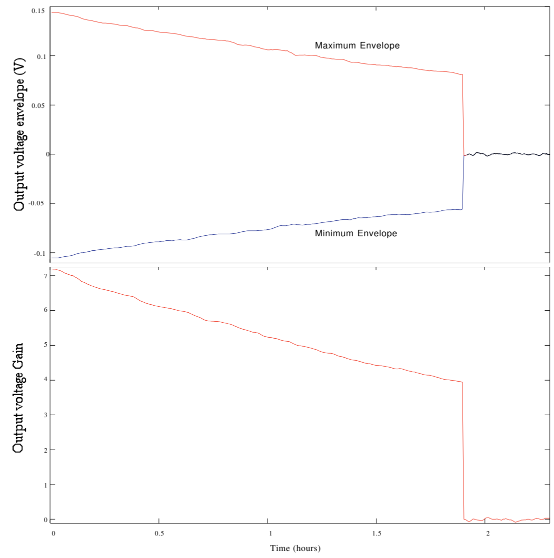

Figure 6: Measured gain adaptation in the circuit shown in Fig. 5. We applied a sine-wave for 1.9 hours; afterwords, we applied only a DC input. For this large amplitude, the amplifier gain decreases; therefore we have adaptation due to statistics in the input signal.

This circuit converges to a single equlbrium as long as the output voltage and DIBL drain voltage remain a few U_T away from the power-supply rails. The solution for the equilibrium weight can be solved by equating (10) and (14), resulting in the simple solution of $w_{eq}^{\beta-\gamma} = 1$; therefore the amplifier will have no adaptation in gain from its maximum value. We also have this case if offset adaptation occurs at a faster timescale than the timescale of the gain adaptation. We experimentally verified that the gain is constant in this region of operation.

Our region of interest is when the gain adaptation occurs at a shorter timescale than the offset adaptation. As a result, we bias our AFGA with an adaptation timeconstant of 10 minutes. Further, since we want a gain smaller than the maximum gain of the AFGA, we set nearly equal bias currents. Fig. 6 shows dynamic gain adaption in this region of interest. The drop in the amplifier gain agrees with the analytical model obtained by combining (14) and (15). This circuit demonstrates that the floating-gate charge adapts the circuit's gain due to statistics in the input signal.

3. REFERENCES

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