A Four-Quadrant Floating-Gate Synapse

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Abstract— **Four-quadrant synapse stuff**

In our first treatments of single-transistor synapses ([1], [2]; elaborated in [3]), we presented the electron-tunneling, hot-electron–injection, and multiplicative behavior of these devices. We used a feedback configuration to characterize the tunneling and hot-electron injection phenomena in these synapses [3]. We also derived an effective learning rule, but we did not consider any specific ways that these synapses could be used in a network. Our presentation of the autozeroing floating-gate amplifier (AFGA) [5], [6] showed the first circuit applications of a single-transistor synapse with continuous oxide currents. In another paper, we generalized the AFGA synapse configuration to consider the behaviors that emerge when single-transistor synapses are coupled together to form various continuous-time learning networks [7]. This paper began to consider these floating-gate devices as continuous-time circuit elements.

This paper presents the next fundament a floating-gate synapse that computes four-quadrant products of its input and weight value, and computes a four-quadrant correlation of the input and output or error function variables. *** need to say something of why four-qudrant computations are important, why they are difficult, etc. *** Four quadrant operation is essential in most adaptive filter and neural network applications. Biological synapses have only seem to have two-quadrant behavior, but .....

** make this paragraph smaller ** Our floating-gate synapses possess five important necessary to build adaptive analog VLSI systems [1], [4]. First, in the absence of learning, the weight is stored permanently; because the floating gate is surrounded by SiO_2, charge leakage is negligible. Second, when operated with subthreshold currents, the synapse's output current is the product of the input signal with the synaptic weight. Third, the synapse requires minimal area, because it comprises only one or two transistors. Fourth, the synapse dissipates a minimal amount of power, because it operates at subthreshold current levels. Fifth, the synapse implements a learning rule for modifying the weight on the floating gate; the form of this rule depends on how various *error signals* are fed back to the floating gate.

In Section I, we review the source-degenerated pFET synapse, and present the operating conditions that we will use in this paper. In Section II, we present and characterize our four quadrant synapse based on source-degenerated pFET synapses. In Section III, we present a small network of four quadrant synapses, and intuitively describe the circuit behavior.

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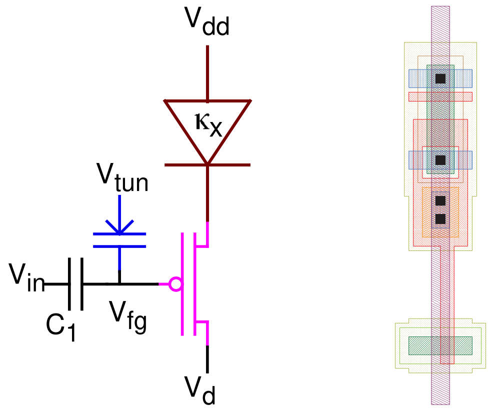


(a) (b)

Fig. 1. The source-degenerated (s-d) pFET synapse. (a) Circuit diagram of the s-d pFET synapse. The s-d pFET synapse is comprised of a pFET single-transistor synapse and the κ_x diode element, which provides feedback to the source terminal. This feedback results in a weaker exponential current dependance of the gate voltage, and changes the circuit dynamics resulting from the floating-gate currents. (b) Layout of the s-d pFET synapse. We utilize the DIBL effect in short-channel MOSFETs to build a compact κ_x element.

I. Source-Degenerated pFET Synapse

Figure 1 shows the circuit model for the source-degenerated (s-d) pFET synapse. We define C_T as the total amount of capacitance connected to the floating gate, and C_2 as the capacitance between floating gate and drain (which is not explicitly drawn for clarity). We assume that all the floating-gate devices are matched. We presented the s-d pFET in terms of its unique feedback properties [7]. The s-d pFET synapse is a pFET synapse that uses a weak exponential element—the κ_x diode in Fig. **??**—to change the injection-current properties versus channel current and drain voltage. We model the κ_x-diode element as

$$I = I_x \exp\left(-\frac{\kappa_x \Delta V}{U_T}\right), \tag{1}$$

where ΔV represents the change in V from the bias level, I_x is the quiesent current through the device, and κ_x is a device parameter. Other synapse elements have similar qualitative properties to the source-degenerated pFET synapse configuration, but the feedback properties might make using these devices more difficult to use in an adaptive network.

We build integrated synapses either by using a short-channel pFET with significant drain-induced barrier lowering (DIBL) to implement the κ_x diode-element, or by using a floating-gate pFET that has a floating-gate–to–drain capacitance much smaller than the total capacitance of the floating gate. A transistor that strongly exhibits DIBL shows an exponential change in current for a linear change in drain voltage. We can also build an external κ_x diode by using an integrated pnp transistor and an op-amp feedback circuit; this approach gives us the freedom to investigate different values of κ_x.

We consider the single-transistor synapse operating with subthreshold channel currents. Many of the behaviors extend qualitatively to above-threshold operation, but as is true of the AFGA [6], the quantitative behaviors do not. Also, we model voltage and current swings around the circuit's steady-state values, because the input signals are capacitively coupled to the floating gate. We describe the subthreshold floating-gate pFET channel current in saturation, I_s, for a change in the pFET's floating-gate voltage, ΔV_{fg}, source voltage ΔV_s, and drain-to-source voltage, ΔV_{ds}, around a bias current, I_{so}, as [6]

$$I_s = I_{so} \exp\left(\frac{\Delta V_s - \kappa_p \Delta V_{fg}}{U_T}\right) \exp\left(-\frac{\Delta V_{ds}}{V_o}\right), \qquad (2)$$

where κ_p is the fractional change in the pFET surface potential due to a change in ΔV_{fg}, V_o is the Early voltage of the pFET, and U_T is the thermal voltage, $\frac{kT}{q}$. We use a modified form of the Early voltage expression that is consistent with classical formulations for large V_o, and more closely models the behavior for small V_o.

We can use the model of the subthreshold pFET channel current to model the drain current of the s-d pFET. By equating the current through the pFET and the κ_x-diode element, and substituting (1) into (2), we obtain the source-degenerated pFET model equation for κ_x much less than 1, which is our region of interest:

$$I_s = I_{so} \exp\left(-\kappa_x \left(\frac{\kappa_p \Delta V_{fg}}{U_T} + \frac{\Delta V_d}{V_o}\right)\right). \qquad (3)$$

Figure 2a shows the channel current through this synapse as a function of gate voltage for three sizes of κ_x; decreasing κ_x reduces the change in channel current for a fixed gate-voltage swing. The κ_x element is effectively cascoded by the pFET; therefore, from (3), the maximum voltage gain of this transistor is $\frac{\kappa V_o}{U_T}$, which is identical to that of a non-degenerated subthreshold pFET transistor.

We use electron tunneling to remove electrons from floating gates. By expanding the classic model of electron tunneling through a silicon–silicon-dioxide system [9] for small changes in V_{fg} and V_{tun} [5], we get

$$\begin{aligned} I_{tun} &= I_{tun0} \exp\left(\frac{\Delta V_{tun} - \Delta V_{fg}}{V_x}\right), & (4)\\ &= I_{tun0} \left(\frac{I_s}{I_{so}}\right)^{\frac{U_T}{\kappa_p \kappa_x V_x}}, & (5) \end{aligned}$$

where V_x is a parameter related to the quiescent tunneling and floating-gate voltages, I_{tun0} is the quiescent tunneling current, and ΔV_{tun} is the change in the tunneling voltage. Our experimental measurements show that the tunneling current is nearly a constant power of I_s for small κ_x, and the power increases with decreasing κ_x.

We use hot-electron injection to add electrons to floating gates. If we are to inject an electron onto a floating gate, the MOSFET must have a high-electric-field region to accelerate channel electrons to energies above the silicon–silicon-dioxide barrier, and in that region the oxide electric field must transport the electrons that surmount the barrier to the floating gate. We derived previously the hot-electron–injection model for the source-degenerated pFET as [7]:

$$\begin{aligned} I_{inj} &= I_{inj0} \exp\left(\frac{\sigma \Delta V_g}{U_T}\right) \exp\left(-\frac{\Delta V_d}{V_{inj}}\right), & (6)\\ &= I_{inj0} \left(\frac{I_s}{I_{so}}\right)^{-\frac{\sigma}{\kappa_p \kappa_x}} \exp\left(-\frac{\Delta V_d}{V_{inj}}\right), & (7) \end{aligned}$$

where $\sigma = \kappa_p \left(\frac{U_T}{V_{inj}} - \kappa_x \alpha\right)$, for small κ_x. The value of κ_x strongly affects the source-current dependence of the injection current. For small κ_x, an increase in the source current requires a large increase in the source voltage, which decreases the drain-to-source voltage, and that, in turn decreases the injection current. From our previous experimental results [7], this linearized approximation is valid for only an order of magnitude change in the source current for small κ_x. This region is much smaller than the valid region for tunneling, but is sufficient for the scope of this paper.

We model the floating-gate behavior by equating the currents at the floating gate:

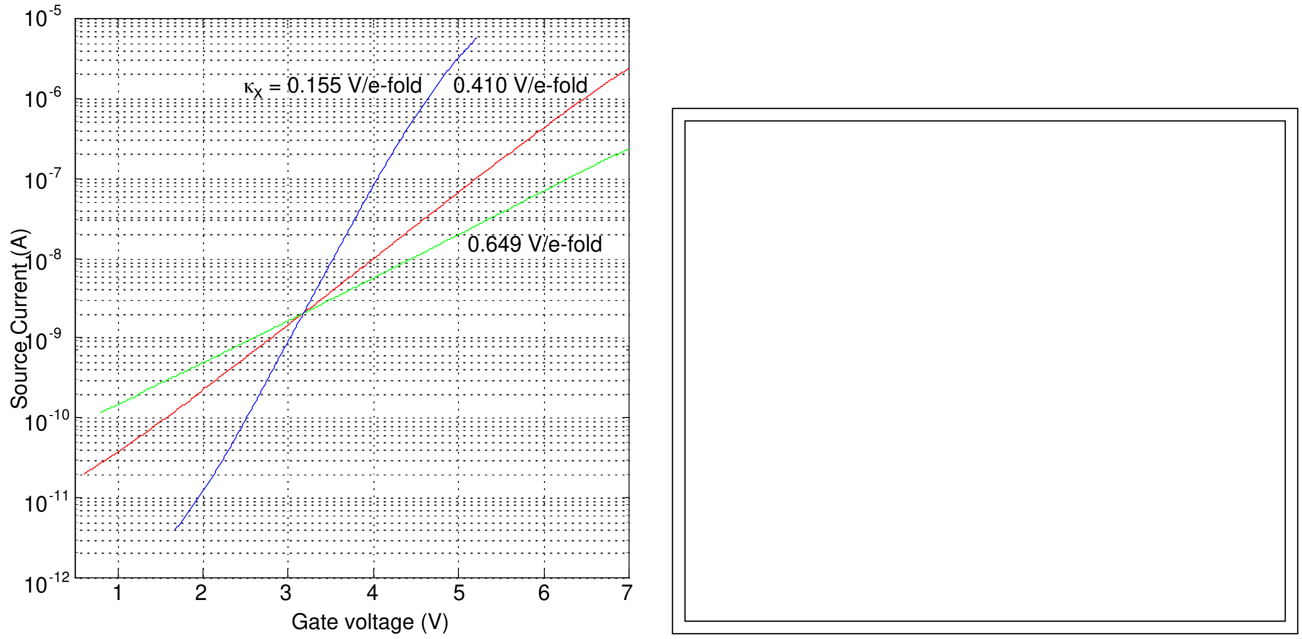
$$C_T \frac{dV_{fg}}{dt} = C_1 \frac{dV_{in}}{dt} + C_2 \frac{dV_d}{dt} + I_{tun} - I_{inj} \qquad (8)$$

where I_{tun} and I_{inj} are the pFET floating-gate currents due to electron tunneling and hot-electron injection. To analyze the adaptation behavior in FGMOS circuits, we decompose our variables into components that change at fast and slow rates. The fast-rate variables represent the rapid changes due to the input signals; the slow-rate variables represent the floating-gate charge (the synapse weights). We assume that we can decompose the synapse terminal voltages as sums of fast ($\Delta\hat{V}$) and slow ($\Delta\bar{V}$) quantities as

$$\begin{aligned} \Delta V_d &= \Delta\hat{V}_d + \Delta\bar{V}_d,\\ \Delta V_s &= \Delta\hat{V}_s + \Delta\bar{V}_s,\\ \Delta V_{fg} &= \Delta\hat{V}_{fg} + \Delta\bar{V}_{fg}. \end{aligned} \qquad (9)$$

Neglecting Early voltage effects, the source current becomes

$$I_s = I_{so} W \exp\left(-\frac{\kappa_x \kappa_p \Delta\hat{V}_{fg}}{U_T}\right), W = \exp\left(-\frac{\kappa_p \Delta\bar{V}_{fg}}{U_T}\right), \qquad (10)$$



(a) (b)

Fig. 2. Characterization of the s-d pFET synapse. (a) Drain current versus gate voltage for two different values of κ_x, as well as for no κ_x element. (b) Plot of $\frac{dW}{dt}$ versus W for different values of V_{tun} and V_{dd}. For this data, I_{s0} is equal to xx nA. Increasing the drain voltage decreased the steady-state value of W, and increasing V_{tun} increases the steady state value of W.

where we define W to be the weight of the synapse. The time derivative of W for the pFET synapse is

$$\frac{d\bar{V}_{fg}}{dt} = \frac{U_T}{\kappa_n W}\frac{dW}{dt} = \frac{U_T}{\kappa_n}\frac{d\log(W)}{dt}; \tag{11}$$

in Figs. ?? and ??, we plot the derivative of $\log(W)$ versus W to illustrate the dependence of source current on the floating-gate currents. At fast timescales, we approximate the tunneling and injection currents to be negligible; we model the behavior at the fast timescales as (V_{in} has only fast components)

$$C_T\frac{d\hat{V}_{fg}}{dt} = C_1\frac{dV_{in}}{dt} + C_2\frac{d\hat{V}_d}{dt} \rightarrow \hat{V}_{fg} = \frac{C_1}{C_T}V_{in} + \frac{C_2}{C_T}\hat{V}_d. \tag{12}$$

By substituting $\frac{d\bar{V}_{fg}}{dt}$ in (11), we obtain the dynamical equations for slow timescales as

$$-\frac{C_T U_T}{\kappa_x\kappa_p W}\frac{dW}{dt} = C_2\frac{d\bar{V}_{out}}{dt} + I_{tun} - I_{inj}, \tag{13}$$

We set $I_{tun0} = I_{inj0}$, because in equilibrium the tunneling current should equal the injection current. By combining (5), (7) and (13), we get the dynamical equation for the weights as

$$\tau\frac{dW}{dt} = W^{1-\frac{\sigma}{\kappa\kappa_x}} e^{\frac{\sigma C_1}{C_T U_T}\Delta V_{in}} e^{-\frac{\Delta V_{out}}{V_{inj}}} - W^{1+\frac{U_T}{\kappa\kappa_x V_x}} e^{-\frac{C_1 \Delta V_{in}}{C_T V_x}} \tag{14}$$

$$\tau\frac{dW}{dt} = \begin{array}{l} W^{1-\frac{\sigma}{\kappa\kappa_x}} \exp\left(\frac{\sigma C_1}{C_T U_T}\Delta V_{in}\right) \exp\left(-\frac{\Delta V_{out}}{V_{inj}}\right) \\ -W^{1+\frac{U_T}{\kappa\kappa_x V_x}} \exp\left(-\frac{C_1 \Delta V_{in}}{C_T V_x}\right) \end{array} \tag{15}$$

where τ_l is equal to $\frac{C_T U_T}{\kappa_x \kappa I_{so}}$. Figure xxx shows plots of ....

Consider a particular choice of κ_x, V_{tun}, and V_{dd} biases such that the following conditions hold:

$$V_x = \frac{U_T}{\kappa\kappa_x}, \text{and } \frac{\kappa}{V_{inj}} = \frac{2}{V_x}. \tag{16}$$

These conditions require that

$$\frac{\sigma}{U_T} = \frac{1}{V_x} \text{ and } \frac{\sigma}{\kappa\kappa_x} = 1. \tag{17}$$

We choose this region because it clarifies our solution techniques, and it is easy to select circuit parameters which are near to these quantities. Typical bias conditions of ..... with the κ_x element efolding every 300mV satisfies these requirements. We define V_y equal to $V_x(C_T/C_1)$; the dynamical equation in (15) become

$$\tau\frac{dW}{dt} = e^{-\frac{\Delta V_{in}}{V_y}} e^{-\frac{\Delta V_{out}}{V_{inj}}} - W^2 e^{-\frac{\Delta V_{in}}{V_y}} \tag{18}$$

Figures ?? and ?? show the characterization of this s-d pFET synapse built with these conditions.

II. A Four-Quadrant Floating-Gate Synapse

The dynamic behavior of a single synapse can be characterized from that synapse's response in both a constant-current configuration and a constant-voltage configuration [7]. The s-d pFET synapse has the unique property that is has stabilizing feedback four both configurations. The two s-d pFET synapses cooperate for the entire available channel current; regardless of the starting position, the two

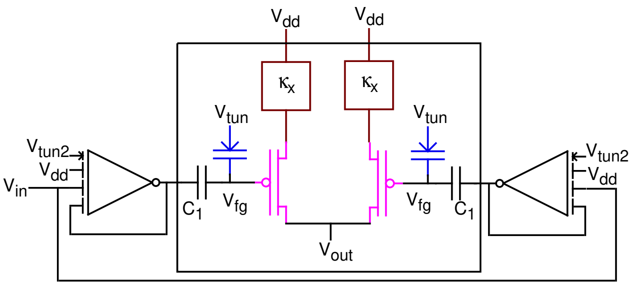


Fig. 3. Circuit of the four-quadrant floating-gate synapse. This synapse is composed of two s-d pFET synapses and two AFGAs. The AFGAs filter slowly varying input signals and provide an inverted signal to the complementary synapse element.

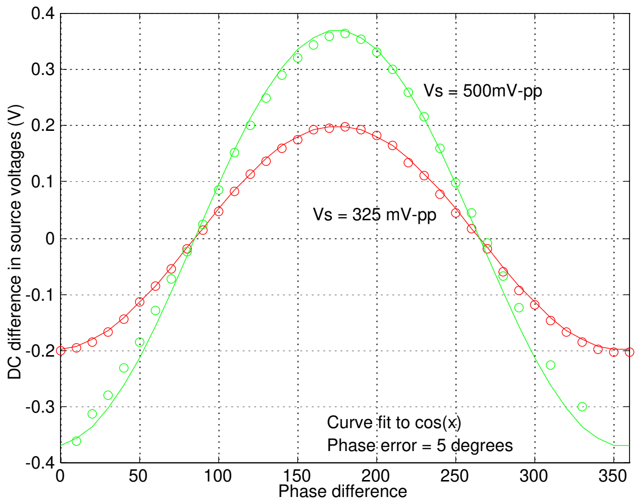


Fig. 4. Difference of the DC source voltages due to two 220Hz sine-wave inputs of different phase versus phase difference. DC level of the drain voltage was 1.778V, and V_{dd} was 12V. This measurement shows how the circuit encodes the correlation between the two sine waves.

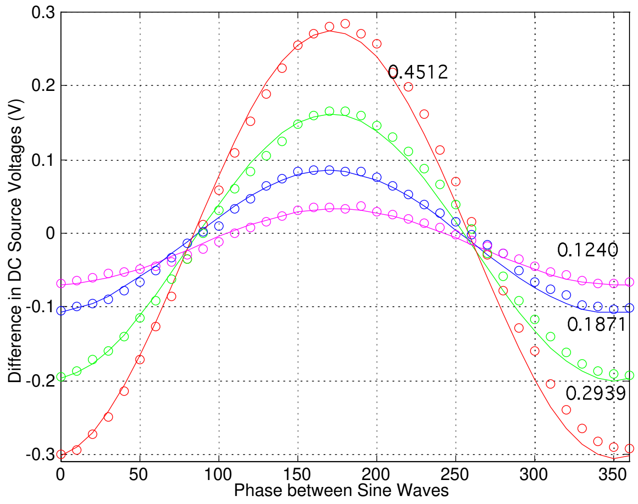


Fig. 5.

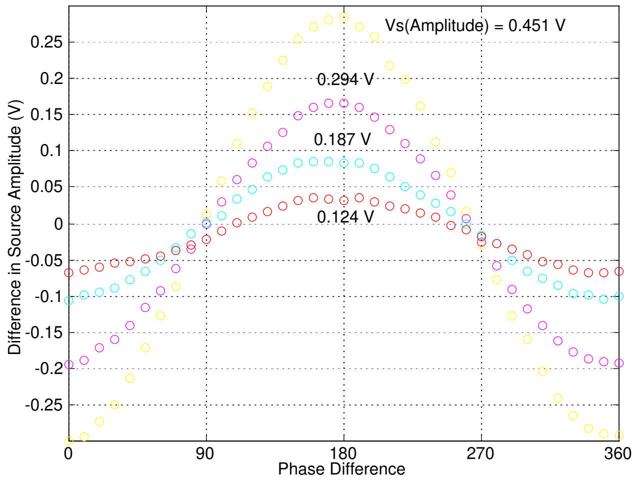


Fig. 6.

synapses converge to nearly equal channel currents. Also, in this section, we will ignore C_2 effects.

Figure 3 shows the circuit and symbol from the floating-gate synapse. The input to this synapse, or a column of synapses, enters in on AFGAs to eliminate any slow variation on the input signal and to provide an inverted version of the input. This synapse couples two s-d pFET synapses in a way that subtracts out their common responses to achieve a four-quadrant multiplication and correlation. The dynamics of two or more coupled floating-gate synapses result in one to all synapses settling to a non-zero weight [?]; a coupled network of pFET synapses will have at most one non-zero weight for constant inputs. Using s-d pFET synapses usually results in each synapse converging to a non-zero weight. The following two subsections consider the two fundamental circuit configurations, fixing the source current or the drain voltage, of the four-quadrant floating-gate synapse.

A. Fixed-Drain Configuration

Consider the synapse in Fig. 3 with inputs applied to V_{in} and V_{out} around a constant bias voltage. We will first show that this simple modification naturally gives us four quadrant multiplications. At fast timescales, the floating-gate voltage is related to the input voltages as

$$\Delta\hat{V}_{fg1} = -\Delta\hat{V}_{fg2} = \frac{C_1}{C_T}\Delta V_{in} \qquad (19)$$

With the above definitions, we get the output current as

$$I_{out} = I_{so}\left(W_1 e^{-\Delta V_{in}/V_y} + W_2 e^{\Delta V_{in}/V_y}\right); \qquad (20)$$

$$I_{out} = I_{so}\left(W_1 \exp\left(-\frac{\kappa\kappa_x C_1 \Delta V_{in}}{C_T U_T}\right) + W_2 \exp\left(\frac{\kappa\kappa_x C_1 \Delta V_{in}}{C_T U_T}\right)\right); \qquad (21)$$

assuming the inputs are within the input linear range, $U_T/(\kappa_x\kappa)$,

$$I_{out} = I_1 + I_2$$

$$I_{out} \approx I_{so}(W_1 + W_2) + \frac{\kappa\kappa_x C_1 I_{so}}{C_T U_T}(W_1 - W_2)\Delta V_{in}.$$

$$I_{out} \approx I_{so}(W_1 + W_2) + W\frac{\Delta V_{in}}{V_y}. \tag{22}$$

The synapse weight, defined by $W = W_1 - W_2$, and ΔV_{in} take on both positive and negative values; therefore the change in the output current is a four-quadrant product of the input by the synapse weight for fast timescales. This approach to obtain four-quadrant is not unexpected due to the tradition in continuous-time filters to get highly linear elements by playing two elements off each other; typically this leads to four-quadrant behaviors and multiplication of resulting parameters. This type of approach has been used in both conventional Previous analog and neural network circuits used a similar approach to get added linearity or multiple quadrants of operation, but usually at the expense of significantly more circuit complexity [10], [?].

What is not expected or understood is how to get simultanious four-quadrant correlations in the same circuit configuration. In this configuration, the input voltage and output voltage have no slowly moving variables. We can write the dynamics for the two weights, W_1 and W_2, from (18) by substituting the appropriate variables. Subtracting and adding these two weight equations, we get

$$\tau\frac{dW}{dt} = \left(e^{-\frac{\Delta V_{out}}{V_{inj}}} - 1\right)\left(e^{\frac{\Delta V_{in}}{V_y}} - e^{-\frac{\Delta V_{in}}{V_y}}\right)$$
$$+e^{\frac{\Delta V_{in}}{V_y}} - e^{-\frac{\Delta V_{in}}{V_y}} + W_2^2 e^{\frac{\Delta V_{in}}{V_y}} - W_1^2 e^{-\frac{\Delta V_{in}}{V_y}} \tag{23}$$

$$\tau\frac{d(W_1 + W_2)}{dt} = e^{-\Delta V_{out}/V_{inj}}\left(e^{\Delta V_{in}/V_y} + e^{-\Delta V_{in}/V_y}\right)$$
$$-W_2^2 e^{\Delta V_{in}/V_y} - W_1^2 e^{-\Delta V_{in}/V_y} \tag{24}$$

Taking the expected value of both sides of (23), (24) results in

$$\tau\frac{dW}{dt} = E\left[\left(e^{-\frac{\Delta V_{out}}{V_{inj}}} - 1\right)\left(2\sinh\left(\frac{\Delta V_{in}}{V_y}\right)\right)\right]$$
$$+W_2^2 E\left[e^{\frac{-\Delta V_{in}}{V_y}}\right] - W_1^2 E\left[e^{\frac{\Delta V_{in}}{V_y}}\right] \tag{25}$$

$$\tau\frac{d(W_1 + W_2)}{dt} = 2E\left[e^{-\Delta V_{out}/V_{inj}}\cosh\left(\frac{\Delta V_{in}}{V_y}\right)\right]$$
$$-W_2^2 E\left[e^{\Delta V_{in}/V_y}\right] - W_1^2 E\left[e^{-\Delta V_{in}/V_y}\right] \tag{26}$$

If ΔV_{in}, and ΔV_{out} are within this linear range, then we can make the following approximations:

$$\sinh\left(\frac{\Delta V_{in}}{V_y}\right) \approx \frac{\Delta V_{in}}{V_y} = X$$

$$\exp\left(-\frac{\Delta V_{out}}{V_{inj}}\right) - 1 \approx \frac{\Delta V_{out}}{V_{inj}} = Y, \tag{27}$$

and that simplifies (25), (26) to

$$\tau\frac{dW}{dt} = 2E[XY] + W(W_2 + W_1)$$

$$\tau\frac{d(W_1 + W_2)}{dt} = 2 - W_2^2 + W_1^2 \tag{28}$$

which is a managable set of differential equations.

- A gain error in the amplifier would simply be a multiplicitive term in the positive or negative weight, and therefore would be seen as an offset in the long term floating gate voltage, but this is the parameter which is being adapted; therefore there is no problem.

If we assume $W_1 + W_2$ is nearly constant, that is only relaxing this condition slightly to account for differences in W_1 and W_2, then the above equation always converges to the following steady state:

$$W_1 - W_2 = \frac{4E\left[\left(e^{-\frac{\Delta V_{out}}{V_{inj}}} - 1\right)\left(\sinh\left(\frac{\Delta V_{in}}{V_y}\right)\right)\right]}{W_1 + W_2} \tag{29}$$

then the solution is

$$W_1 - W_2 = \frac{E[XY]}{W_1 + W_2}$$

which is similar to LMS, Hebbian, and related outer product rules.

The next question is how does the sum, $W_1 + W_2$ converge to its steady state (or what steady state this sum converges to)? Adding the two dynamical equations for W_1 and W_2 that we get from (18):

$$\tau\frac{d(W_1 + W_2)}{dt} = e^{-\frac{\Delta V_{out}}{V_{inj}}}\left(e^{\frac{\Delta V_{in}}{V_y}} + e^{-\frac{\Delta V_{in}}{V_y}}\right)$$
$$+W_2^2 e^{\frac{\Delta V_{in}}{V_y}} + W_1^2 e^{-\frac{\Delta V_{in}}{V_y}} \tag{30}$$

Now by taking E[·] of this equation, we get

$$\tau\frac{d(W_1 + W_2)}{dt} = e^{-\frac{\Delta V_{out}}{V_{inj}}}\left(e^{\frac{\Delta V_{in}}{V_y}} + e^{-\frac{\Delta V_{in}}{V_y}}\right)$$
$$+W_2^2 e^{\frac{\Delta V_{in}}{V_y}} + W_1^2 e^{-\frac{\Delta V_{in}}{V_y}} \tag{31}$$

We can directly show that $W_1^2 + W_2^2$ converges to 1; therefore $W_1 + W_2$ will be between 1 and $\sqrt{2}$ for $W_1 - W_2 = 1$, which is the normal extend of the weight values.

If we mesaured the voltages at the source nodes, what behavior would we expect?

$$\Delta V_{s1} - \Delta V_{s2} = \frac{U_T}{\kappa_x}\ln\left(\frac{W_1}{W_2}\right) + 2\kappa\frac{C_1}{C_T}\Delta\hat{V}_{in}$$

Note, the sum is similar except that the second term does not exist unless there is mismatch between devices.

In steady state, we can evaluate

$$\ln\left(\frac{W_1}{W_2}\right) = \frac{1}{2}\ln\left(\frac{E\left[e^{-\frac{\Delta V_{out}}{V_{inj}}}e^{-\frac{\Delta V_{in}}{V_y}}\right]/E\left[e^{-\frac{\Delta V_{in}}{V_y}}\right]}{E\left[e^{-\frac{\Delta V_{out}}{V_{inj}}}e^{-\frac{\Delta V_{in}}{V_y}}\right]/E\left[e^{\frac{\Delta V_{in}}{V_y}}\right]}\right) \tag{32}$$

Assume we apply sinusoidial inputs at the input and output of the form

$$\Delta V_{in} = A_1 V_y \sin(\omega t), \text{and} \Delta V_{out} = A_2 V_{inj}\sin(\omega t)$$

In this case,

$$E\left[\exp\left(\frac{\Delta V_{in}}{V_y}\right)\right] = E\left[\exp\left(\frac{\Delta V_{in}}{V_y}\right)\right]$$

$$\ln\left(\frac{W_1}{W_2}\right) = \frac{1}{2}\ln\left(\frac{I_o(A_1 - A_2)}{I_o(A_1 + A_2)}\right) \tag{33}$$

where $I_o(\cdot)$ is the Bessel function of zeroth order. If we assume the arguments of the Bessel function are small, then we can approximate $I_o(x) = 1 + \frac{1}{4}x^2$, which simplifies (**??**) as

$$\ln\left(\frac{W_1}{W_2}\right) = -\frac{1}{2}A_1 A_2$$

Also note that a 180 degree phase shift on one input inverts this sign, therefore we get a four-quadrant correlation function.

We also get similar expressions for two similar amplitudes with a phase shift and for square-wave inputs.

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