THE MATCHING OF SMALL CAPACITORS FOR ANALOG VLSI

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ABSTRACT

The capacitor has become the dominant passive component for analog circuits designed in standard CMOS processes. Thus, capacitor matching is a primary factor in determining the precision of many analog circuit techniques. In this paper, we present experimental measurements of the mismatch between square capacitors ranging in size from $6\,\mu m \times 6\,\mu m$ to $20\,\mu m \times 20\,\mu m$ fabricated in a standard $2\,\mu m$ double-poly CMOS process available through MOSIS. For a size of $6\,\mu m \times 6\,\mu m$, we have found that those capacitors that fell within one standard deviation of the mean matched to better than 1%. For the $20\,\mu m \times 20\,\mu m$ size, we observed that those capacitors that fell within 1 standard deviation of the mean matched to about 0.2%. Finally, we observed the effect of nonidentical surrounds on capacitor matching.

1. INTRODUCTION

As analog circuits have been integrated with digital circuits on CMOS chips, the capacitor has come to dominate analog circuit design. In many cases, resistors are unavailable in CMOS processes, and inductors are generally unattractive for use in the design of all but RF or microwave circuits. As a result, many analog circuits rely on capacitor matching to achieve high accuracy; these include switched capacitor filters [1], many D/A and A/D converters [2], [3], and precision gain amplifiers [4]. A recent study [5] indicated that one can obtain capacitor ratios that match to better than 0.1% by interleaving identical capacitors, each between $20\,\mu m$ and $40\,\mu m$ on a side, and connecting them in clever alternating patterns. This technique is well suited to situations in which a relatively small number of high-precision analog circuits is required on a single VLSI chip. However, as the integration density of analog circuits increases [6], smaller cell sizes will prohibit the use of such techniques. Consequently, the question of how well small capacitors can be expected to match arises.

To begin to answer this question, we fabricated linear arrays of square capacitors, ranging in size from $6\,\mu m \times 6\,\mu m$ to $20\,\mu m \times 20\,\mu m$, in a standard $2\,\mu m$ double-poly process available through MOSIS. We measured the resulting mismatch in capacitance as a function of side length. In section 2, we describe the experimental procedure that we used to measure the capacitance mismatch. In section 3, we present the results of the study. In section 4, we discuss these results.

2. EXPERIMENTAL METHOD

We assessed capacitance mismatch by measuring the current–voltage (I/V) characteristics of νMOS transistors [7] operating in the subthreshold region [8], using the experimental setup depicted in Fig. 1. A νMOS transistor is a floating-gate MOS transistor with multiple control gates that capacitively couple into the floating gate, establishing the floating gate's voltage via a capacitive divider. For present purposes, the drain current of a saturated subthreshold νMOS transistor with grounded source and fixed drain is given by

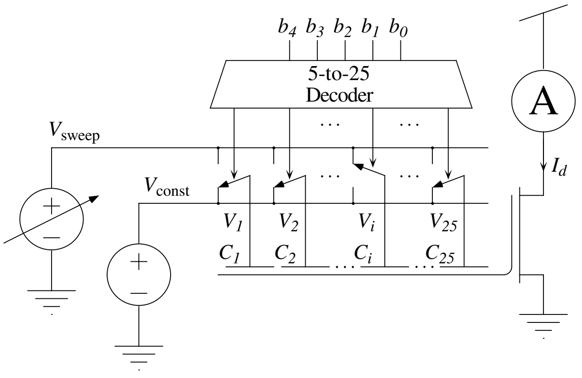


Figure 1. Experimental setup used to measure capacitance mismatch.

$$I_d = \mathrm{I}_0 \exp\left\{\frac{\kappa Q}{\mathrm{C_T U_T}}\right\} \exp\left\{\frac{\kappa}{\mathrm{C_T U_T}} \sum_{i=1}^{N} C_i V_i\right\},$$

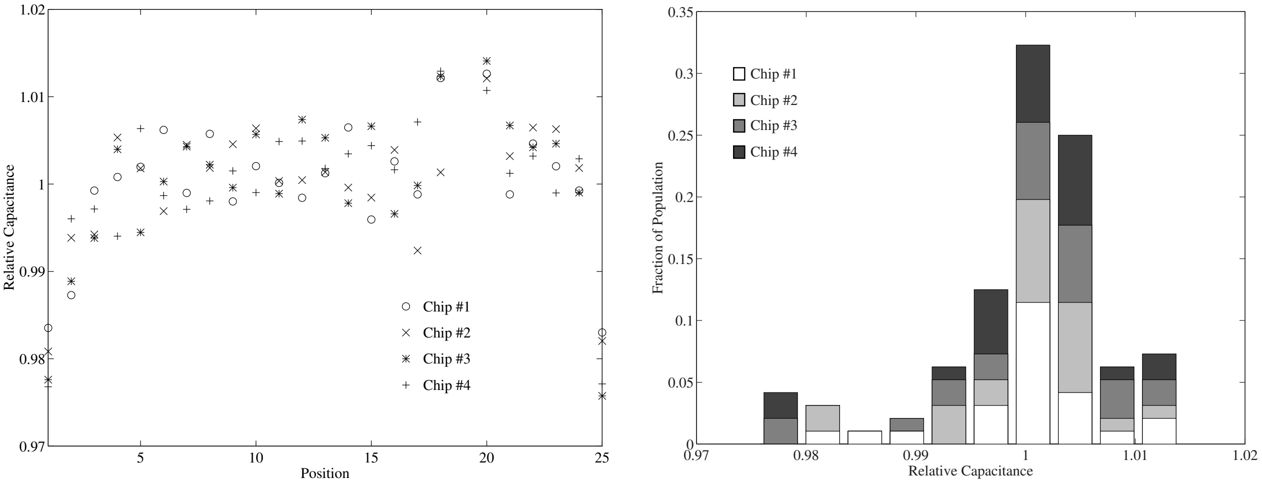
where I_0 is the subthreshold pre-exponential current factor, κ is the back-gate coefficient, Q is the net charge stored on the floating gate, $\mathrm{U_T}$ is the thermal voltage ($\frac{\mathrm{kT}}{\mathrm{q}}$), $\mathrm{C_T}$ is the total capacitance "seen" by the floating gate, C_i is the capacitance of the ith control gate, and V_i is the voltage of the ith control gate. If all but the ith control gate are held fixed at some constant voltage, $\mathrm{V_{const}}$, and I_d is measured while V_i is swept, then the transistor's I/V curve will have the form

$$I_d = \mathrm{I_{const}} \exp\left\{\frac{\kappa C_i V_i}{\mathrm{C_T U_T}}\right\},$$

where $\mathrm{I_{const}}$ is given by

$$\mathrm{I_{const}} = \mathrm{I}_0 \exp\left\{\frac{\kappa Q}{\mathrm{C_T U_T}}\right\} \exp\left\{\frac{\kappa \mathrm{V_{const}}}{\mathrm{C_T U_T}} \sum_{j \neq i} C_j\right\}.$$

The slope of the resulting I/V curve on a semilog plot is directly proportional to the capacitance of the ith control



(a) (b)

Figure 2. Relative capacitance distribution for $6\,\mu m \times 6\,\mu m$ capacitors. (a) Plot showing relative capacitance as a function of position. Note that the capacitors on the left and right edges of the array (i.e., positions 1 and 25) are systematically lower than the rest by nearly 2%. These capacitors have only one neighbor, whereas all the rest have two. (b) Histogram of relative capacitance.

gate, C_i. All the control gates were designed to be nominally identical. We successively swept each control-gate voltage in turn, while measuring the drain current over the same range of currents; the mismatch in the slopes of the resulting exponential I/V curves directly gives the mismatch in the coupling capacitances.

A chip with eight 25-input νMOS transistors was fabricated in the ORBIT $2\,\mu m$ double-poly n-well CMOS process available through MOSIS. The control gates of each νMOS transistor were identically drawn squares arranged in a linear array. The first νMOS transistor's control gates were $6\,\mu m \times 6\,\mu m$. The second νMOS transistor's control gates were $8\,\mu m \times 8\,\mu m$, and so on in $2\,\mu m$ increments up to $20\,\mu m \times 20\,\mu m$ for the control gates of the eighth νMOS transitor. For each of the four chips, we swept each control gate of each νMOS transistor from ground to $5\,V$ in $100\,mV$ increments while measuring the drain current. We extracted the slopes of the resulting exonential I/V characteristics by linear regression and statistically analyzed the distributions of the slopes.

3. EXPERIMENTAL RESULTS

We normalized each of the slope distributions (i.e., for each capacitor size and for each chip) to have a mean of unity by dividing each by its sample mean. We call the resulting normalized quantities *relative capacitances.* We pooled the relative-capacitance distributions from the four chips tested. Figure 2 shows the relative-capacitance distribution for the $6\,\mu m \times 6\,\mu m$ capacitors. Figure 3 shows the relative-capacitance distribution for the $20\,\mu m \times 20\,\mu m$ capacitors. Figures 2(a) and 3(a) show relative capacitance as a function of position in the array for the $6\,\mu m$ and $20\,\mu m$ cases, respectively. Note that the capacitors on the ends of the arrays are systematically lower than are the rest (almost 2% in the $6\,\mu m$ case, and 0.5% in the $20\,\mu m$ case). We observed this trend for all capacitor sizes tested. The capacitors on the ends of each array have only one neighbor, whereas all the rest have two. These data corroborate the well-known fact that one can improve matching by using identical surrounds [9], and suggest that we can markedly improve the matching of small capacitors by adding dummy capacitors where needed. Figures 2(b) and 3(b) show histograms of relative capacitance for the $6\,\mu m$ and $20\,\mu m$ cases, respectively.

Finally, we computed the coefficient of variation (defined as the ratio of the standard deviation of a distribution divided by the distribuition's mean) for each capacitor size; the data are plotted as a function of drawn side length in Fig. 4.

4. CONCLUSION

We have presented experimental measurements of the mismatch between square capacitors ranging in size from $6\,\mu m \times 6\,\mu m$ to $20\,\mu m \times 20\,\mu m$, fabricated in the ORBIT $2\,\mu m$ double-poly n-well CMOS process available through MOSIS. For a size of $6\,\mu m \times 6\,\mu m$, we found that those capacitors that fell within 1 standard deviation of the mean matched to better than 1%, with a worst case of 4%. For the $20\,\mu m \times 20\,\mu m$ size, we observed that those capacitors that fell within 1 standard deviation of the mean matched to 0.2%, with a worst case of 1%. Finally, we observed the effect of nonidentical surrounds on the matching of small capacitors. Our data indicate that one can construct analog circuits with reasonably accurate (e.g., to 1% or better) characteristics using small capacitors by the use of dummy capacitors in suitable places.

5. ACKNOWLEDGMENTS

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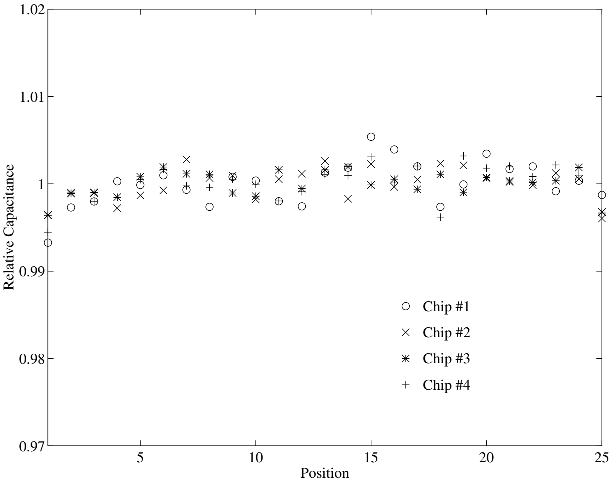
1.02
1.01
1
0.99
0.98
0.97
Relative Capacitance
5
10
15
20
25
Position
Chip #1
Chip #2
Chip #3
Chip #4