LEARNING IN FLOATING-GATE PFET SYNAPSES

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Floating-gate devices can be used as adaptive analog computational elements. Considered as an analog computational element, a floating-gate device computes its output as a product of its input and an adaptive device parameter. We call the adaptive device parameter the weight. When used as an adaptive analog computational element, we call the floating-gate device a synapse, since we will use it to build electronic neural networks. The weight dynamics of the floating-gate pFET is unstable, so we add source- degenerative feedback to obtain a stable system. The source-degenerated (s-d) floating-gate synapse is shown in Fig. 1.

A fundamental question we would like to answer is how we adapt the synapse weight based on the device's input and output signals. We study the weight dynamics of the floating-gate pFET synapse and the effects of the pFET's gate and drain voltages on these dynamics. Experimental data showing the weight equilibrium for sinusoidal inputs on the gate and drain terminals appears in Fig. 2. The figure shows how the equilibrium weight varies when both sinusoid amplitudes are fixed and the phase difference is varied.

We show that we can derive a weight update rule such that the equilibrium weight value is proportional to the correlation between the gate and drain voltages. From our s-d pFET synapse, we obtain a Hebbian learning rule with weight decay:

$$\tau \Delta \dot{w} = -\Delta w + \eta E[xy], \tag{1}$$

where x is the (input) signal on the gate terminal, y is the (error) signal on the drain terminal, Δw is the weight of this synapse, and τ is the adaptation rate. The Hebbian learning rule is is a special case of outer-product learning which is fundamental to most neural network models, including self-organizing neural networks. We obtain this rule by approximating the weight dynamics of the pFET synapse around a given equilibrium point. We develop this approximation by considering the basic functional form of the system dynamics and then examining the effects of the gate and drain voltages on the specifics of this form.

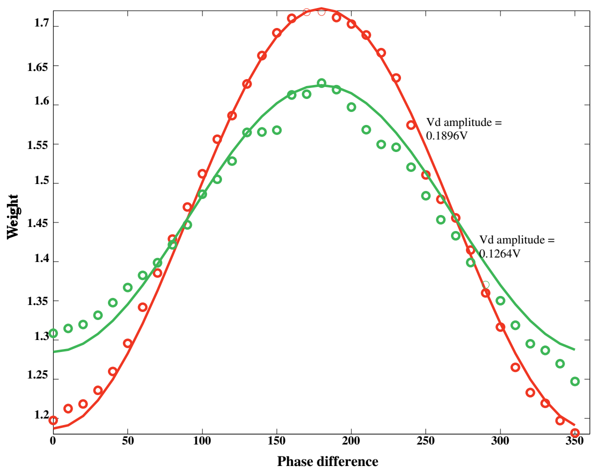

Figure 2: Change in the dynamical weight equation due to various degrees of correlation (phase difference) between sinusoidal input signals at the gate and drain terminals. The amplitude of the input sine wave was 1.29V.

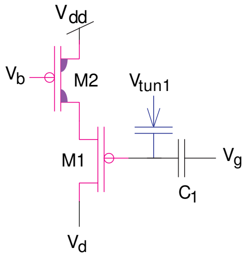

Figure 1: Circuit diagram of our floating-gate pFET synapse. The synapse is comprised of a floating-gate pFET synapse and a second ultra-short pFET, which provides feedback to the source terminal. We use a short-channel pFET to take advantage of drain-induced barrier lowering (DIBL) to build a compact weakly exponential element.