A FLOATING-GATE TECHNOLOGY FOR DIGITAL CMOS PROCESSES

Bradley A. Minch

Cornell University
Ithaca, NY 14853-5401
minch@ee.cornell.edu

Paul Hasler

Georgia Institute of Technology
Atlanta, GA 30332-0250
phasler@ee.gatech.edu

ABSTRACT

We discuss the possibility of developing high-quality floating-gate memories and circuits in digital CMOS technologies that have only one layer of polysilicon. Here, the primary concern is whether or not we can get adequate control-gate linearity from MOS capacitors. We employ two experimental proceedures to address this issue and find acceptable floating-gate circuit behavior with MOS capacitors. First, we simultaniously characterize a MOS capacitor and a linear capacitor; the experimental data show that MOS capacitors behave similarly to linear capacitors over a finite, but usable range. Second, we characterize two typical floating-gate MOS circuit primatives, a floating-gate amplifier and a multiple-input translinear element, two basic circuits that rely heavily on the linearity of the capacitors that couple into the floating gates. Our measurements show that floating-gate circuits with MOS-capacitor control gates behave like their counterparts built with linear capacitors over specific regions of operation.

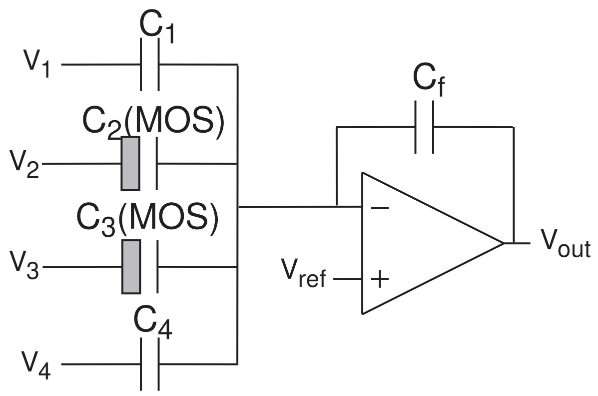

Figure 1: Experimental measurment set-up to characterize linear capacitors (C_1, C_4) and MOS capacitors (C_2, C_3).

1. INTRODUCTION

Recently, there has been a tremendous amount of interest in using multiple-input floating-gate MOS (FGMOS) transistors to build circuits that process information by linearly summing a number of input voltages on the floating-gate via a capacitive voltage divider [3]. Nearly all such FGMOS circuits have been developed in CMOS processes with two levels of polysilicon. Unfortunately, the second poly layer results in significantly higher fabrication costs; consequently, this option is now found in only a small percentage of current commercial processes. Our motivation for this work is to demonstrate that we can build high-performance, floating-gate memories and circuits in digital CMOS processes that have only one layer of polysilicon. The primary issue is whether or not we can obtain adequate control-gate linearity with MOS capacitors. Current research in a similar vein for switched-capacitor circuits gives us reasonable hope of similar results for FGMOS circuits [1]. The focus of this paper is to address the performance of FGMOS circuits using MOS-capacitor control gates.

Figure 1 shows the experimental set-up that we use to measure the capacitance-voltage characteristics of our candidate control-gate capacitors; the circuit shown is completely integrated on a single chip. With this circuit arrangement, we can measure the capacitance-voltage relationship of a capacitor using dc voltage sweeps or with simple gain measurements. Thus, we have a direct method for measuring capacitance without constructing the sort of resonance circuits that are typically used to measure capacitance-voltage characteristics of MOS capacitors. The closed-loop gain from a capacitor input to the amplifier output is set by the ratio of the input capacitance to the feedback capacitance. For example, the gain from V_1 to V_{out} is $-C_1/\ C_f$; therefore, we can calculate C_1 as a function of the voltage across it by measuring the gain of the amplifier at that bias voltage. Thus, if the feedback capacitor is linear, we have a direct measure of the capacitance of the on-chip capacitor under test. By coupling some of the inputs into the floating node through poly-poly capacitors, we can simulaneously characterize the linearity of these “linear” capacitors. The reference voltage, V_{ref}, sets the floating-gate voltage. We must construct the floating node from the polysilicion layer, so, for the MOS capacitors (C_2, C_3), we connect input signals to separate wells through well-plug diffusion.

2. CAPACITORS: LINEAR AND MOS

Figure 2 illustrates the differences between poly-poly capacitors, which are only available in double-poly processes, and MOS capacitors, which available in any CMOS process. The top illustrations depict typical layout views of the linear (poly-poly) and the MOS capacitors; the bottom ones

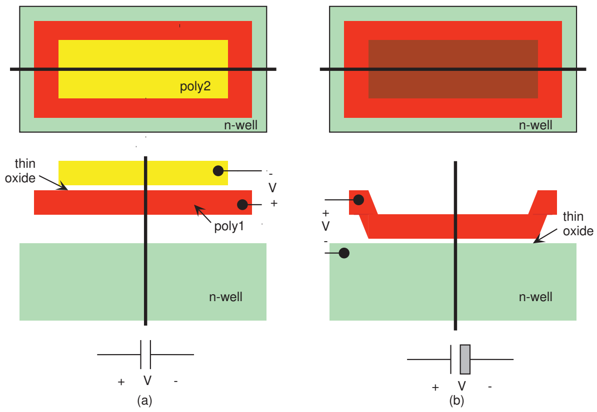

Figure 2: Layout, cross section, and circuit symbol of two integrated capacitors. (a) The linear capacitor. (b) The MOS Capacitor.

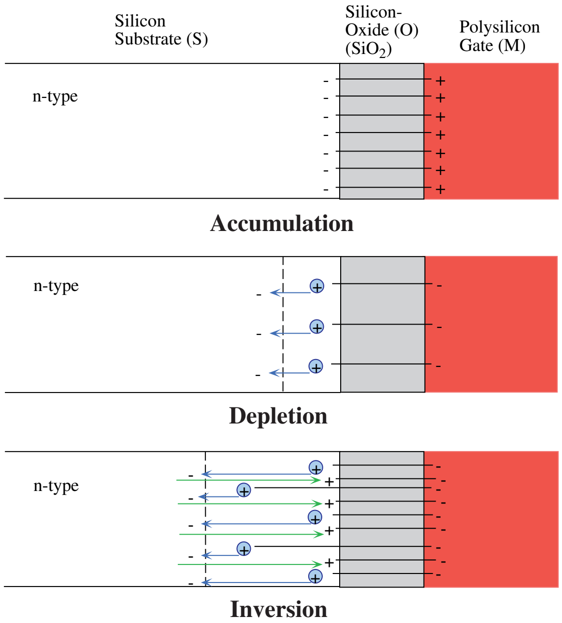

Figure 3: Illustration of the three operating regimes of an MOS capacitor: accumulation, depletion, and inversion.

show a cross-section for each of these two capacitors along the line indicated in the layout view. The linear capacitor, shown in Fig. 2a, is a nearly ideal parallel-plate structure, comprising two conducting plates separated by a very thin high-quality dielectric. Because the MOS capacitor, shown in Fig. 2b, is fundamental to the MOS transistor structure, it requires no additional processing steps, and therefore is available in all CMOS processes. From the standpoint of implementing control gates, the main limitations of MOS capacitors are that the control-gate capacitance can vary with the control-gate voltage, and that each capacitor requires a separate well, which costs in silicon real estate. However, for many applications, the area increase might be relatively small, and the cell sizes will be nearly identical to what they would be in CMOS processes that provide a diffused capacitor option.

3. CHARACTERIZING THE MOS CAPACITOR

The nonconstant capacitance-voltage relationship is the biggest difference between MOS capacitors and linear capacitors. If we want use MOS capacitors in place of linear ones in FG-MOS circuits, then understanding their large-signal behavior is vital, because their nonlinear characteristics will impose limitations on our circuit's operating ranges. A MOS capacitor has three operating regions: accumulation, depletion, and inversion; each of these regions is illustrated in Fig. 3. A MOS capacitor operating in accumulation terminates gate-charge field lines on majority carriers at the silicon–silicon-dioxide interface. In our case, additional gate charges are terminated by building up additional electrons at the silicon–silicon-dioxode interface. A MOS capacitor operating in depletion terminates additional gate-charge field lines on exposed ions in the silicon depletion region. Larger voltages require a wider depletion region, thereby reducing the series capacitance of the depletion region. A MOS capacitor operating in inversion brings externally generated (minority) carriers to the silicon surface to terminate the field lines emanating from additional gate charges. These carriers are either thermally generated in the silicon depletion region, or come from neighboring p+ diffusion regions.

Ideally, we want our MOS capacitors to be operating either in accumulation or in inversion at all times, because the capacitance will remain fairly constant in these two regimes. The voltage at the transistion between accumulation and depletion is called the flatband voltage, and the voltage at the transition between depletion and inversion is called the threshold voltage. For our well-based MOS capacitors, the threshold voltage is about 0.8 V, and the flatband voltage is roughly -0.4 V. A MOS capacitor acts most like a parallel-plate capacitor when operated in accumulation; therefore, if we bias the floating-gate–to–well voltage across each capacitor so that it is greater than the flatband voltage, we should obtain nearly linear MOS capacitor operation.

4. CAPACITANCE-VOLTAGE MEASUREMENTS

Figure 4a shows the output voltage of the circuit of Fig. 1 as a function of the difference of input voltage and V_{ref}, becuase the capacitance of the MOS capacitor depends on the voltage across it. For these experiments, we are holding V_{ref} constant while sweeping V_2, which is connected to a MOS capacitor that is about four times the area of C_f. For the linear-capacitor inputs, an output voltage between the power-supply rails is always a linear function of the applied capacitor voltage; the data shown in Fig. 4a clearly shows that this is the case only in limited regions for a MOS capacitor. From Fig. 4b, the capacitance at flatband (≈ -0.4 V) has dropped by 15% from its maximum value, and the capacitance reaches its minimum value near the

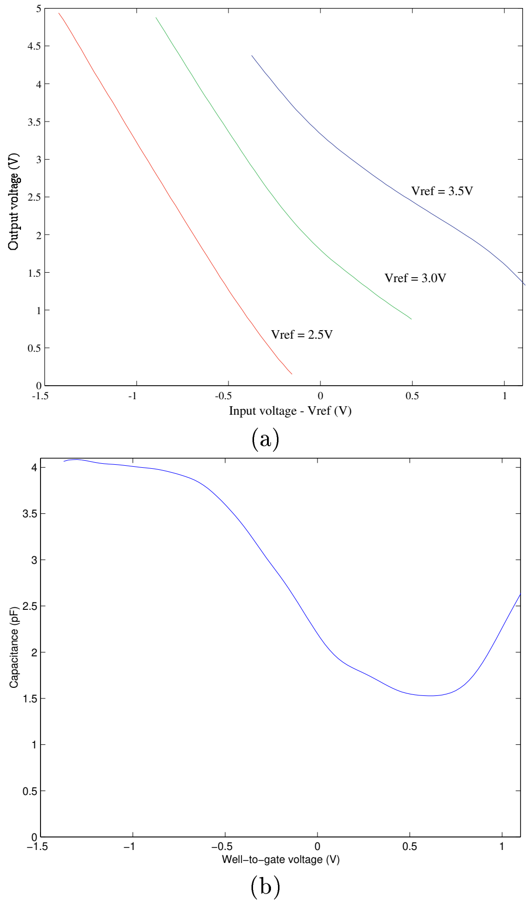

Figure 4: Measurements from the test set-up of Fig. 1 for an MOS capacitor. (a) Transfer curves for an MOS-capacitor input with different values of V_{ref}. The linear capacitor had a nearly constant capacitance for all applied bias voltages. (b) The extracted MOS capacitor C-V curve from the measurements. From these data, we clearly see two MOS capacitor operating regions, accumulation and inversion, where the capacitance is nearly constant, so we can use it in place of a linear capacitor.

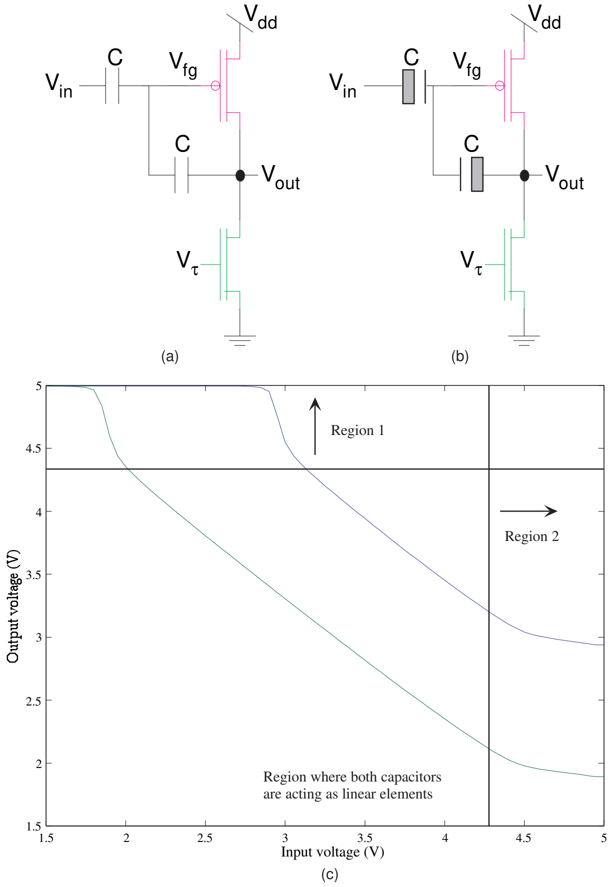

Figure 5: Unity-gain inverting floating-gate amplifiers. (a) Floating-gate amplifier circuit using linear capacitors. (b) Floating-gate amplifier circuit using MOS capacitors. (c) Transfer curves for the MOS-capacitor amplifier; it had a constant gain of -1 for a relatively wide range of input and output voltages. The linear-capacitor amplifier had a constant gain of -1 from rail-to-rail.

threshold voltage (≈ 0.8 V). The shape of the capacitance-voltage curve extracted from the V_2 sweep closely agrees with those obtained from MOS-capacitor inputs of different sizes.

5. FLOATING-GATE MOS CAPACITOR CIRCUITS

In this section, we investigate how using MOS capacitors affects the performance of FGMOS circuits whose characteristics depend critically on the linearity of the coupling capacitors. We fabricated two basic FGMOS circuit primatives, a floating-gate amplifier and a multiple-input translinear element (MITE), in a 1.2μm CMOS process, with MOS-capacitor control gates and we compared their characteristics to similar circuit elements fabricated with linear-capacitor control gates. We found that the MOS-capacitor floating-gate circuits will act like their linear-capacitor counterparts if the gate-to-well voltages are always a few hundred millivolts larger than the MOS capacitor's flatband voltage.

5.1. MOS Capacitors in a Floating-Gate Amplifier

Figure 5a shows the schematic of a unity-gain inverting floating-gate amplifier with linear capacitors, and Fig. 5b shows the schematic of the same amplifier, except with MOS capacitors. The gain of both amplifiers from input (V_{in}) to output (V_{out}) is designed to be -1. The amplifier using linear capacitors showed a linear response for all output votlages between the power-supply rails. Figure 5c shows measured data for the amplifier of Fig. 5b. This amplifier has a linear response, like the amplifier of Fig. 5a, except in two regions. In Region 1, the feedback MOS capacitor goes into depletion, decreasing the feedback capacitance, thereby increasing the closed-loop amplifier gain. In Region 2, the input MOS capacitor goes into depletion, decreasing the input capacitance, thereby decreasing the

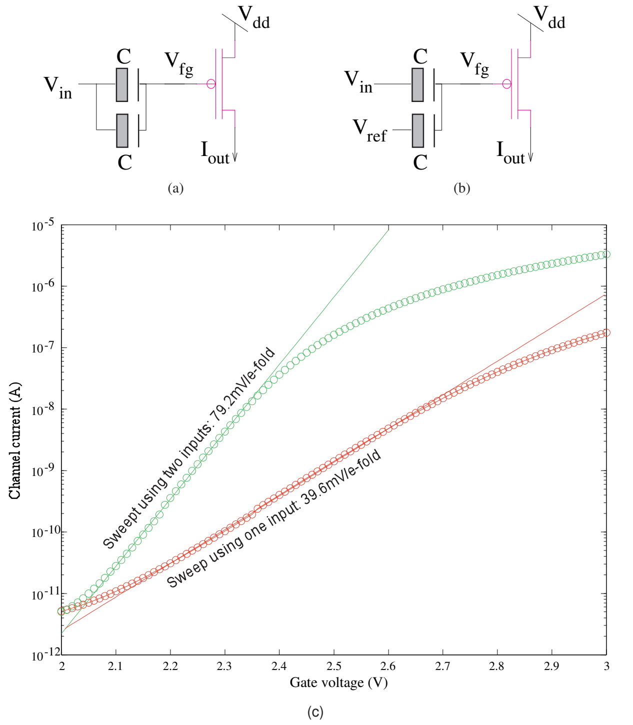

Figure 6: A two-input MITE with MOS-capacitor inputs. For these measurements, we set V_{dd} at $5\,V$ and we adjusted the floating-gate charge so the MOS capacitors were biased into accumulation. Circuit arrangement for measuring the channel current while (a) sweeping both control gates together and (b) sweeping one input while holding the other constant. (c) Measured MITE current-voltage characteristics. These curves are nearly identical to those obtained from two-input MITEs with linear-capacitor control gates; under these conditions, we expect to see exponentials current-voltage characteristics with slopes in a ratio of 2:1.

closed-loop amplifier gain.

By modifying the floating-gate charge, we can shift the amplifier's operating point. We modify the charge on the floating-gate by a combination of hot-electron injection and electron tunneling, as we have described previously [3]. Figure 5c shows transfer curves for two different amplifier operating points. Because the region boundaries are the same for both curves, we conclude that this operating-range limitation is due the voltage dependence of the two MOS capacitors.

5.2. MOS-Capacitor Multiple-Input Translinear Elements

We recently introduced a new translinear circuit primative, which we call the multiple-input translinear element (MITE) [2, 4]. Such an element produces an output current that is exponential in a weighted sum of its input voltages. For the most part, we use the capacitive voltage division on a floating-gate to implement the weighted voltage summation and we use either a subthreshold MOS transistor or a bipolar transistor to produce the exponential output current. For example, a single subthreshold multiple-input FGMOS transistor can serve as a MITE. From MITEs, we can build low-voltage translinear circuits, called MITE networks [2, 5], that accurately embody product-of-power-law relationships in the current signal domain. The power laws in these relationships depend primarily on ratios of control-gate capacitors, so nonconstant control-gate capacitances directly result in nonconstant power-law relationships for these circuits.

To assess the possibility of implementing MITE networks, we fabricated several two-input MITEs with two identical MOS-capacitor control gates in a 1.2μm CMOS process and measured their current-voltage characteristics. Figure 6 shows a typical current-voltage characteristics for one such two-input MITE. For these measurements, we set V_{dd} at $5\,V$ and we adjusted the floating-gate charge using electron tunneling so the MOS capacitors were biased into accumulation. We swept both control gates together and measured the channel current and then we swept one of the control gates with the other held fixed. Figure 6c shows typical measured current-voltage characteristics for such experiments. These curves are nearly identical to those obtained from two-input MITEs with linear-capacitor control gates that we have fabricated previously [4]; under such conditions, we expect to see exponential current-voltage characteristics in the subthreshold region with slopes in a ratio of 2:1, which is evident from the data of Fig. 6c.

6. CONCLUSIONS

In this paper, we raised the possibility of using accumulated MOS capacitors as control gates in FGMOS circuits. We found that, as long as the floating-gate–to–well voltage is always a few hundred millivolts larger than the MOS capacitor's flatband voltage, the MOS-capacitor FGMOS circuits perform like their linear-capacitor counterparts. Therefore, we believe that most of the FGMOS circuit techniques that have been developed recently can be applied in standard digital CMOS processes.

7. REFERENCES

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