

A Floating-Gate-Based Field-Programmable Analog Array

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Abstract—A field-programmable analog array (FPAA) with 32 computational analog blocks (CABs) and occupying $3 \times 3 \text{ mm}^2$ in $0.35\text{-}\mu\text{m}$ CMOS is presented. Each CAB has a wide variety of subcircuits ranging in granularity from multipliers and programmable offset wide-linear-range Gm blocks to nMOS and pMOS transistors. The programmable interconnects and circuit elements in the CAB are implemented using floating-gate (FG) transistors, the total number of which exceeds fifty thousand. Using FG devices eliminates the need for SRAM to store configuration bits since the switch stores its own configuration. This system exhibits significant performance enhancements over its predecessor in terms of achievable dynamic range ($> 9 \text{ b}$ of FG voltage) and speed ($\approx 20 \text{ gates/s}$) of accurate FG current programming and isolation between ON and OFF switches. An improved routing fabric has been designed that includes nearest neighbor connections to minimize the penalty on bandwidth due to routing parasitic. A maximum bandwidth of 57 MHz through the switch matrix and around 5 MHz for a first-order low-pass filter is achievable on this chip, the limitation being a “program” mode switch that will be rectified in the next chip. Programming performance improved drastically by implementing the entire algorithm on-chip with an SPI digital interface. Measured results of the individual subcircuits and two system examples including an AM receiver and a speech processor are presented.

Index Terms—Analog signal processing, field-programmable analog array (FPAA), floating-gate (FG), reconfigurable system.

I. RASP 2.8: OVERVIEW

WE present a field-programmable analog array (FPAA) with over 50,000 floating-gate (FG) elements, allowing it to operate as a reconfigurable analog signal processor (RASP). The FG devices serve as switches for reconfiguration and also endow the sub-circuits with tunable parameters. Using FG devices as switches eliminates the need for extra memory to store the configuration of the switches. Essentially, these devices perform “computation in memory” leading to high computational area efficiency. This is one of the first large-scale FPAA devices

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reported that is capable of versatile computations, making it a viable platform for prototyping and implementing analog signal processing tasks.

In the recent past, FPAAs have been gaining popularity because of their ability to allow rapid prototyping, flexibility in testing, and reducing the design cycle time, reasons that led to the growth of the FPGA market. However, most of the FPAAs reported in literature or available commercially have a small number of computational analog blocks (CABs) with high-performance components. The few designs that have a large number of CABs [1], [2] are specifically designed for constructing programmable analog filters. The chip we present has a wide assortment of components in the CABs ranging from folded Gilbert cell multipliers and programmable offset transconductors to simple pMOS and nMOS transistors. This offers the user more flexibility in creating circuits. This also permits the usage of the chip in teaching analog circuits in a class, a task that has been performed multiple times.

An aspect of FPAAs that has attracted considerable attention is the parasitic effects and under-utilization of the switch matrix. A method for overcoming this problem is to use the switch matrix devices as valid circuit elements [2], [3]. In our chip also, since the voltage on the gate of the FG devices can be programmed in a continuum, we have used these devices as circuit elements in various cases. To reduce the parasitic capacitance due to the OFF switches in a crossbar-type network, routing lines of varying sizes are present so that the length of the line chosen can depend on the number of components to be connected.

Initial results from this chip were presented in [4]. Here, we present complete characterization of the system and provide examples of two different systems proving the versatility of the chip. In Section II, we describe the architectural details of the chip including the CAB components and switch matrix. Section III presents the software infrastructure for programming the chip. In Section IV, characterization of the CAB components and simple sub-circuits are presented. In Section V, an AM receiver and a speech processing system are detailed as examples of the computational power of the chip. Finally, we conclude by comparing our work with others in Section VI.

II. ARCHITECTURE

The architecture of the chip is depicted in Fig. 1 and a die photograph of the chip (fabricated in $0.35\text{-}\mu\text{m}$ CMOS) is shown in Fig. 2(b). It consists of a set of 32 CABs arranged in a 4×8 matrix. An interconnect matrix comprising FG elements allows for arbitrary connectivity between components. FG elements

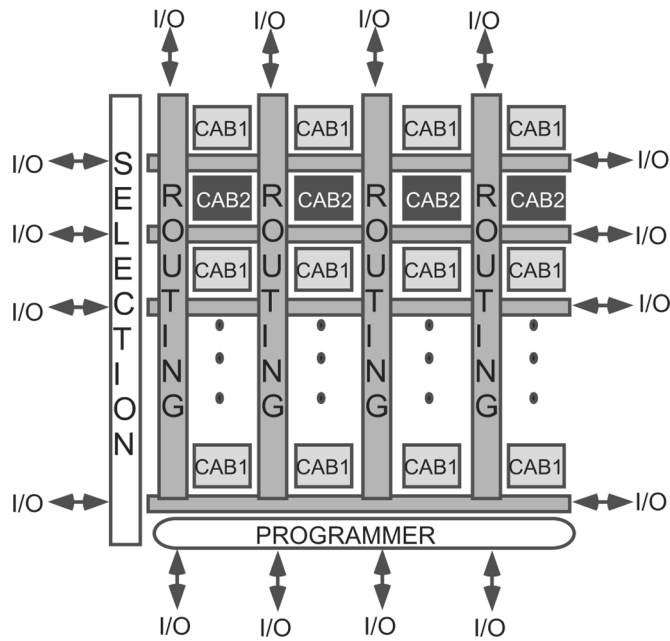


Fig. 1. Architecture: The chip is organized into an array of 4×8 CABs with multilevel interconnect matrix in between. CABs are of two types. The circuitry for selection and programming of FG elements is at the periphery of the array.

show insignificant charge loss over tens of years [5]–[7]—hence this FPAA holds its configuration even after it is powered down. There are two types of CABs whose components are detailed later. The selection and programming circuits for setting the desired charge on the FG devices are placed at the periphery of the array. The chip has 56 pins available for routing signals. More details about each part is detailed in the following subsections.

A. Routing

The routing architecture of the IC shown in 2(a) demonstrates the different types of interconnections—local vertical (loc), local horizontal (rows), nearest neighbor vertical and horizontal (nnv and nnh), global vertical (glob), and global horizontal (gh). The glob/gh lines span the entire length of the chip vertically/horizontally. There are 4 gh/10 glob lines per row/column of CABs. The local lines span the length/width of one CAB only. There are 41 rows and 4 loc lines. The rows form a fully connected crossbar network with the different vertical lines allowing any CAB node to connect with any routing line. The nnv lines (six for each neighbor) connect to vertically neighboring CABs while the nnh lines (four for each neighbor) connect two horizontally neighboring ones. This granularity allows for high-speed interconnects to be routed on low-capacitance lines like local or nearest neighbors while global connections are used only for I/O after the internal processing is complete. Bandwidth of a signal passing through two switches and one nnv and one loc lines has been found to be 57 MHz. The other feature of the routing scheme is bridge transistors that allow local/nnv/nnh lines to be bridged between CABs facilitating variable-length connections without incurring the capacitance penalty of global lines.

The parasitic capacitance associated with the routing lines have been estimated. The extracted capacitances are 1.6 pF for

glob, 1.5 pF for gh, 552 fF for nnh, 458 fF for nnv lines, and 220 fF for a loc line. Thus, routing between CABs can be accomplished with relatively lower parasitic as compared with the earlier version. In addition, this characterization allows one to use the routing as extra capacitance that can be used in circuits.

B. Switch Isolation and Programming

The programmable switch matrix used in the earlier FPAA [8] used the application of different gate and drain voltages for obtaining isolation between ON and OFF switches. However, this method has a number of disadvantages, the primary one being over-injection of devices beyond the isolation point [9]. This IC employs the superior source side selection [9] coupled with indirect programming [10] to achieve impressive isolation while not sacrificing the quality of an ON switch. Fig. 3(a) shows the architecture of one switch element that occupies $13 \times 6 \mu\text{m}^2$. The rsel signal provides source side selection by cutting off the current in the switches not being programmed. V_{gate} and V_{d} are the voltages provided by two on-chip DACs for programming the FG device. A similar architecture is used for the bias FG elements. For more precise matching between the direct and indirect transistors, an array of coefficients for V_T mismatch of each direct–indirect pair of transistors needs to be stored for predistortion of the programmed currents.

The “disconnect” switch serves to cut off the rows from the CAB based on a control signal. Each of these transmission gates were made wide to reduce ON resistance below 500Ω but have been found to provide 400 fF of capacitance when turned ON. This factor combined with maximum accurately programmed currents of $20 \mu\text{A}$ provides a limitation on the maximum achievable frequency on this FPAA and will be rectified in the next version by reducing their width. However, this chip can still be used for many applications requiring lesser speed like audio processing or low frequency ultrasound. Also, higher effective throughput may be obtained by employing parallelism.

Fig. 3(b) shows the variation of the resistance of an ON switch with temperature. It increases with temperature due to a decrease in mobility. It has a value of around 9 k Ω at room temperature. The OFF switches have a resistance that is more than 10 G Ω . The ON switch resistance can be reduced further if the gate voltage (currently at mid rail) can be lowered to ground. This option is also being included in the next version of the chip.

C. CAB Elements

The CABs are of two major types as shown in Fig. 1. Fig. 2(c) depicts the components in the two CABs. The first one has three operational transconductance amplifiers (OTAs), three floating capacitors (500 fF each), two multi-input floating gates which can be used for constructing translinear circuits using MITE architectures, a voltage buffer, a transmission gate with dummy switch for switched-capacitor applications, and nMOS/pMOS transistor arrays with two common terminal for easily constructing source-follower or current-mirror topologies. All of the OTAs are biased using FG transistors, giving the user the option to trade off bandwidth, noise, and power. Two of the OTAs have FG differential pairs (FGOTA) which enable programming the offset of the amplifier as well as provide a wide

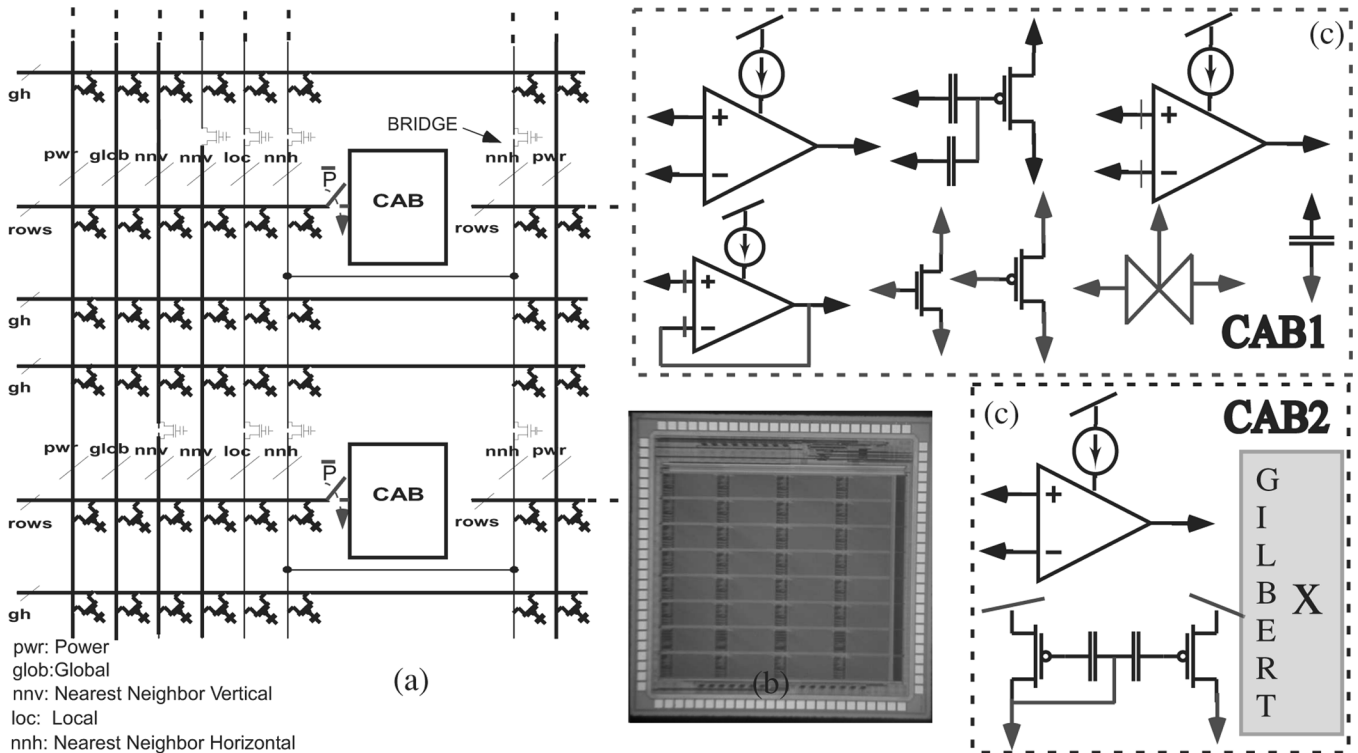


Fig. 2. Switch matrix. (a) The different categories of routing lines interconnecting the CABs is shown. Global, nearest neighbor, and local routing options are available on this chip, allowing one to optimally route their circuit. (b) The die photograph of the chip is shown. (c) The components in the two types of CABs vary from programmable transconductors and multipliers to transistors and capacitors.

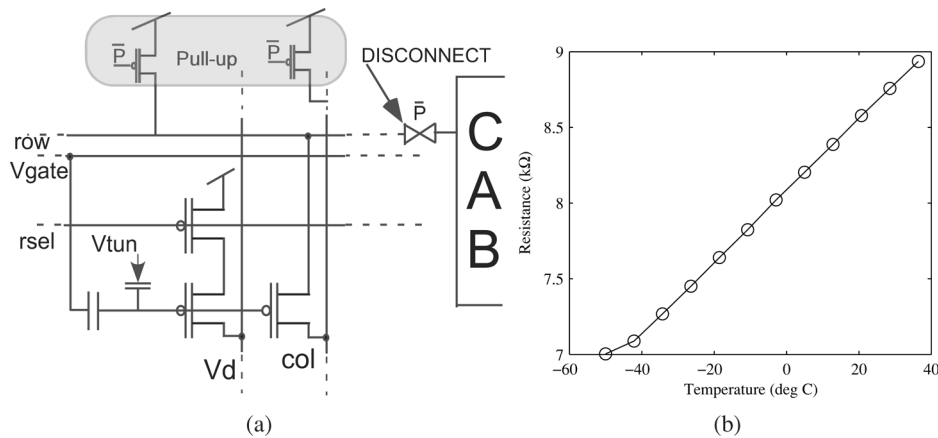


Fig. 3. Switch performance. (a) Architecture of the indirectly programmed switch and associated selection circuits is shown. (b) Switch resistance is plotted as a function of temperature. Its value at room temperature is around 9 kΩ.

input linear range that is essential to reduce distortion in Gm-C filters and oscillators. The second type of CAB has two folded Gilbert multipliers and a FG current mirror in addition to a wide-linear-range OTA. The multiplier also has FG differential pairs to reduce distortion. These CAB components can be connected using the switch-matrix consisting of FG switches. The choice of CAB elements was motivated by typical audio signal processing architectures (for de-noising or gain compression) which require different nonlinear feedback mechanisms around a multiplier. Some flexibility has also been provided to allow for either current or voltage mode processing.

D. On-Chip Programming

Earlier generations of the FPAA [8] used off-chip current measurement circuits which led to inaccuracy in the measurement due to noise and increased the minimum measurable current to the ESD leakage. Fig. 4(a) shows the architecture of the current programming scheme which does all measurement operations on-chip and provides a digital SPI interface to a microprocessor (uP) or FPGA. Binary scaled current mode 7-bit DACs are used to supply the gate and drain voltages during programming. The drain selection circuit connects the drain to current

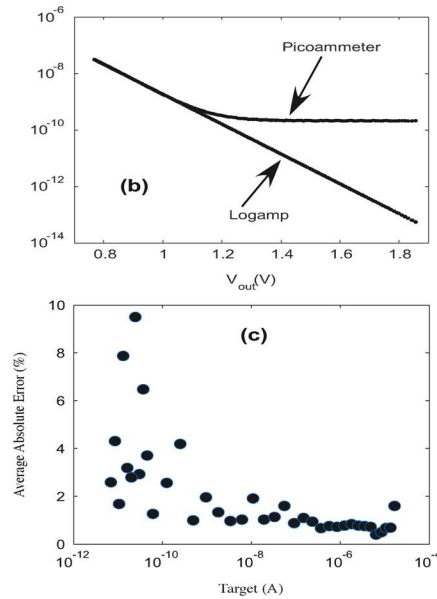
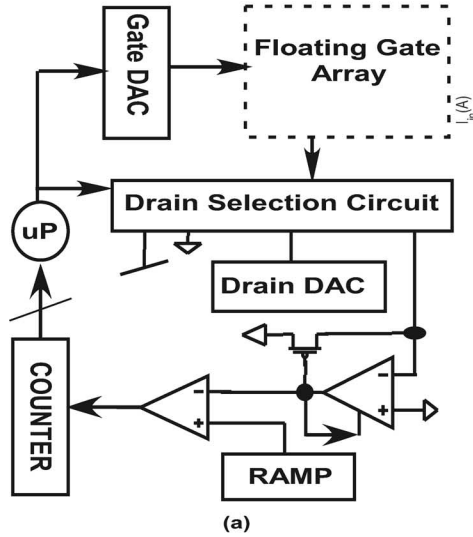


Fig. 4. Programming. (a) Architecture of the on-chip programming module. Seven-bit DACs supply gate and drain voltages while a floating-point ADC converts the FG current to a digital code. A micro-controller hosts the state machine for the programming algorithm and completes the feedback loop for programming. (b) Measured output from the logarithmic amplifier demonstrating its capability to measure very low currents (≈ 100 fA) while the off-chip measurement gets limited around 100 pA due to leakage from pads and noise on the board. (c) Average accuracy of the programmed currents over 6 pA–20 μ A.

measurement circuits, drain DAC, ground or V_{dd} based on the current state of the programming algorithm.

The huge improvement in measuring accuracy, speed, and dynamic range is obtained by using a logarithmic transimpedance amplifier (TIA) described in [11]. SNR is improved by using source degeneration on the feedback PMOS. The TIA is kept stable over a wide range of currents by adaptively biasing it based on the input current. Fig. 4(b) shows measured current from an off-chip pico-ammeter which saturates at the ESD leakage level of around 100 pA while the inferred current from the TIA goes below 100 fA. The current is inferred based on a curve fit to the I - V characteristic of the TIA for currents in the range of 1–10 nA. The logamp is followed by a low-pass filter to limit bandwidth and improve noise performance [11].

The output voltage of the logarithmic amplifier is quantized by a ramp ADC, as shown in the figure. The main disadvantage of this ADC is its slow speed. However, in this application, it was not a problem since the bottleneck in measurement time was the settling time for the log TIA while measuring small currents. The clock is currently generated by a microprocessor and is limited to 25 MHz, resulting in an average conversion time of 500 μ s, which should decrease in proportion to clock frequency. The digital word is sent to a microprocessor that implements the programming algorithm over a serial peripheral interface (SPI). The combination of the logarithmic TIA and the linear ADC form a floating-point current-measuring ADC that achieves a thermal noise limited accuracy of 9.5 floating-point bits which increases to around 11 bits with averaging.

A set of 40 FGs are programmed to currents ranging from approximately 6 pA to 20 μ A using a version of the algorithm shown in [12]. The experiment was run 15 times choosing a random set of devices from a pool of over thousand devices. The average of the absolute error in achieving the current targets is

plotted in Fig. 4(c). The average error is 2.14% for this range of currents and reduces to below 1% if currents higher than 100 pA are considered.

Another important improvement in programming is introduction of row-parallel programming for switches. The rows of the FG array are selected by a decoder but the columns are selected using a shift register which enables selecting multiple columns per row. This leads to switch programming time given by $N_{rows} \times 1$ ms.

The last component of programming is the global erase of FG devices by electron tunneling. This process takes 25 s for all CAB devices and 9 s for all switch elements.

E. I/O Pad and Scanner Shift Register

Special bidirectional I/O pads have been incorporated in this IC which have buffer amplifiers capable of driving high capacitive loads when enabled. Their bandwidth is determined by a programmable FG device. For a total bias current of 2.1 mA (including biasing circuits), the corresponding amplifier (designed following [13]) achieves a unity gain bandwidth of 48 MHz, a dc gain of 103 dB, and a phase margin of 70° while driving a capacitive load of 15 pF in SPICE simulations. Also, an analog 16-bit shift register is available to scan through and observe different lines, allowing the user an option to debug their circuit almost in a SPICE-like fashion.

III. SOFTWARE INTERFACE

Configuring the FPAA to implement a particular circuit requires turning ON a certain set of switches and accurately programming some FG elements for biases. A software tool chain has been developed to enable this task. Fig. 5 shows a graphical description of the software flow. A library containing different circuits (e.g., FGOTA, multiplier, and peak detector)

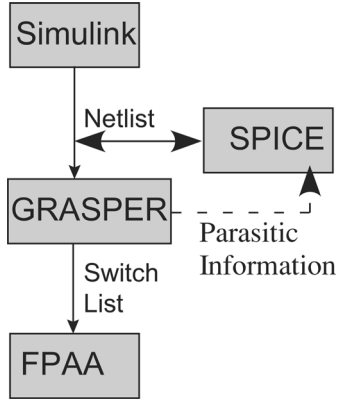


Fig. 5. Simulink. Flow of the software infrastructure is shown. A simulink level description is first translated to a Spice netlist and then converted to a list of switches on the FPAA. The tool for mapping a netlist to the FPAA also provides information on routing parasitics that may be used to manually tune the parameters.

is used to create a larger system in Simulink, a software product by The Mathworks. A first code (sim2SPICE [14]) converts the Simulink description to a Spice netlist, while a second one (GRASPER [15]) compiles the netlist to switch addresses on the chip. A Spice file can also be a direct input to GRASPER. The conversion of netlist to FPAA switches involves two parts—placement and routing (similar to a digital VLSI flow). The algorithm for placement tries to maximize the possibility of local wire usage while the routing algorithm is based on a maze routing approach [16] based on Dijkstra’s shortest path algorithm. GRASPER also provides a parasitic annotated post-routing netlist that can be used to retune the circuit parameters for desired performance.

Fig. 6(a) shows an example of a Simulink-level circuit description while Fig. 6(b) shows the schematic of the circuit. The vector matrix multiplier [17] enables multiplying a vector of input signals with a matrix of fixed coefficients/weights and will be described in detail later in the paper. The schematic shows a 2-input 1-output VMM with the output given by

$$I_{\text{out}} = w_1 I_{\text{in1}} + w_2 I_{\text{in2}} \quad (1)$$

where w_1 and w_2 are set by difference in charge on the gates of the M_i and M_o transistors. This is the simple case where the weight matrix is just a vector and the output is the projection of the input vector on the weight vector. The output currents are converted to a voltage using a TIA where the resistor is implemented using an FGOTA resulting in $R = 1/G_m$. The input currents are also created using FGOTA circuits. Fig. 6(c) shows the output of the TIA plotted against the input voltages applied to the FGOTA elements to create I_{in1} and I_{in2} . The two different slopes representing w_1 and w_2 are obtained by sweeping only one input. Sweeping both the inputs results in a slope that is nominally equal to $w_1 + w_2$. The offset in the curves results from FGOTA offsets which can be corrected (shown later).

Fig. 7(a) plots the circuit of a second-order low-pass filter based on a resonator topology. FGOTA elements are used here to increase linear range. This circuit is used to demonstrate the

parasitic capacitance prediction feature. The transfer function of this circuit is given by

$$H(s) = \frac{V_{\text{out}}(s)}{V_{\text{in}}(s)} = \frac{G_{m,\text{in}}/G_{m,\tau}}{1 + \frac{sC_2 G_{m,Q}}{G_{m,\tau}} + \frac{s^2 C_1 C_2}{G_{m,\tau}^2}}$$

$$f_0 = \frac{G_{m,\tau}}{2\pi\sqrt{C_1 C_2}}$$

$$Q = \sqrt{C_1/C_2} \frac{G_{m,\tau}}{G_{m,Q}}. \quad (2)$$

In this implementation, both $G_{m,\tau} = G_{m,Q} = 15.5$ nS while $C_1 = C_2 = 0.5$ pF, resulting in $Q = 1$ and $f_0 = 4.95$ kHz. Fig. 7(b) plots the theoretical frequency response of the circuit for these nominal values. However, the measured frequency response has a smaller $f_0 = 850$ Hz because of parasitic capacitances. The measured Q is 1.05 which is close to the expected value. Using the back-annotated parasitic values obtained from GRASPER, the theoretical value becomes $f_0 = 480$ Hz, which is close to the measured value. Thus, using these parasitic capacitance values the G_m values can now be modified to get the desired frequency response. It should be noted that the Q -mismatch is because of a mismatch in the measured G_m values due to the mismatch between the indirect programming transistor and the direct transistor [10] in the circuit. This can be corrected iteratively or by characterizing and storing this mismatch for every FG device on the chip.

IV. CAB ELEMENTS: CHARACTERIZATION AND SIMPLE CIRCUITS

Here, we describe the performance of the different CAB elements by configuring the chip into different simple circuits. In all of the experiments, the power supply of the chip is maintained at 2.4 V. A printed circuit board (PCB), shown in Fig. 8, has been designed for testing and demonstration. USB connection serves as the communication link with the host PC and also provides power to the board. This makes the entire setup portable. Next, we describe several small circuits demonstrating the operation of the CAB elements.

A. FGOTA

One of the most versatile circuit elements on the chip is the FGOTA [18]. The circuit is shown in Fig. 9(a). It consists of a differential amplifier followed by a push–pull output stage. The bias current of the amplifier can be programmed using an FG device (M1). The differential pair transistors (M2 and M3) are also FGs, which allows the user to program a desired input offset voltage. The input is applied to the differential pair through a capacitive divider that has a 1:9 ratio. This allows a wider input linear range by effectively degenerating the transconductance. The advantage of this method over other degeneration schemes is that the capacitors add virtually no noise. The DC gain of this circuit varies from 27 to 19 as the bias current is varied from 1 nA to 3 μ A. In future versions, cascode transistors will be used in the output stage to improve the output impedance and dc gain.

Since arbitrary input offsets (limited by the precision of programming charge) can be stored in the input differential pair,

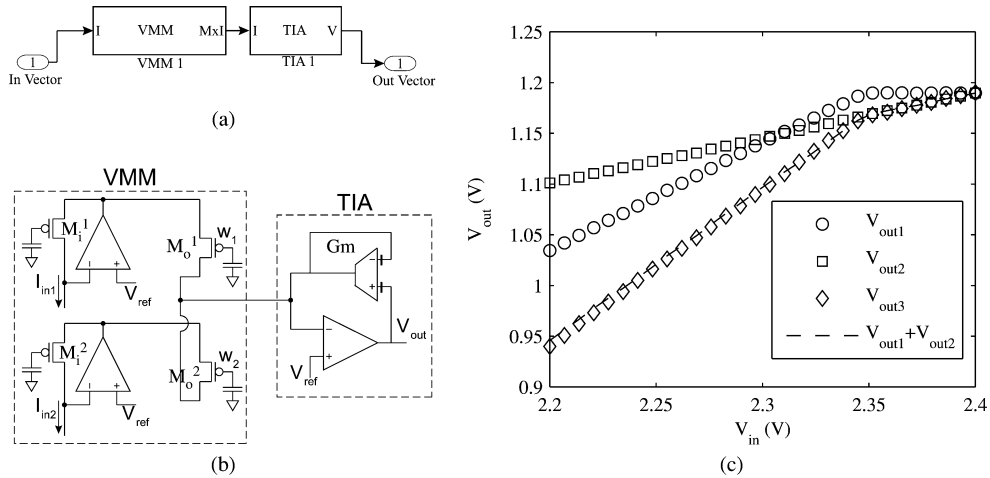


Fig. 6. Simulink example. (a) Block diagram description of a vector matrix multiplier (VMM) followed by a TIA. (b) Circuit schematic of the single ended VMM followed by a TIA where a wide-linear-range transconductor is used as a resistor. (c) Measured data from the FPAA showing the input multiplied by different weights.

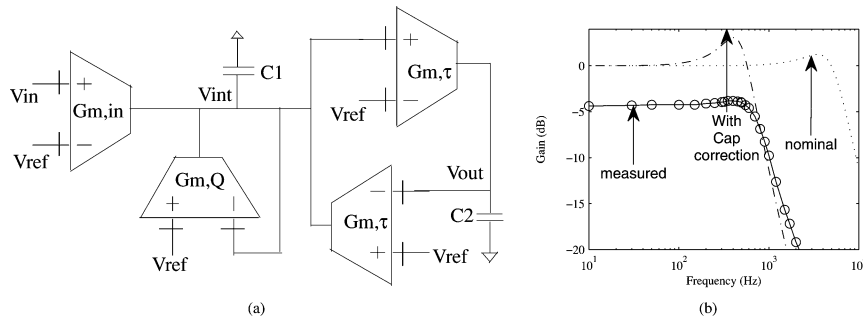


Fig. 7. Gm-C filter. (a) Circuit diagram for a second-order low-pass filter based on a resonator topology. (b) Measured corner frequency from the FPAA matches well with theory simulation obtained after including the effect of parasitic capacitances and G_m mismatch.

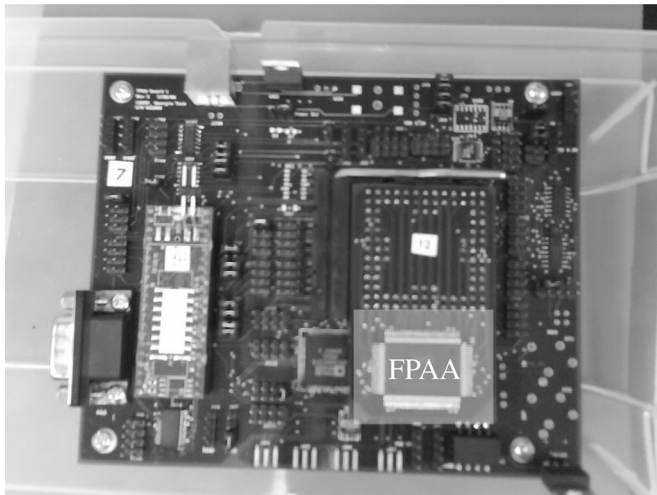


Fig. 8. PCB. Test setup for the chip includes a microprocessor, voltage regulators, and data converters on the same board. USB is used for communication with the PC and also for the board's power supply.

the FGOTA can be used as a comparator for a flash ADC and eliminates the need for a resistor ladder. Fig. 9(b) shows a case where nine different offset values are set by programming the

charge difference. Fig. 9(c) shows the relation between the programmed difference in floating-gate voltage and the measured trip-point of the comparator. The average deviation from linearity is 5.8% and can be attributed to errors in programming, extrapolating the floating-gate potential and measuring the trip point from the high gain curve. The power dissipation of the circuit is $9.6 \mu\text{W}$.

The widening of the input linear range is depicted in Fig. 10 by plotting the transconductance of the block with respect to input differential voltage. Assuming subthreshold operation, the $I-V$ relation is

$$I_{\text{out}} = I_{\text{bias}} \tanh \left(\frac{\kappa \alpha (V_{\text{in}+} - V_{\text{in}-})}{2U_T} \right) \quad (3)$$

where α is the attenuation factor due to the divider, I_{bias} is the bias current of the stage, κ is the coupling of the gate to the channel of a subthreshold MOSFET, and U_T is the thermal voltage. The operation region for the input differential pair is weak inversion for bias currents less than 500 nA , strong inversion for currents greater than $1.5 \mu\text{A}$ and moderate inversion for intermediate current values. Fig. 10 plots the transconductance when the bias current is varied from approximately 1 nA to $3 \mu\text{A}$. The linear range for 5% degradation in G_m increases from 0.489 to 1.347 V over this range of currents.

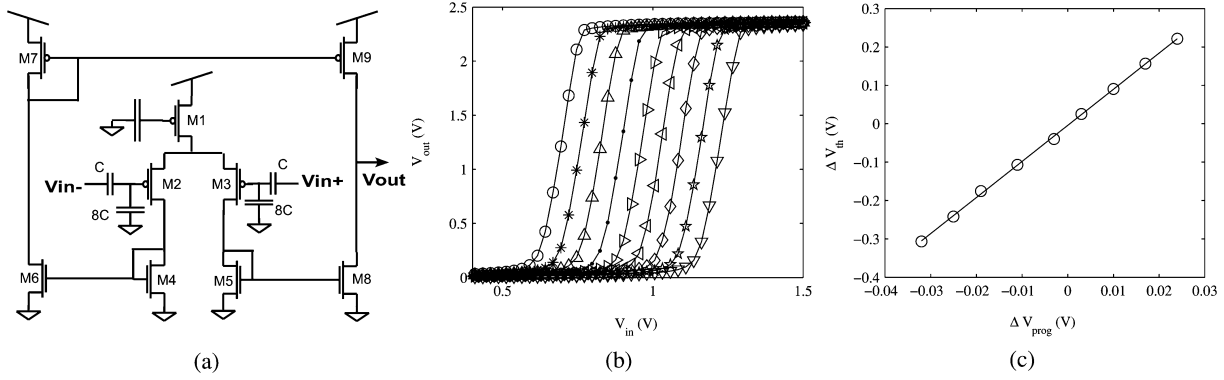


Fig. 9. Variable offset comparator. (a) Schematic of a floating-gate input OTA whose input offset can be programmed using the FG inputs. It is used as a comparator in this experiment. (b) Different values of programmed charge difference on the differential inputs leads to different measured trip points for the comparator. (c) Relation between the comparator trip points and the programmed charge difference shows an average deviation of 5.8% from linearity.

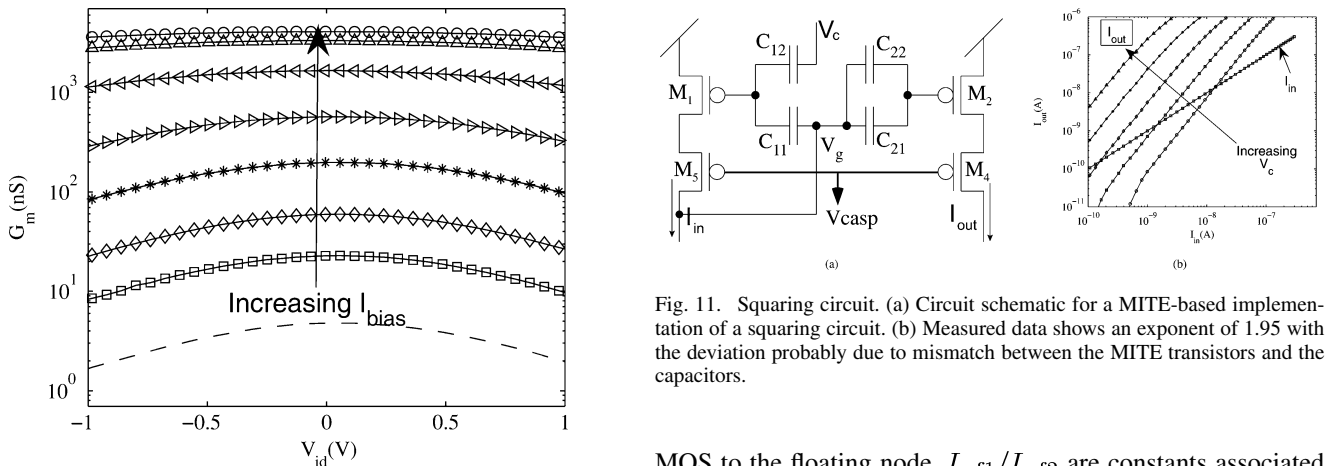


Fig. 10. Wide input linear range. A capacitive divider is placed before the input of a traditional differential pair to provide an effectively wider linear range. This circuit has a measured linear range varying from 0.489 to 1.347 V for 5% degradation in transconductance when the bias current is varied from 1 nA to 3 μ A.

B. Current-Mode Translinear Circuits

Translinear circuits introduced by Gilbert are very popular for its versatility in implementing signal processing functions. In particular, multi-input translinear elements (MITEs) [19] have been shown to successfully synthesize various static and dynamic functions. This FPAA chip has a couple of two-input MITE elements in every CAB of type 1. Fig. 11(a) shows the schematic of a simple circuit to implement the static function of squaring the input. All of the capacitors are nominally equal to 110 fF. The output current is measured using an off-chip pico-ammeter. The output current is given by

$$I_{\text{out}} = I_{\text{ref2}} \left(\frac{I_{\text{in}}}{I_{\text{ref1}}} \right)^{1+a/b}$$

$$a = -\frac{\kappa_2(C_{21} + C_{22})}{C_{T2}U_T} + \frac{\kappa_1(C_{11} + C_{gd1})}{C_{T1}U_T}$$

$$b = -\frac{\kappa_1(C_{11} + C_{gd1})}{C_{T1}U_T}$$

$$C_{Tj} = C_{j1} + C_{j2} + C_{gj}, \quad j = 1, 2 \quad (4)$$

where quantities with subscripts 1 or 2 refer to parameters for M1 or M2 and C_g denotes the capacitance contributed by the

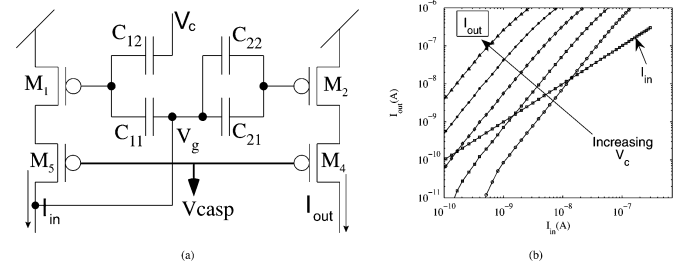


Fig. 11. Squaring circuit. (a) Circuit schematic for a MITE-based implementation of a squaring circuit. (b) Measured data shows an exponent of 1.95 with the deviation probably due to mismatch between the MITE transistors and the capacitors.

MOS to the floating node. $I_{\text{ref1}}/I_{\text{ref2}}$ are constants associated with M1/M2 and are controlled by their respective FG charges. I_{ref1} is also controlled by V_c . For nominally matched parameters of both devices and ignoring C_{gd1} , “a” and “b” are equal leading to a squaring circuit.

Fig. 11(b) plots the output current against the input current for several values of V_c . The average slope of the plots is 1.95 with the error resulting from mismatch. The bandwidth of this circuit depends on the magnitude of dc bias currents and attains a value of 21 kHz for an input bias current of 33 nA and output current of approximately 1 μ A. Many other static and dynamic functions can be synthesized but are not shown due to lack of space.

C. Programmable Offset Buffer

An FGOTA circuit configured as a voltage buffer has been placed in the CAB due to its frequent need. The circuit is shown in Fig. 12(a). The ratio of C2 and C1 is 8, as mentioned earlier. Since an offset can be programmed by setting a desired charge difference on the floating nodes, this can serve as a level shifting buffer with the level shift being approximately nine times the programmed offset voltage. The offset can also be reduced to zero (within programming precision) which leads to a reduction in the second harmonic signal at the output. Fig. 12(b) plots the output spectrum of the buffer with a 10 kHz sinusoid at its input. The output is plotted without and with offset correction. The spurious free dynamic range (SFDR) is 65.2 dB after correction, 19 dB better than earlier.

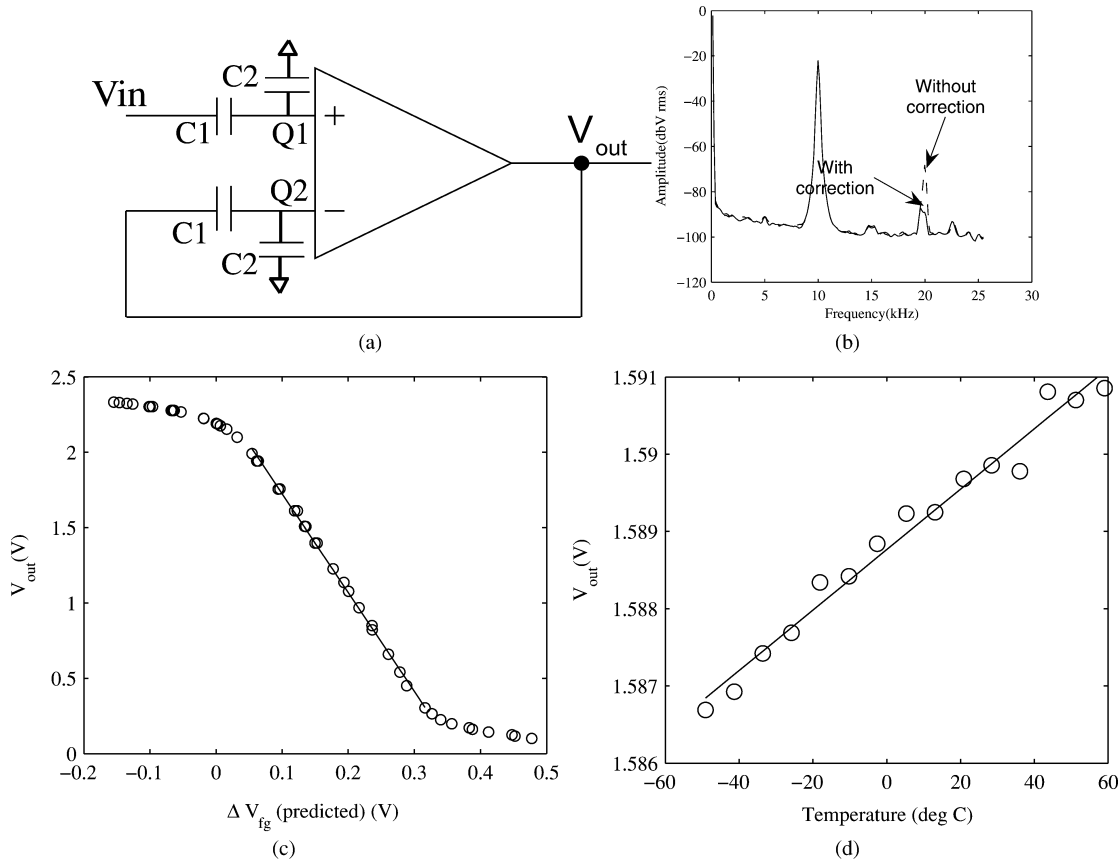


Fig. 12. FGOTA buffer. (a) Circuit schematic of the FG input buffer. (b) Offset voltage reduction leads to a reduction in second harmonic at the output of the buffer. Measurements show an improvement of 19 dB. (c) The programmable input offset voltage leads to a level shift in the output. This can be used as a reference voltage generator with V_{in} connected to V_{dd} . Measured reference voltage is linearly related to programmed offset. (d) Since the FG charge does not change appreciably with temperature, the reference has a low TC. Measured TC is equal to 24.6 ppm.

Because of the level shifting properties mentioned earlier, the output voltage can be set to any arbitrary value within a range of voltages even if the input is fixed to V_{dd} . This method is used to create a reference voltage generator. The capacitive divider ensures that generating a wide range of reference voltages does not need a wide ICMR for the amplifier. Fig. 12(c) plots the output reference voltage against the programmed offset voltage (predicted from current measurements of the FGs). In this experiment, Q1 was fixed to a value while Q2 was varied. The curve saturates near the power rails possibly due to output swing limitations. Within the range of 0.3–1.99 V, the average deviation from linearity is 1.6%. The power dissipation in this case is 9.6 μ W and can be reduced by reducing the bias current.

Since the FG charge does not vary appreciably with temperature [7], this voltage reference also exhibits good temperature stability. Fig. 12(d) plots the measured temperature behavior for a particular reference voltage over a range of -50°C to 60°C . The measured temperature coefficient (TC) over this range is 24.6 ppm. Assuming perfect matching between the capacitors and no charge loss from the floating node, the TC of the reference can be shown to be

$$\text{TC}_{V_{\text{ref}}} = \frac{1}{V_{\text{ref}}} \frac{dV_{\text{ref}}}{dT} = -\frac{1}{C_1} \frac{dC_1}{dT} = -\text{TC}_{C_1}. \quad (5)$$

In practice, the temperature performance may degrade further because of the variation of the DAC voltage that supplies the

voltage at the end of the capacitor C_2 [shown as a small-signal ground in Fig. 12(a)] and due to variation of the amplifier's gain.

D. Folded Gilbert Multiplier

The Gilbert multiplier is a widely used analog component useful for mixers, variable gain amplifiers (VGAs), automatic gain control (AGC), and many more applications. However, the stacking of multiple differential pairs leads to voltage headroom issues in a traditional Gilbert cell. This has been solved by folding the signal currents [20], [21]. We employ a similar approach as shown in Fig. 13(a). The cascode biases are generated following [22]. In the figure, I_b refers to the current in the bias generation circuits. V_1 and V_2 are the two differential inputs to the multiplier. The multiplier block produces differential output currents which can be converted to a single ended voltage using a FG current mirror (M14 and M15). Fig. 13(b) plots the measured output voltage against differential input voltage V_{in1} for several fixed values of V_{in2} . For this case, $I_b = 1$ nA, leading to a power dissipation of 230 nW. The maximum deviation from linearity over a differential range of 2 V is 1.5%.

Next, we show an AGC circuit as an example application of the multiplier. The schematic of the AGC is shown in Fig. 14(a). The multiplier is used as a VGA with the gain controlling input being set by feedback. The feedback loop comprises a peak detector, a low pass filter and a high gain amplifier. The desired amplitude of the output is indicated by the signal V_{amp} .

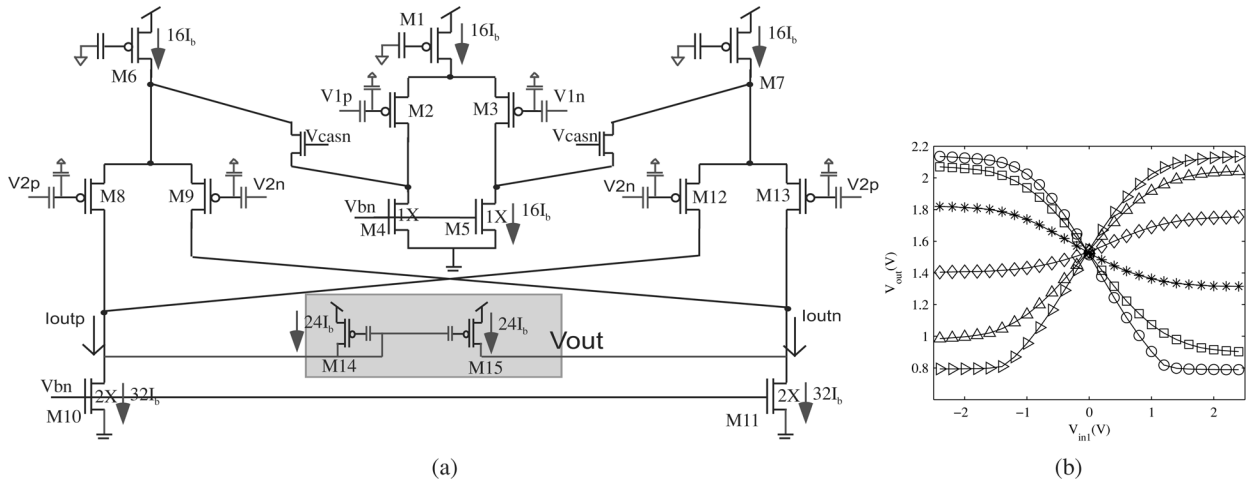


Fig. 13. Gilbert multiplier. (a) Circuit schematic for a folded Gilbert multiplier. M14 and M15 forms an FG current mirror that can be optionally added to convert the output currents to a single-ended voltage. (b) Measured output voltage for sweeping the differential input V_{in1} for different values of V_{in2} . The measured linear range is 2 V differential for a maximum error of 1.5%.

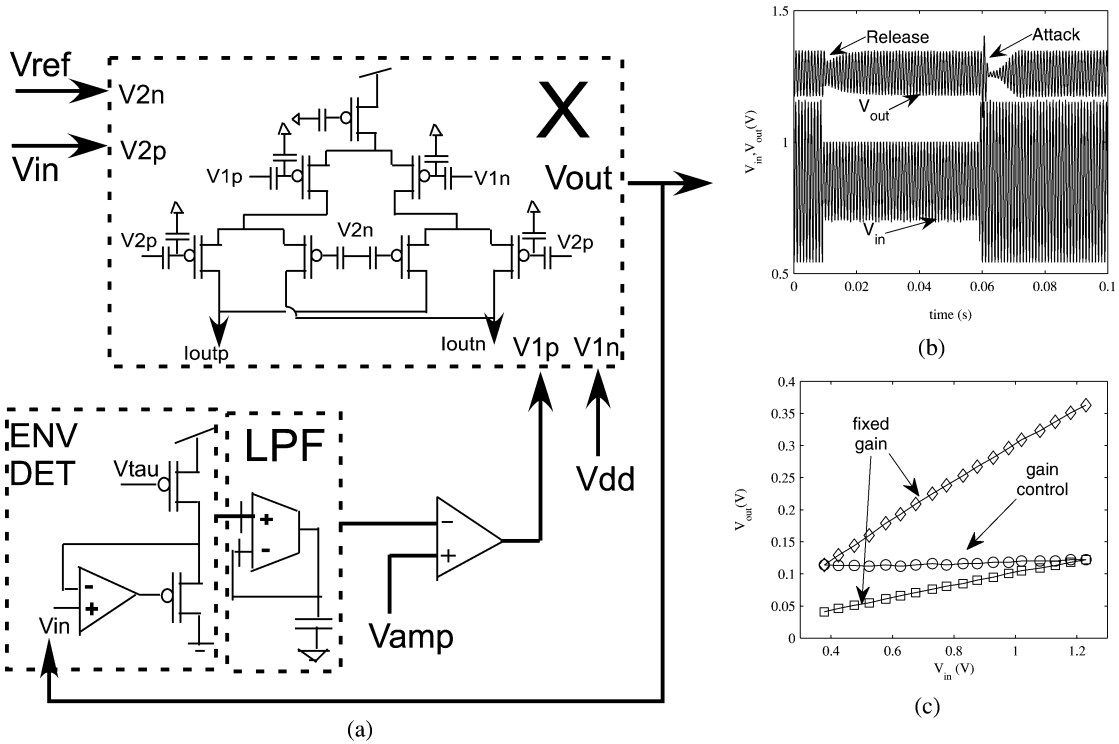


Fig. 14. AGC. (a) Circuit schematic for an AGC system. (b) Measured transient response of the AGC to large variations of input amplitude. The attack and release times are approximately 11 ms. (c) Measured gain compression curves showing a maximum compression of 28 dB.

Fig. 14(b) shows measured output waveforms when the input is an amplitude modulated sinusoid. The output amplitude at steady state is relatively constant. The time constants for recovery in response to amplitude steps are around 11 ms. The whole circuit consumes approximately $3.76 \mu\text{W}$ of static power excluding the power consumed in buffering the signal off-chip. Fig. 14(c) shows the measured gain compression characteristics. A fixed high gain and a fixed low gain characteristic are also shown for comparison. The AGC achieves 28 dB of compression for the largest input. The total variation of output amplitude is approximately 10 mV over the whole range.

E. Vector Matrix Multiplier

Unlike a Gilbert multiplier that computes the product of two time-varying signals, many applications require computing the dot product (or projection) of a time-varying input vector with a fixed coefficient matrix. A fully differential circuit [17] to achieve this is shown in Fig. 15(a). The OTAs are biased at $2 \mu\text{A}$ of current. The FG devices in the circuit are routing elements, a classic example of a powerful computation being performed on the switch matrix. This circuit implements a 1×1 VMM, i.e., it multiplies a differential input current signal with a differential weight to produce a differential output current. The core of the

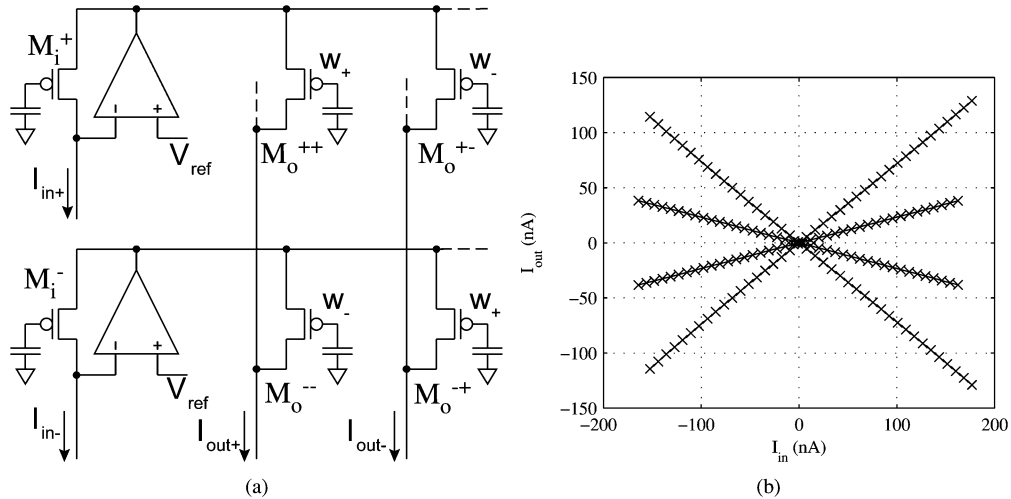


Fig. 15. Vector matrix multiplier. (a) Differential circuit for 1×1 VMM to multiply an input current with a fixed weight is shown. (b) Measured data from the circuit for two different weight values.

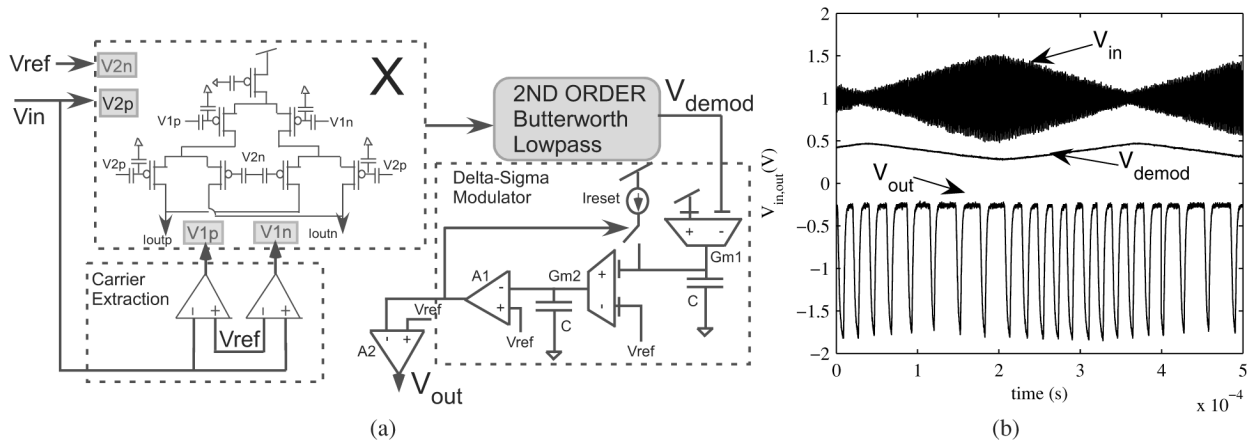


Fig. 16. AM baseband. (a) Circuit for demodulation of an amplitude modulated signal and subsequent filtering and conversion to a digital bit stream. (b) Measured transient data for the whole system when the input is a 3-kHz triangle waveform modulating a 500-kHz carrier.

circuit is an FG-based current mirror (e.g., M_i^+ and M_o^{++}). The relation between input and output currents is given by

$$I_{out} = I_{in} e^{\frac{\Delta V_{fg}}{U_T}} \quad (6)$$

where ΔV_{fg} is the difference in the FG charge between the two transistors. To obtain four quadrant multiplication, four such single-ended multiplications are done. The resulting differential output is given by

$$I_{out+} - I_{out-} = (w_+ - w_-)(I_{in+} - I_{in-})$$

$$w_{\pm} = w_0 \pm \Delta w, \quad I_{in\pm} = I_{in0} \pm \Delta I_{in} \quad (7)$$

where I_{in0} and w_0 are nominal or bias values. Since the output is a current, summing many such outputs to compute the projection of an input vector on a weight vector can be achieved by KCL.

Fig. 15(b) plots measured output currents from this circuit for four different weight values, two of which are of opposite signs but same magnitude. The average deviation from linearity is 7% with the major source of error being the overlap capacitors coupling onto the FG.

V. LARGER SYSTEMS

A. AM Receiver

A receiver for an amplitude modulated signal has been implemented on the FPAA. Fig. 16(a) depicts the circuit diagram for the receiver. A synchronous demodulation scheme is used to extract the modulating signal. The Gilbert multiplier is used to down-convert the modulated signal. The carrier signal is extracted from the received signal itself by using two comparators to threshold the received signal. The comparators are connected in reverse polarity to generate a pseudo differential signal. The resulting square wave signals are used to demodulate the received signal. Since a square wave at the carrier frequency is used to demodulate, a low pass filter is needed to sufficiently suppress the higher harmonic signals in the demodulated message. This is not a problem provided the modulating and modulated signals are sufficiently separated in frequency. The output of the low-pass filter (7-kHz bandwidth) is digitized using a second order continuous-time delta sigma. The integrations of the input signal are performed using two Gm-C integrators composed of FGOTA devices. Finally, the output of the second integrator is digitized by a comparator that acts like a 1-bit quan-

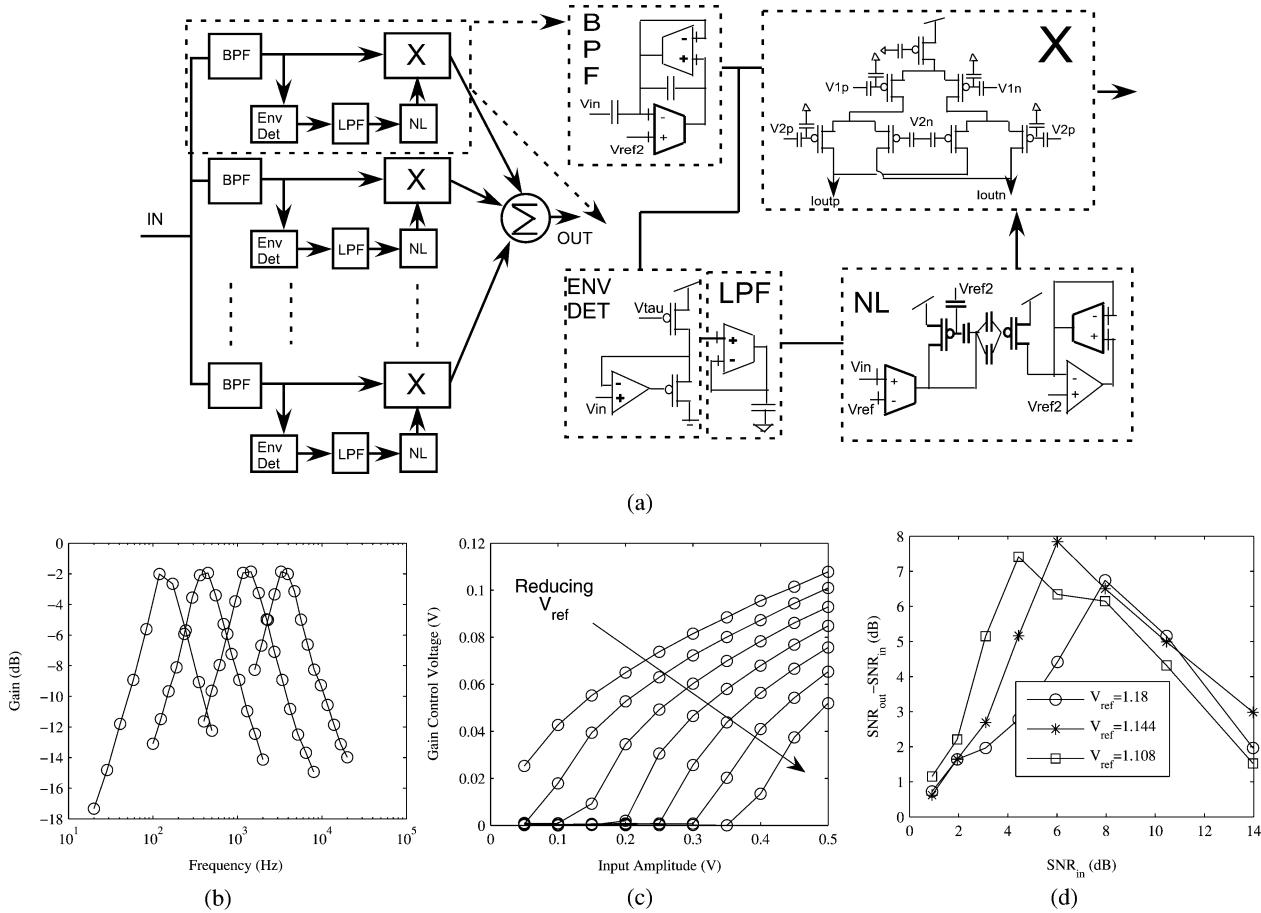


Fig. 17. Speech processor. (a) Circuit for processing one subband of a noisy speech signal. (b) Programmability of the bandpass filter. (c) Gain-controlling voltage input to the Gilbert multiplier for a range of V_{ref} values. (d) Output SNR for the circuits is around 7.5 dB better than input SNR.

tizer. This signal is used to add a reset current to the first integration node. The output digital signal is buffered using another comparator. Thus, there are no clocks in this system, and the delta-sigma acts as a continuous-time modulator. The bit stream can be clocked and stored externally if desired. The dominant sources of error are the finite output impedances of the transconductors and the current sources.

Fig. 16(c) shows the output of the full system when the input is a 500-kHz carrier modulated by a 3-kHz triangle wave. The demodulated and filtered waveform shows the triangle waveform while the output of the delta sigma modulator is a pulswidth modulated signal based on input amplitude. The static power dissipation of this circuit is around 28 μ W excluding analog and digital buffers.

B. Analog Speech Processor

The components in this FPAA are suited for a variety of speech-processing algorithms. Here we show an example of an algorithm for enhancing the SNR of a noisy speech signal. Fig. 17(a) plots the schematic of the system along with details about one subband of the system. The algorithm is inspired by the physiological basis of hearing and is detailed in [28], [29]. Here, we only mention the salient points of the algorithm for completeness.

An acoustic signal can be represented as

$$s(t) = \sum_n e_n(t)v_n(t) \quad (8)$$

where $e_n(t)$ is the slowly varying envelope of speech and $v_n(t)$ is the rapidly varying speech excitation component in the n th channel. The de-noising algorithm suggested by [29] requires nonlinear processing of the envelope in each channel. The output of the nonlinear block is related to the input as follows:

$$\hat{e}_n(t) = \beta e_n^\alpha(t). \quad (9)$$

Methods for estimating α and β are given in [29]. Intuitively, the nonlinear gain applied to the original subband signal is like a $1 + \tanh(x - x_0)$ function with x_0 depending on the input noise level. For larger noise, the algorithm chooses a larger x_0 such that the noise is maximally suppressed while the signal still has a gain. In our implementation, the combination of an OTA and the rectifying action of a MITE based current mirror is used to create one half of a tanh function while V_{ref} sets the parameter x_0 . The saturating characteristic of the other half of the tanh is approximated by a current mode square root circuit. We are currently modifying this circuit to allow for automatic generation of V_{ref} .

TABLE II
PERFORMANCE COMPARISON OF FPAA DESIGNS

Ref.	Process	Area	Num. of CABs	CAB elements	Num. of params.	Features	Application
This work	0.35 μm	9 mm^2	32	Prog. offset and bias OTA and multiplier, prog. bias MITE, MOSFET, Capacitor, T-gate	$\approx 50\text{k}^1$	Floating-gate	Analog signal proc.
[23]	0.25 μm	1 cm^2	16	Integrator, multiplier, logarithm, exponent	416	log-domain current-mode	Analog computer
[2], [24]	0.13 μm	1 mm^2	7	7 digitally tuned transconductors	55-58	Hexagonal layout	Filter design
[1]	2 μm	>18.75 mm^2	10 ²	Digital and analog tuned Gm and capacitors	80	Automatic tuning	Filter design
[25]	-	-	4	Switched capacitor filter, differential amp., SAR, Reference generator	16	Switched capacitor	Analog sensing and processing
[26]	2.4 μm	20 mm^2	4	Programmable gain, integrator/comparator	16	Buffers for switches	Analog signal proc.
[27]	1.2 μm	21.62 mm^2	5	Programmable bias integrator, amplifier, attenuator	5	Current mode	Filter design

¹ All switches can be programmed in an analog way leading to around 50000 parameters. The CABs have 460 parameters.

² Minimum complexity of CAB considered to be 4 programmable transconductors similar to this work.

TABLE I
TABLE OF PARAMETERS

Process	0.35 μm
Die Size	3mm \times 3mm
Power Supply	2.4V
Number of CABs	32
Switch programming time	$N_{\text{rows}} \times 1 \text{ ms}$
Bias programming time	50 ms/element
Programming accuracy and range	9.5 bits over 6 pA to 20 μA

We present measured data for one sub-band of the proposed system. Fig. 17(b) shows measured frequency responses from the tunable bandpass filter based on [30]. This shows that the results from this sub-band can be easily obtained for other sub-bands also. The total current consumption for the four cases are 1.5, 6, 24, and 96 nA. Fig. 17(c) shows the input differential voltage on the gain controlling input of the Gilbert multiplier for different V_{ref} values. The nonlinear processing results in almost zero gain for small signals while larger signals get larger gain. Fig. 17(d) shows the output SNR improvement of around 7.5 dB over the input SNR. Also, for different input SNR values, the

optimum point is reached for different V_{ref} values as expected. The static power consumption of this circuit is around 34.5 μW with 28.8 μW being dissipated in the peak detector and the TIA. Optimizations for reducing the bias current of these elements are being done currently. The equivalent digital computation for one subband in this case is approximately 500 kMAC (assuming sampling at 40 kps) leading to a computational efficiency of 14.5 kMAC/ μW which is an order of magnitude better compared to an efficiency of around 2 kMAC/ μW for digital signal processors [31].

VI. CONCLUSION

FPAA devices have come a long way since the introduction of the first few prototypes [32]. The RASP 2.8 generation of FPAA devices provide a powerful platform for prototyping and implementing large-scale signal processing applications. Table I presents the parameters for this chip. The programmable switch matrix composed of FG devices shows excellent isolation and can be readily utilized in computation. Programming times are around 50 ms for accurate biases and 1 ms per row of switches. Different levels of routing allow implementation of high-performance circuits while allowing for fast turn-around times. A comparison with other FPAA chips is presented in Table II. To the best of the authors' knowledge, there is still no concrete performance metrics to compare different FPAA designs. One method that may be used in the future is to have a number of benchmark applications (filters, vector-matrix multiplication

etc.) for which power per unit computation or speed may be compared. In that case a possible figure of merit (FOM) is

$$\text{FOM} = \frac{\text{Number of parameters}}{\text{Area}} \times \frac{f_{\max} L_{\min}^2}{f_T} (\text{MMAC}/\mu\text{W})(\text{SNR}) \quad (10)$$

where f_{\max} , SNR, and MMAC/ μW are the maximum bandwidth, SNR, and power efficiency obtained for the benchmark applications while f_T and L_{\min} are features of the VLSI process used. The chip we present is the largest designs reported with around 50,000 programmable analog parameters and has significantly more variety in CAB components compared with others. We hope to use this chip for prototyping and implementing systems for a variety of applications ranging from speech processing to sensor interfacing.

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