A Large-Scale Reconfigurable Smart Sensory Chip

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***Abstract*— The Reconfigurable Smart Sensory Chip (RSSC) is a powerful tool for fast prototyping sensory microsystems. Innovative design ideas can be quickly realized and tested in hardware without doing time-consuming and expensive silicon fabrication. The RSSC is a large-scale floating-gate based IC containing 8 universal sensor interface blocks, each of which can be configured for voltage sensing, capacitive sensing, or current sensing, and 28 configurable analog blocks. The outputs of the interface circuits can be multiplexed out in a time-division sequence or can be routed to the configurable analog blocks for further analog signal processing or data conversion. With more than 50,000 programmable elements and on-chip programming circuitry, RSSC is an extremely powerful tool to develop and test a great variety of smart sensory microsystems in minutes.**

I. Motivation

The advancements in silicon technologies have not only made electronic devices smaller and faster but also have enabled the fabrication of a great diversity of micromachined transducers. A large number of external signals received from multiple sensors and the powerful computational capabilities provided by the integrated electronics create great opportunities to develop advanced "smart" sensory microsystems with features that previously could not be achieved. Some autonomous microsystems can interact with the environment without explicit user involvement. These sensory microsystems have attracted a lot of research interest and are expected to bring positive and revolutionary impacts on our daily lives.

At the same time, circuit and sensor designers also have to face several new and challenging obstacles to bring these products to market quickly. As a variety of sensors have been developed, the demand for corresponding interface circuits has also grown rapidly. A design-test cycle can easily take several months in conventional ASIC design, and each new sensor would require its own new interface integrated circuit. A reconfigurable sensory chip that can synthesize different interface circuits in minutes would be an extremely useful tool for fast prototyping new sensors or new sensory systems and would significantly reduce the costs and time-to-market of new microsystem development.

Another challenge in microsystem design is the severe power constraints. The available power and the heat dissipation capabilities are all limited by the small form factor of these smart sensors. Low-power operation can prolong the lifetime of a system, or it can decrease the recharge frequency. These more stringent power constraints determine both the functionality and the feasibility of these microsystems.

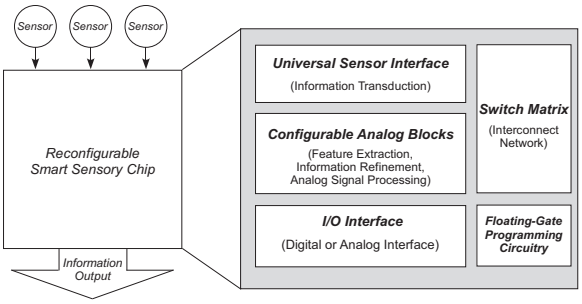

Fig. 1. The block diagram of a Reconfigurable Smart Sensory Chip.

Analog signal processing has been shown as a promising approach to addressing these power issues because of its superior power efficiency. Furthermore, if the meaningful information can be refined using analog signal processing techniques at the sensor interface, the bandwidth for the subsequent transmission, conversion, and processing can be significantly reduced. As a result, the system can achieve a much higher efficiency and overcome the difficulties associated with the power constraints.

Although analog signal processing plays a significant role in addressing the power issues of advanced sensory microsystems, analog design, especially analog signal processing, can be difficult and very time consuming. Analog circuit performance is vulnerable to fabrication imperfection using traditional analog design techniques. Therefore, an effective means to compensate for device mismatch and offsets, in the interface circuit as well as the sensor, is necessary. In conventional analog approaches, these techniques consume a significant amount of power and silicon area, which negate many of the advantages of analog signal processing. A lack of programmability and reconfigurability is a significant shortcoming of conventional analog systems, and is likely one of the major reasons that analog signal processing is not as popular as digital signal processing today. Recently, some field programmable analog arrays have been developed [1–3] to facilitate analog signal processing.

In this paper, we introduce a large-scale floating-gate based IC called the Reconfigurable Smart Sensory Chip (RSSC) that can address the aforementioned challenges. The block diagram of this chip is shown in Fig. 1. The RSSC is capable of interfacing with different kinds of sensors and can be programmed to perform arbitrary analog algorithms for different applications. Depending on the types of sensors employed in

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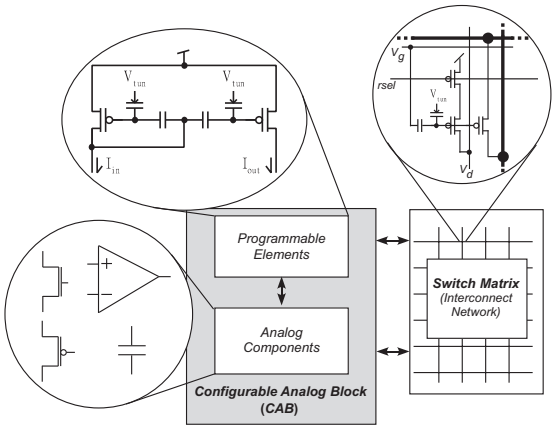

Fig. 2. The block diagram of a Reconfigurable Analog Signal Processor (RASP).

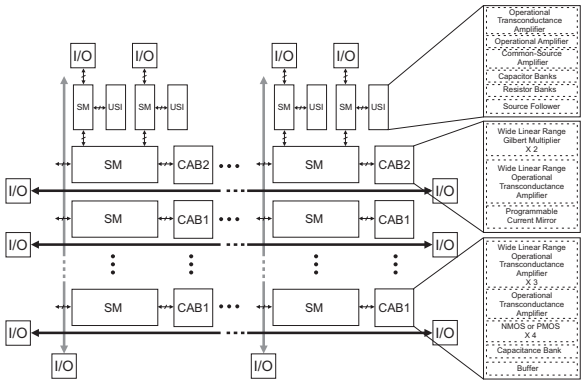

Fig. 3. The high-level architecture of the Reconfigurable Smart Sensory Chip (RSSC), which contains 8 USI and 4×7 CABs.

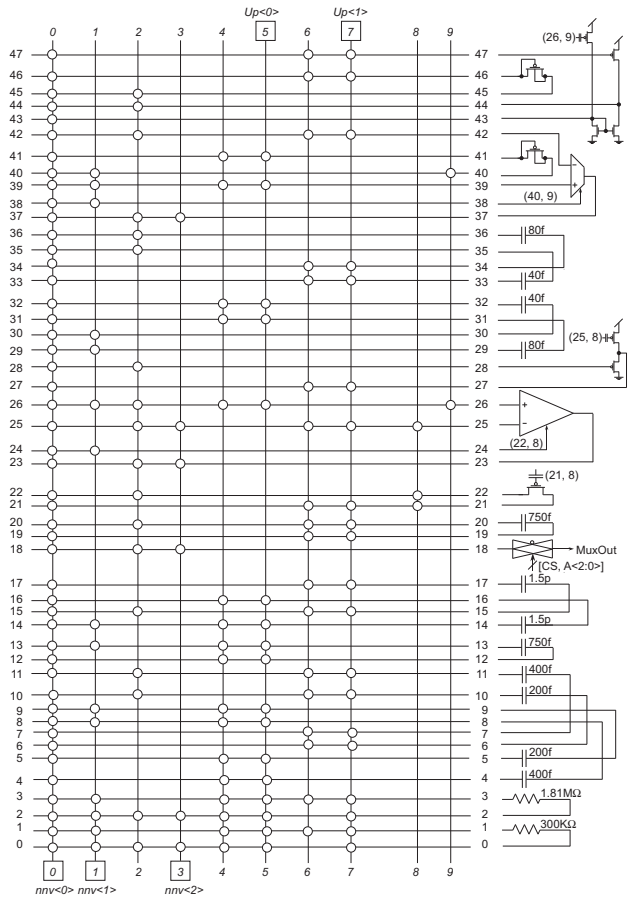

Fig. 4. The interconnect network and components of a USI block in the RSSC.

the system, appropriate interface circuits are synthesized in the Universal Sensor Interface (USI) blocks to transduce information received from the outside world. The components inside the Configurable Analog Blocks (CABs) can be configured for feature extraction, information refinement, or other analog signal processing tasks.

The reconfigurability of the chip is achieved by the Switch Matrix (SM) that connects component terminals to form different circuit topologies. The floating-gate charge programming circuitry is integrated into the chip for fast programming. Floating-gate charge storage techniques are utilized in this chip to set the bias and the bandwidth of the analog components and to compensate for device mismatch and circuit offset without consuming extra power. Therefore, this reconfigurable chip can perform highly power-efficient signal processing to facilitate the development of advanced smart sensory microsystems.

II. Architecture

The large-scale reconfigurable sensory chip demonstrated in this paper adopts the architecture of floating-gate based Reconfigurable Analog Signal Processors (RASPs) that are composed of switch matrices and CABs as shown in Fig. 2 [3]. The reconfigurability is mainly achieved through switch matrices that are composed of an array of floating-gate transistors. In this RSSC, an indirect programming transistor and a row-select transistor are employed to improve the programming isolation. The CABs are made up of analog components and programmable elements, which include current mirrors with programmable ratios and programmable current sources that can set the biases and the bandwidths of analog components.

The high-level architecture of the RSSC discussed in this paper is shown in Fig. 3. It has eight USI blocks at the frontend, so a single chip can interface with up to eight sensors of the same or different types. The USI can be programmed to be voltage sensing, current sensing, or capacitive sensing with a programmable transduction gain. The signals coming out of the USI blocks can either be multiplexed out of the chip in a time-division sequence or can be routed to subsequent CABs for further signal processing in parallel. Two different types of CABs are deployed in a 4×7 array. The major components in these CABs include wide linear range operational transconductance amplifiers (OTAs), Gilbert multipliers, transistors, and capacitor banks. Floating-gate techniques have been used to compensate for the offsets of these analog components, such as input pair and current mirror mismatch in the OTAs [4].

The components and the interconnect network in a USI block are shown in Fig. 4. To reduce the parasitic capacitance at the interface between the sensor and the RSSC, the floating-

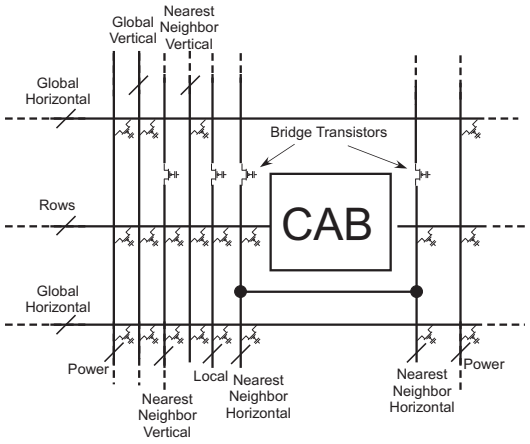

Fig. 5. The routing architecture of the RSSC.

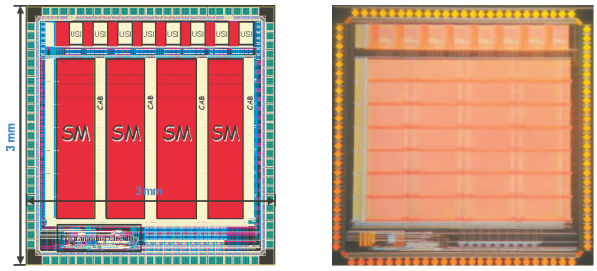

Fig. 6. The layout and the micrograph of the RSSC.

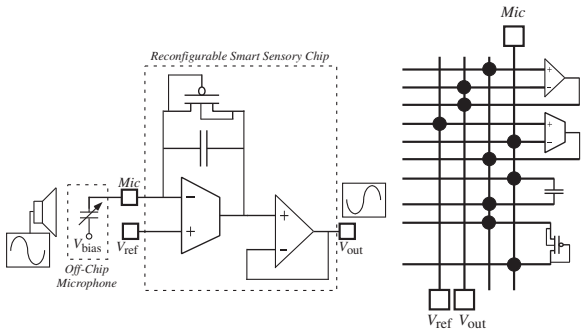

Fig. 7. The capacitive sensing charge amplifier synthesized in the RSSC and the test setup.

gate switches are not designed as a full crossbar interconnect network, as is the case with the RASP ICs. Instead, limited connectivity between USI components is provided, as illustrated by the circles, representing floating-gate switches, in Fig. 4. The components in a USI block include a self-biased cascoded common-source amplifier, a nine-transistor operational transconductance amplifier, an operational amplifier with an output stage, a transmission gate for multiplexing signals, a source follower, two sets of capacitor banks, two poly-resistors, two MOS-BJT nonlinear resistors, and a floating-gate pMOS transistor. With these components in a USI block, the RSSC can synthesize interface circuits for voltage sensing, capacitive sensing, or current sensing with programmable transduction gain.

To achieve high signal bandwidth and to improve power efficiency, the RSSC adopts a three-level routing architecture, which is used in the RASP 2.8 and is shown in Fig. 5. High speed circuits are synthesized by using components inside the same CAB using local connections. Nearest-neighbor connections are used to minimize the parasitic capacitance of circuits synthesized using components in adjacent CABs . Bridge transistors can be programmed to extend the connections if necessary. They allow local lines to be bridged between CABs facilitating variable length connections without incurring the capacitance penalty of long global lines with many switch transistors. A voltage buffer is used to isolate the pad capacitance from the CAB components. In this three-level architecture, routing between CABs can be accomplished with relatively low parasitic capacitance and can achieve bandwidths of approximately 6 MHz at around 100 nA of current. The achievable bandwidth within a CAB should be an order of magnitude higher.

The RSSC contains more than 50,000 programmable analog elements. To achieve fast programming speed, a programming circuitry that includes a logarithmic amplifier, analog-to-digital converter, two digital-to-analog converters, and a look-up table is integrated on chip. This programming circuitry is designed to program more than 200 floating-gate transistors per second [4]. With this programming infrastructure, a great variety of interface circuits and analog algorithms for different sensors and applications can be developed and tested in just minutes.

III. Measurement Results

A version of the RSSC has been fabricated in a $0.35\,\mu$m CMOS process and is under test. The chip area is $3\,m$m $\times$ $3\,m$m and the area of the programming circuitry is around $1\,m$m $\times$ $200\,\mu$m as shown at the lower left corner of Fig. 6. The die micrograph is also shown in Fig. 6.

A low-power high-SNR capacitive sensing charge amplifier [5] is synthesized in a USI block by enabling the proper floating-gate switches as shown in Fig. 7. The MOS-BJT nonlinear resistor is used to provide the DC path for the high impedance node. A commercial MEMS microphone sensor from Knowles Electronics is wire-bonded to the RSSC and a speaker is used to provide acoustic inputs at frequencies of 500 Hz, 1 KHz, and 2 KHz. The measured output waveforms as shown in Fig. 8 verify the functionality of the capacitive sensing interface circuit. The DC drift of the output waveforms is because of the external coupling from the testing environment and can be avoided by using a battery powered test bench with better shielding. Different feedback capacitors can be switched into the circuit to set different transduction gain.

Capacitors in the USI block can be switched into the charge amplifier topology to replace the microphone sensor as the input capacitance forming a low-power low-noise voltage amplifier [6]. In the voltage sensing experiment, the minimum capacitor available in a USI, which is 40 fF, is used as the feedback capacitor. The rest of the capacitors in the capacitor bank are progressively switched into the circuit to form an input capacitance ranging from 80 fF to 1.5 pF. The output

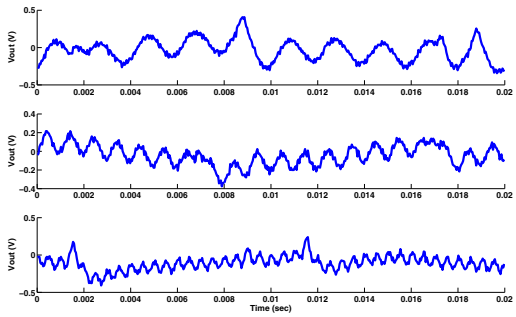

Fig. 8. The recorded transient waveforms from the RSSC when it is interfaced with a commercial microphone sensor for the input frequencies of 500 Hz, 1 KHz, and 2 KHz, respectively.

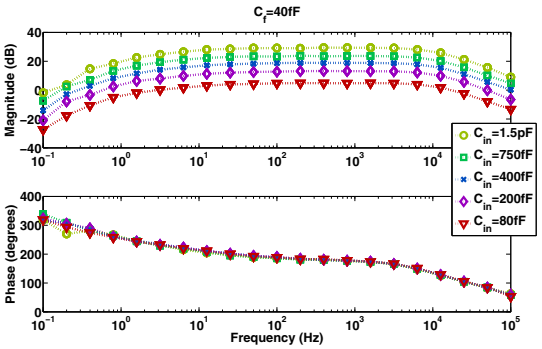

Fig. 9. The frequency response measured from a voltage sensing charge amplifier synthesized in the RSSC.

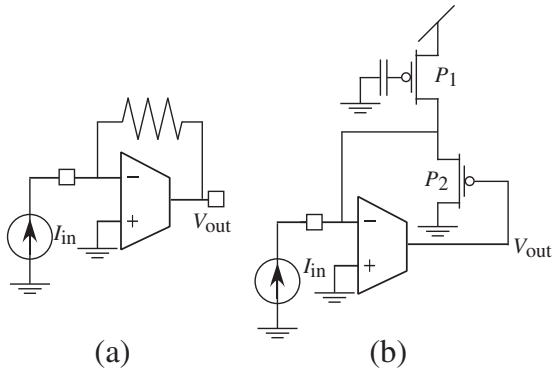

Fig. 10. The schematics of a transimpedance amplifier and a logarithmic amplifier that can be synthesized in a USI block for current sensing.

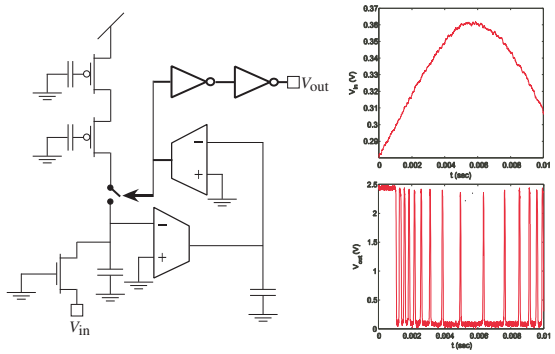

Fig. 11. The schematic and measurement results of a current mode second-order delta-sigma converter that has been synthesized using components in the switch matrices and in the CABs.

frequency responses for the different input capacitances are shown in Fig. 9. The low-frequency corner is lower than 10 Hz and is set by the leakage current at the high impedance node. The high frequency corner is set by the output buffer and can to be increased if a larger biasing current is provided.

Two types of current sensing interface circuits can be synthesized in a USI block, a transimpedance amplifier or a logarithmic amplifier as shown in Fig. 10. The floating-gate source follower in the USI is used to implement the logarithmic amplifier. The floating-gate transistor P_1 is programmed to be off and the I-V characteristics of P_2 are used to provide the logarithmic relationship. To demonstrate the analog processing capabilities of the chip, additional CABs are configured into a current mode second-order sigma-delta converter, which converts the received sensory current signal to digital. The schematic of the converter and the measured results from components in the CABs are shown in Fig. 11.

IV. Conclusion

A large-scale reconfigurable smart sensory chip is demonstrated in this paper. This chip contains 8 universal sensor interface blocks, 28 configurable analog blocks, more than 50,000 programmable elements, and on-chip programming circuitry. Each universal sensor interface block can be configured for capacitive sensing, voltage sensing, or current sensing. The outputs of the interface circuits can be multiplexed out of the chip or can be routed to other CABs for further analog signal processing or for sigma-delta conversion. This reconfigurable smart sensory chip has been demonstrated to be a useful tool for the fast prototyping of sensory microsystems for various kinds of power efficient sensing and processing applications.

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