A Mixed-Mode FPAA SoC for Analog-Enhanced Signal Processing

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***Abstract*—We present the RASP 2.9v, an FPAA for mixed-signal computation with an emphasis on enhanced digital support. This 25mm^2, 350nm CMOS chip includes on-chip compilable DACs, dynamic reconfigurability and digital storage, and 76,000 programmable elements. We demonstrate an analog image-transform processor, an arbitrary waveform generator, and a mixed-mode FIR filter.**

I. Reconfigurable Analog Systems

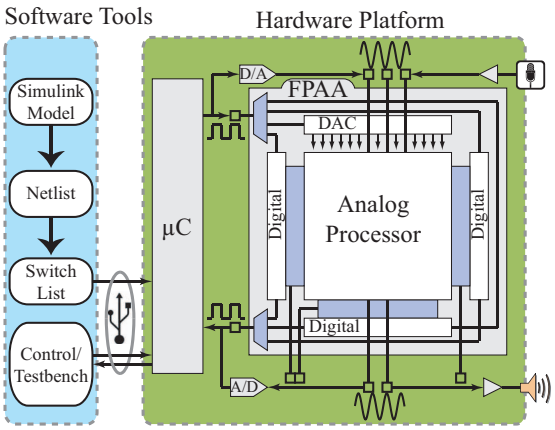
Field-programmable analog arrays (FPAA) are providing a low-power, low-cost, reconfigurable, and reusable hardware technology. We present the Reconfigurable Analog Signal Processor (RASP) 2.9v FPAA (Fig. 1), the first chip to combine large analog parameter density and digital dataflow handling. This generation of FPAA is more computationally dense than the previous largest FPAA design [1], which was itself higher density than any previous FPAA designs [2], [3]. The novel digital enhancements enable higher chip utilization and facilitate the chip's use as an embedded mixed-signal processor.

To illustrate this IC's potential to provide analog support to signal-processing systems, we focus the examples on mixed-mode processing systems. We demonstrate compilable DACs, an arbitrary waveform generator (AWG), a mixed-mode FIR filter, and an analog image-transform processor.

II. FPAA Architecture

The architecture of the RASP 2.9v FPAA is detailed in Fig. 2. The two main elements of traditional FPAAs are computational analog blocks (CABs) and the switch matrix (SM). CABs contain analog subcircuits, which can be arbitrarily connected using switches from the SM. The SM is not just overhead—it is composed of over 76,000 floating-fate (FG) MOS transistors, compact analog computational elements that require no external memory. These "interconnects" can be used as current sources, programmable resistances, or precision-tuning elements. This use of FG switches has proven to be stable and mature, relying on well-established programming methods [4]. Further, FG approaches have been widely used for parameter programming, tuning, and mismatch elimination [5].

The RASP 2.9v contains 78 CABs: 18 designed for compiling current-mode DACs, 24 optimized for vector-matrix multiplication (VMM), and 36 for general purpose computation. The embedded digital registers are detailed in Fig. 2(f). Signals are applied to and read from the chip using 79 analog I/Os, 18



(a)

Process	350nm CMOS
Voltage	Analog 2.4V, Digital 3.3V
Die Size	5mm × 5mm
Number of CABs	78 Total: 18 DAC, 36 Regular, 24 VMM (x4 input structures)
Programmable parameters	> 76,000
Number of Volatile Switches	4728: 6 × 400-bit (vertical), 14 × 156-bit (horizontal), 6 × 24-bit (DAC)
Chip I/O	79 Analog, 20 Dynamic output lines, 18 compilable DAC
Regular CAB Elements	132 OTA, 168 FgOTA, 36 T-gate, 72 nFET, 72 pFET, 36 OTA buffer, 144 500fF Cap
Mean Programming Speed	Volatile Switch: 719ns FG Switch: 31 Analog Indirect FG: 38 Analog Direct FG: 36

(b)

Fig. 1: The RASP 2.9v. (a) (a) The system-level diagram shows the analog core and surrounding digital control and interfacing. (b) Summary of the IC's parameters.

on-chip configurable DACs, and 20 digital register controlled I/Os that can configure analog I/O or store digital values.

A major innovation of the RASP 2.9v is the volatile switch registers, which connect every internal circuit node to one of 20 I/O lines and can be dynamically reconfigured while the chip is in run mode. This chip is the first to offer such dynamic reconfigurability in an FPAA. Buffered shift registers set each volatile switch open or closed. The shift registers are controlled by SPI protocol. To increase routing efficiency for biases, this chip introduces a V_{Ref} line that is routed throughout the SM, in addition to V_{DD} and GND lines.

Each DAC CAB contains an 8-bit shift register for con-

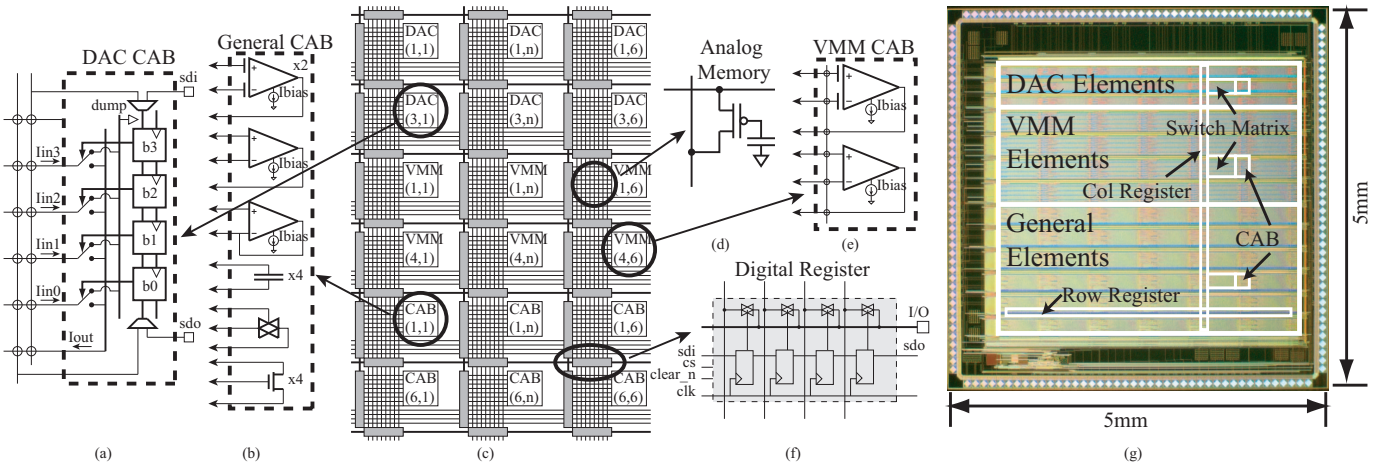


Fig. 2: Structure of the FPAA. (a) The DAC CAB contains an 8-bit register, allowing for multiple DAC topologies to be compiled. (b) The "General" CAB consists of common analog elements: amplifiers, transistors, capacitors, and transmission-gate switches. (c) The CABs are arranged in 6 columns with 13 rows. (d) The routing is a full cross-bar switch matrix with floating-gate switches intersecting each row and column. (e) The VMM CAB contains both regular and FG-input OTAs, which are commonly used as the front end to the VMM. (f) The volatile switch is controlled by a digital shift register that spans all of the columns (156-bit) and rows (400-bit). (g) Micrograph of the fabricated IC.

trolling current sources, allowing implementation of an 8-bit current DAC. The DAC CABs are grouped in threes, allowing easy creation of DACs up to 24 bits. Each DAC register can also be configured to take input data from an on-chip source, providing digital memory storage or scanning the DAC inputs serially. The CAB's reconfigurable nature allows the user to alter the least significant bit (LSB), change the number of bits, or try multiple topologies. Fig. 3 illustrates an 8-bit current DAC compiled with a single FG-current source for each bit.

The other two CAB types, VMM and General, contain common analog components which allow the synthesis of almost any large-scale system. The VMM CABs contain paired OTAs connected by local wiring. One of the OTAs is part of the current-scaling active current mirror; the other is a wide-range OTA for V/I or I/V conversion. All OTAs have bias currents set by programmable FGs. The wide-range OTAs also have programmable input offsets.

To combat the transistor mismatch which plagues indirectly-programmed FG switches, our SM contains a number of directly-programmed switches, shown in Fig. 4. This eliminates the need to characterize the mismatch before using the switches as precise current sources. However, the trade-off is the introduction of a selection pFET to the signal path, reducing the conductance at low voltages. Therefore, the SM provides both types of switch to fit the needs of the application.

III. Mixed-mode System Examples

We show here results of multiple systems that illustrate the key advances of the RASP 2.9v. Each of these example systems would have been difficult or impossible to compile on previous FPAA platforms. We validate the chip by demonstrating the versatility of systems that can be compiled, whereas we achieve comparable performance to systems that were fabricated in custom silicon.

The FPAA design and test flow involves using our synthesis and programming tools in the MATLAB environment. The resulting object code is then programmed onto the FPAA, which is embedded on our Program & Evaluation (PE) board [6]. This PE board is powered by and communicates with the PC via a USB connection. It also includes a digital microcontroller and data converters for testing embedded systems.

The banks of shift registers make the RASP 2.9v well suited for an analog AWG [7], as shown in Fig. 5. The AWG architecture makes full use of the SM; every transistor acts as a memory element, holding the value of the current it will pass to the channel. A single ON bit repeatedly passes down the shift register and activates one current source at a time per output channel. Each row of switch elements can hold a different waveform, which can be selected by a second select register, orthogonal to the scan register. The waveform is current-mode, so any configuration of output lines can be selected at the same time, and the output will be the sum of the individual waves. The example shows a sine wave generated at multiple frequencies, with THD of -24.6dB.

Fig. 6 illustrates a novel architecture for a mixed-signal FIR filter system. The front-end analog integrate-and-fire system acts as an asynchronous sigma-delta ADC [8]. This converts the signal into a digital spike train that is scanned in by the register. Each element in the register operates a current source that is programmed to an FIR coefficient. The overall system performs a signal convolution a against the mixed-signal FIR filter. The example data shows a sinusoid processed by the sigma delta, and the resultant bit stream after passing through a low pass filter.

Fig. 7 shows an image transform system based on computing a separable convolution on the RASP 29v. A separable transform requires the vector-vector product of two vectors over the image. The processor block is a compiled VMM [9], and the input pixels are scanned in with the on-chip current DACs. On the RASP 2.9v, the VMM gain error is 6 bits accurate (7-bit programmed) by using the direct switches. The

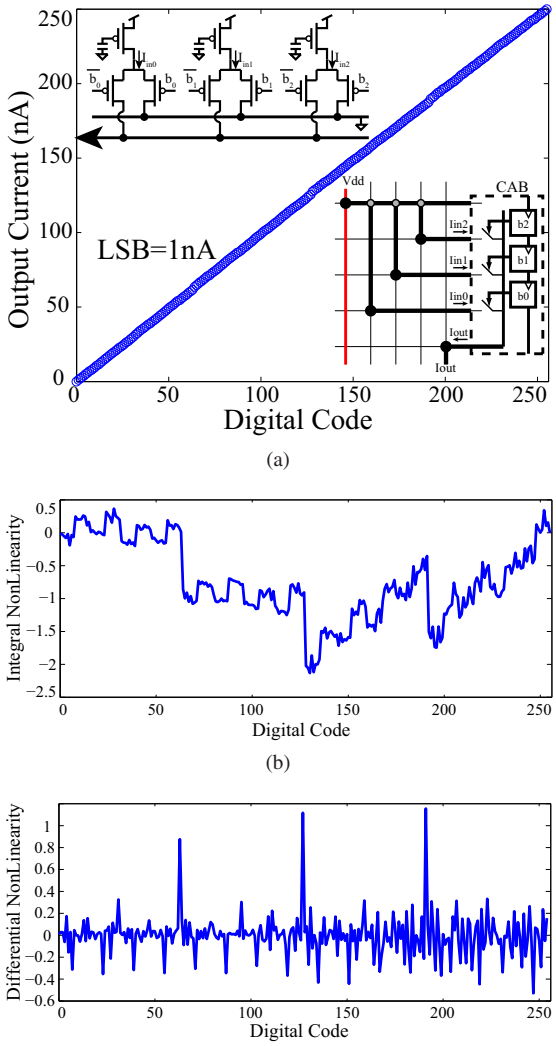


Fig. 3: The on-chip reconfigurable DAC. (a) The schematic and FPAA implementation of the floating-gate current-source DAC. The measured results are from a compiled 8-bit current DAC with an LSB of 1nA. (b) The INL and (c) DNL plots from the 8-bit current DAC.

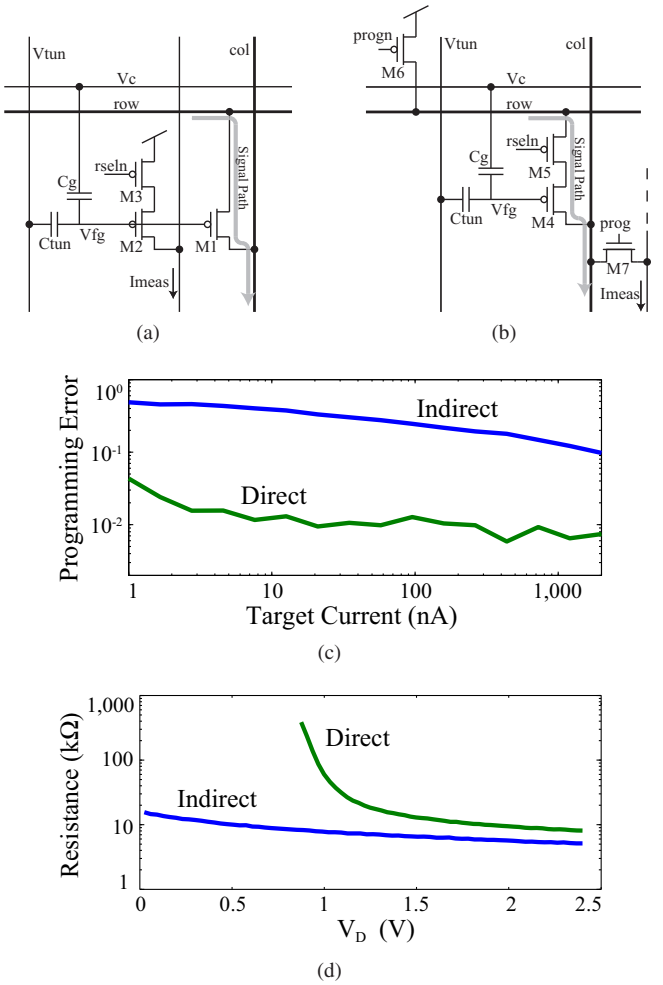


Fig. 4: The routing structure contains two FG switch variations. (a) The indirect-programmed FG switch (M1) provides a very good pass element, since there is no selection circuitry in the signal path. (b) The direct-programmed FG switch (M4) has improved matching, but is a poor all-purpose switch. (c) The direct switch shows a much lower first-pass programming error between targeted current and measured output current. (d) Each switch shows an ON resistance of about 10kΩ; the direct switch's resistance, however, rises sharply at low voltages because of the pFET in the signal path.

input pixels are scanned into the on-chip current DACs and fed into the VMM block. The transform kernel is separated into two vectors (S1 and S2) and programmed into different rows of the VMM. To complete the transform two passes must be made, once against each vector, where the appropriate output is selected by the registers. The example shows a 3×3 Sobel edge detect transform and a 9×9 smoothing filter.

IV. Conclusion

The RASP 2.9v is designed for mixed-signal computation, with configurable DACs, VMMs for efficient linear operations, generic CABs for many nonlinear operations, and digital switch registers for dynamic reconfigurability and digital storage. This novel SoC is a deliberate push into the space of digitally-controlled analog systems. We see the future of reconfigurable analog systems as not just stand-alone analog chips, but embedded alongside digital hardware in large-scale low-power mixed-mode systems. We have demonstrated an 8-bit compilable DAC, an arbitrary waveform generator (AWG), a mixed-mode FIR filter, and an analog image processor.

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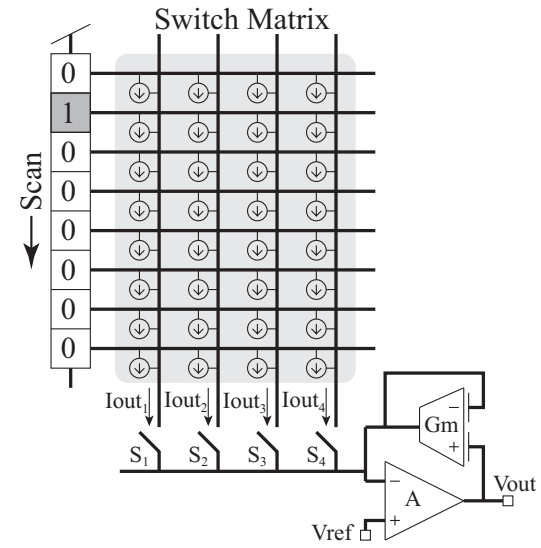

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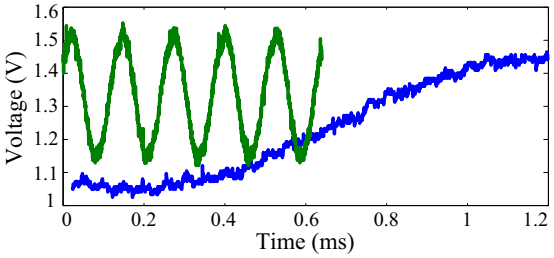

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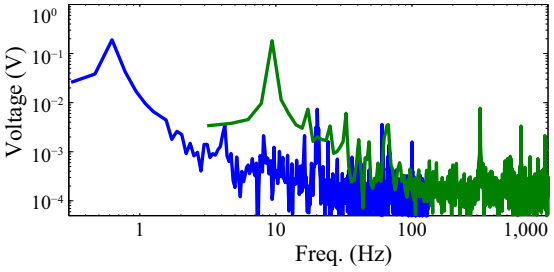
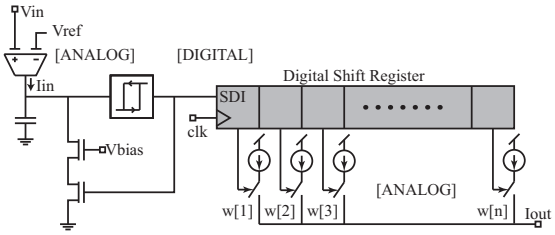


(c)

Fig. 5: Application of the RASP 2.9v as an Arbitrary Waveform Generator. (a) Architecture for a 4-Channel AWG. The volatile switches serially connect each row to V_{DD}, so that each column passes the current supplied by the scanned floating gate elements. The volatile switch lines can be used to choose one channel—or combine multiple channels—to be converted to an output voltage. The I-to-V is an OTA with a FGOTA in feedback to provide a tunable transimpedance. (b) Two sine waves generated by the AWG, using 40 devices scanned at 17.5 kHz and 310 kHz. Note that the FGOTA has been programmed to allow different gain and offsets. (c) FFT of the two sine waves. Total harmonic distortion is -29.5dB and -25.5dB respectively.



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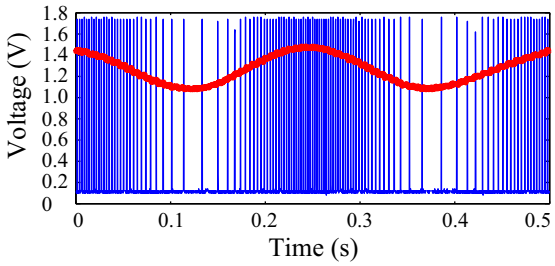

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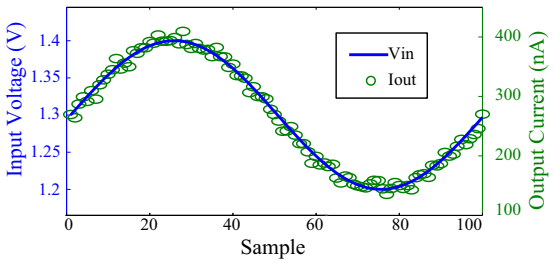

(c)

Fig. 6: (a) Architecture of the mixed-signal FIR filter. (b) The integrate-and-fire spike generator produces digital pulses with a frequency based of the input current. (d) The output of the mixed-signal system. The initial results show the output current correctly reconstructing a slow-moving input analog signal.

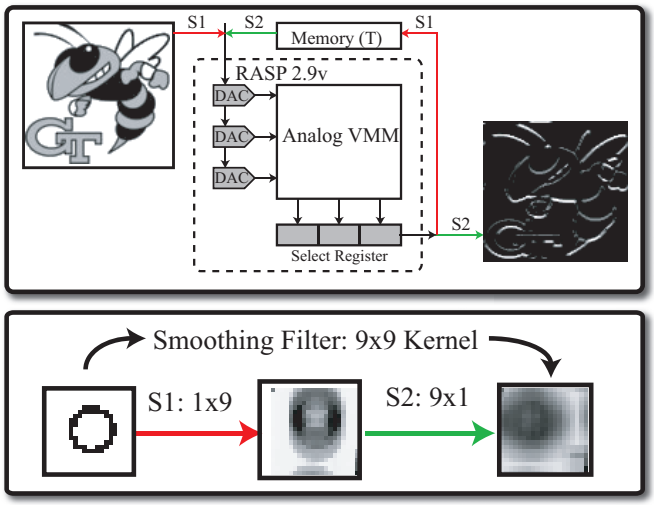

Fig. 7: Application of the VMM in an image processing system. The image processor performs separable transforms scanning in the image and convolving by S1 and S2 in two passes. The kernels chosen for this test are a 3×3 Sobel edge detector and a 9×9 smoothing filter. The system schematic of the image processor front end shows the on-chip DAC components providing the signals to the VMM.

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