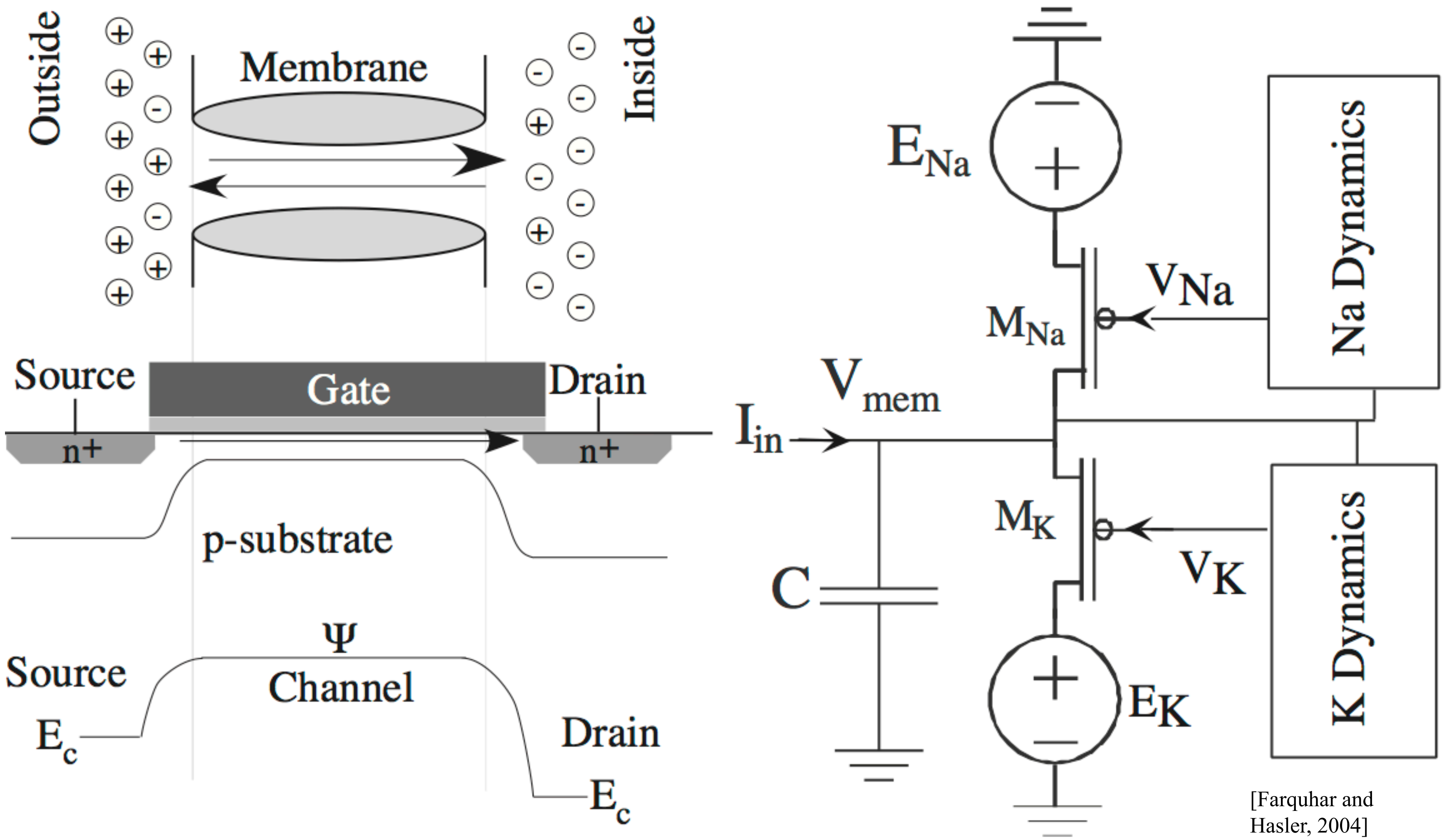
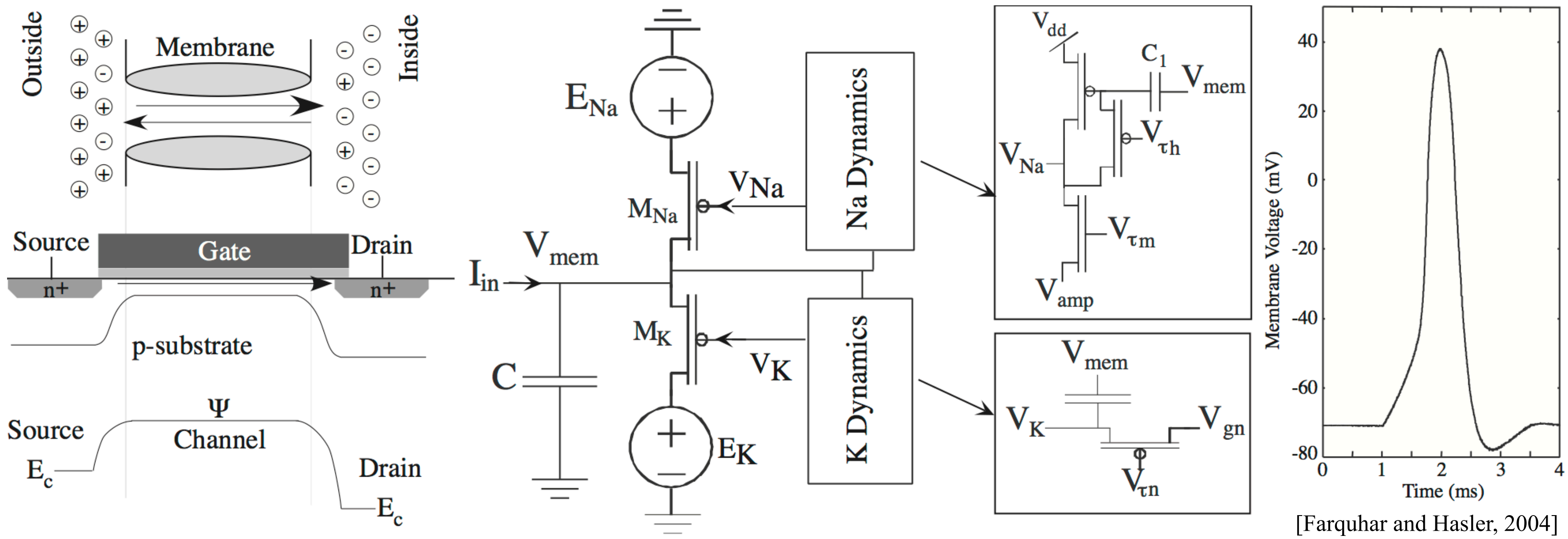
Transistor Channel Model



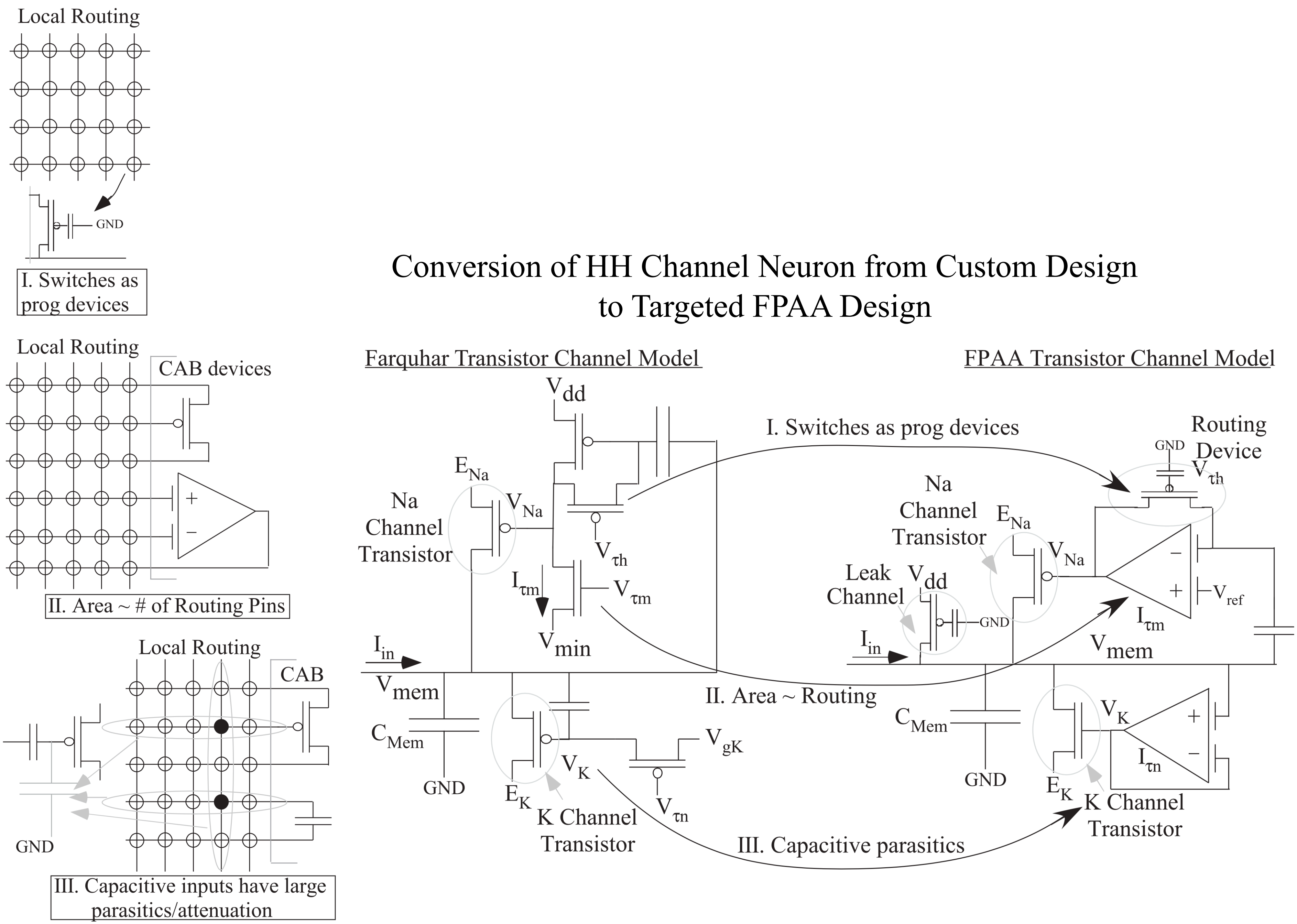
[Farquhar and Hasler, 2004]

Transistor HH Channel Model



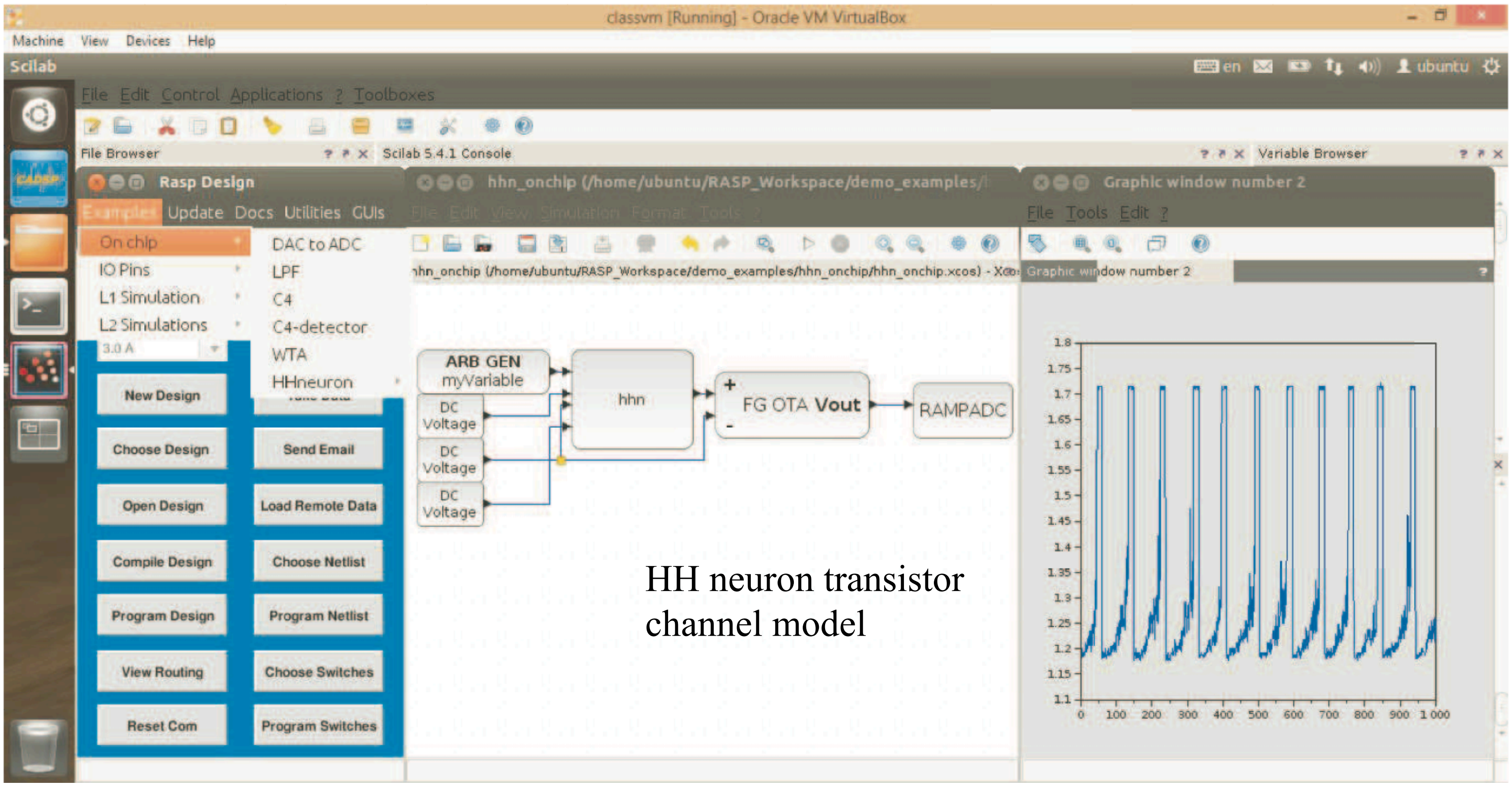
[Farquhar and Hasler, 2004]

Utilizing the physics of physical medium (Si) to efficiently implement computation



Conversion of HH Channel Neuron from Custom Design to Targeted FPAA Design
Local Routing
GND
I. Switches as prog devices
Local Routing
CAB devices
+
−
II. Area ~ # of Routing Pins
Local Routing
CAB
GND
III. Capacitive inputs have large parasitics/attenuation
Farquhar Transistor Channel Model
V_{dd}
E_{Na}
V_{Na}
Na Channel Transistor
$V_{\tau h}$
$I_{\tau m}$
$V_{\tau m}$
V_{min}
I_{in}
V_{mem}
C_{Mem}
GND
E_K
V_K
K Channel Transistor
V_{gK}
$V_{\tau n}$
I. Switches as prog devices
II. Area ~ Routing
III. Capacitive parasitics
FPAA Transistor Channel Model
Routing Device
GND
$V_{\tau h}$
Na Channel Transistor
E_{Na}
V_{Na}
Leak Channel
V_{dd}
GND
I_{in}
−
+
V_{ref}
$I_{\tau m}$
V_{mem}
C_{Mem}
GND
V_K
+
−
$I_{\tau n}$
E_K
K Channel Transistor

FPAA HH Neuron Example Block and Measurement



HH neuron transistor channel model

Experiment Session

Compile an HH Neuron Block.
See the neuron spikes.
(No indirect programming mismatch compensation)

You can modify the input signal with a higher input current, and re-run the computation.