A Senior-Level Analog IC Design Course Built on Open-Source Technologies

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ABSTRACT

We present a project-based alternative to a classical senior-level first Analog IC design course. This hands-on approach is enabled through a systematic approach to on-line lectures and course material, as well as open-source IC design process (Skywater 130nm CMOS) and tools (magic, Xschem) that are capable of fabricating working ICs. This realistic student design experience builds student confidence in designing 10-100 transistor circuits that could be fabricated on this IC process.

CCS CONCEPTS

• **Hardware → Integrated circuits**.

KEYWORDS

analog design, IC design, educational techniques

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This discussion presents our hands-on project based learning for a senior-level analog IC design course (Fig. 1) currently enabled through open-source IC design files (Skywater 130nm CMOS). This senior-level undergraduate semester course on analog IC design is a class where one might typically use Grey and Meyer's classic textbook [1] where students would work out a number of typical homework problems. The students taking this class would have a semester course in linear circuits, device physics, and basic transistor circuits. These courses are taught at a large US engineering program that can sustain multiple analog design courses.

This open-source analog IC design centric course development (Fig. 1) focused on two goals. First, as ECE students have more and more interest at higher system levels (e.g. signal processing), this course needed to move towards system design, abstracting device

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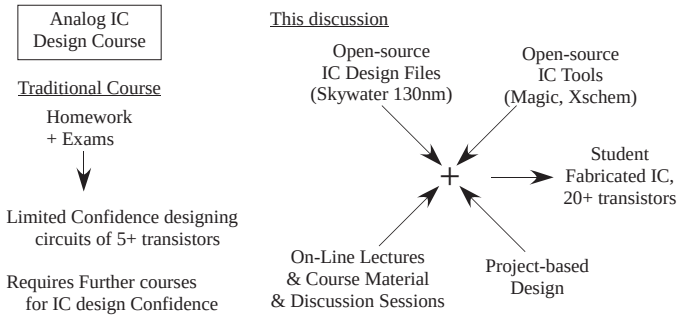

Figure 1: Although a traditional first analog IC design is primarily focused on homework and exams, we discuss our experience and data on a project-based first analog IC design course. Students work directly with a realistic IC design experience due to the recent availability of open-source 130nm CMOS design files (e.g. Skywater 130nm CMOS), and students directly have their own setup as the process is enabled through open-source (magic, Xschem) tools. The use of on-line lectures and course material enables sufficient student interaction to develop sufficient student expertise to build 10-100 transistor designs, typically considered impossible in a first analog IC design course, including some designs ready for 130nm IC fabrication.

and circuit information in a careful and yet understandable framework. Second, as hands-on learning and interaction is strongly encouraged by industry recruiters, a project-based curriculum empowers a hands-on approach. The following sections discuss analog IC design course overview (Sec. 1), use of hybrid format to increase student conversations (Sec. 2), and course structure (Sec. 3), the analog IC design course impact and assessment (Sec. 4), as well as discussion and summary (Sec. 5).

1 ANALOG IC COURSE OVERVIEW

This effort developed a fully open-source course [2], that includes lecture nuggets, course and project resources, and project requirements. The recent 130nm CMOS open-source Skywater opportunity with no-cost fabrication to the community completed the structure of a completely open-source analog IC design course. This course does not cover IC measurements and does not require hardware measurements. Hardware could be made available in future versions of this course through a remote test system (e.g. [3]).

This Georgia Tech (GT) course, ECE 4430 had two possible student backgrounds. GT undergraduate students typically have taken a class in linear circuits (ECE 2040), a device physics course (ECE 3040), and a first full course in transistor level circuits (ECE3400). Although ECE3400 can be taught with a system level focus (e.g. [4]), most faculty teach this course in a traditional manner working through discrete audio amplifiers with different transistors [5]. GT graduate students typically have a traditional ECE degree with a wide variation in their circuit background and knowledge. A couple of graduate students received their undergraduate

ECE degree from GT in both courses. This course development builds upon previous undergraduate (e.g. [4]) and graduate (e.g. [6]) course development efforts, efforts that, in turn, come through a Caltech tradition of hands-on and project-cenric teaching around analog and digital circuit design (e.g. CNS 181, 182, 184).

The course deployment and development occurred over multiple course offerings of ECE 4430 (Fig. 2). The first semester (Semester 1, Fall 2017) was an early deployment for a project based first analog IC design course utilizing Cadence design tools that would also be used for digital VLSI design courses. Semester 1 used a generic 130nm design process that would not exactly relate to fabrication that could be used through the Cadence tools.

The second semester (Semester 2, Fall 2021) was the first fully developed course curriculum using open-source design tools and technology items due to the availability of the 130nm open-source Skywater IC fabrication. Semester 2 occurred during the COVID-19 pandemic with the multiple associated issues for students and faculty (Fig. 2). The availability of Skywater's open-source 130nm CMOS process [7], where the design files were sufficient for fabricatable IC design avoided students signing NDA agreements, and the required information was available for the students. Because the 130nm IC process is valid for fabrication, the students learned using a real IC technology that enables having cells developed in the class projects to be included on upcoming Skywater 130nm CMOS run. We are incorporating Semester 2 designs into an IC to be submitted on an upcoming 130nm CMOS run.

The open-source 130nm tool set (Semester 2) was encapsulated into a single, openly available Ubuntu 20.04 VM [8]. The toolset includes magic, Xschem, ngspice, and resulting technology files for the Skywater 130nm CMOS process. A single framework enables straight-forward instruction for students using these tools, including either loading VirtualBox to operate the VM on any machine, as well as having instructions for student to build their own setup if they prefer. Encapsulating open-source tools in one VM reduces the stress of utilizing open-source tools.

From our perspective, the student effort for using the open-source tools is significantly less than using the Cadence tools, and lets students operate everything on their own machines, unless they had used the tools in a previous digital VLSI course. Most students quickly were able to utilize magic's toolflow, and even those students with previous Cadence experience preferred magic layout by the middle of the semester. Class sessions naturally integrated layout into discussions. On the otherhand, given the student culture of learning Cadence tools at our institution (students are expected to just learn it on their own), student questions and interactions about the open-source tools was higher. Students tended to have a deeper knowledge of layout and resulting circuit design by having the open-source tools available.

2 HYBRID FORMAT TO ENABLE GREATER STUDENT CONVERSATIONS

The course structure utilized an inverted classroom approach to increase student interactions and conversations. The motivation for this approach comes from the positive impact of faculty-led recitations (e.g. MIT) on student learning. We aim for meaningful in-person interaction by optimizing the classroom experience

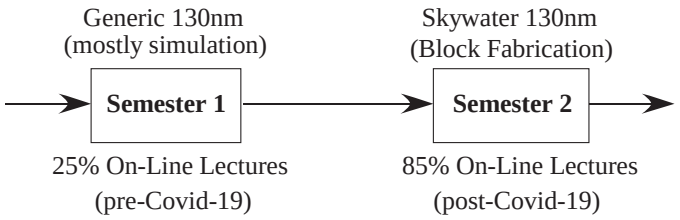

Figure 2: Comparison of the two semester implementations for this course at Georgia Tech(GT), illustrating the different factors in each step of the development, as well as factors for comparison between the courses (ECE 4430). Semester 1 was offered Fall 2017, and semester 2 was offered Fall 2021. The author taught both this class both semesters (single section).

through small on-line lectures (Lecture Nuggets) and flexible discussion & problem-solving sessions during normal classroom time. Course materials were all on-line [9], and possible textbooks were considered reference material.

Lecture Nuggets: The traditional straight-forward hour long lecture often compresses to two to four 5-10 minute lecture nuggets (Fig. 3), a concept related to short lectures advocated elsewhere (Small lectures [10]). The length was chosen as the average length of a Youtube video where someone is speaking is 8 minutes, so the videos attempt to match an average attention span. Lecture nuggets are roughly the content of a single dense slide, although some videos use different styles, including animation. A short lecture often uses a pointer to highlight important points on a single one slide. All lecture nuggets are openly available on Youtube [9], being consistent with the open-source course development. Open-source lectures builds an ecosystem that not only enable students at the local university, but rather has a global reach, typical of the MIT opencourseware project. These lecture nuggets are interchangeable between multiple classes. Students that are missing a particular prerequisite concept or wish to catch up on background material can watch a lecture nugget from an earlier class. A lecture nugget on MOSFET transistor physics could be used in a device class, a first transistor circuits course, as well as this analog IC design course. Several lecture nuggets, some not used for this ECE 4430 course, were directly used for other teaching directions, including the virtual 2021 version of the Telluride Neuromorphic Workshop, and we expect they will be useful for the hybrid 2022 Workshop. Roughly 25% of the lecture nuggets were available for Semester 1, and nearly a full set ($\approx$ 85%) of lecture nuggets were used for Semester 2; every semester generates additional resources.

Interactive Class Sessions: The lecture nuggets, viewed by the start of class, enables interactive faculty–class sessions instead of faculty covering general topics that rarely have any class interaction. These class sessions were all in-person, faculty-led interactive class sessions. Some nuggets were developed as the starting class conversation topics, and recorded after the discussions to be available for those who could not make the session while still being useful for future courses. Having started these approaches before the Covid-19 pandemic, these techniques proved invaluable during the pandemic, enabling hybrid approaches that facilitated meaningful in-person interaction craved by students. During the semester, more than half of the students were routinely participating in the conversations. By using these techniques for classes (including this one) during the Covid-19 pandemic, students consistently showed up for the sessions, even as students generally were

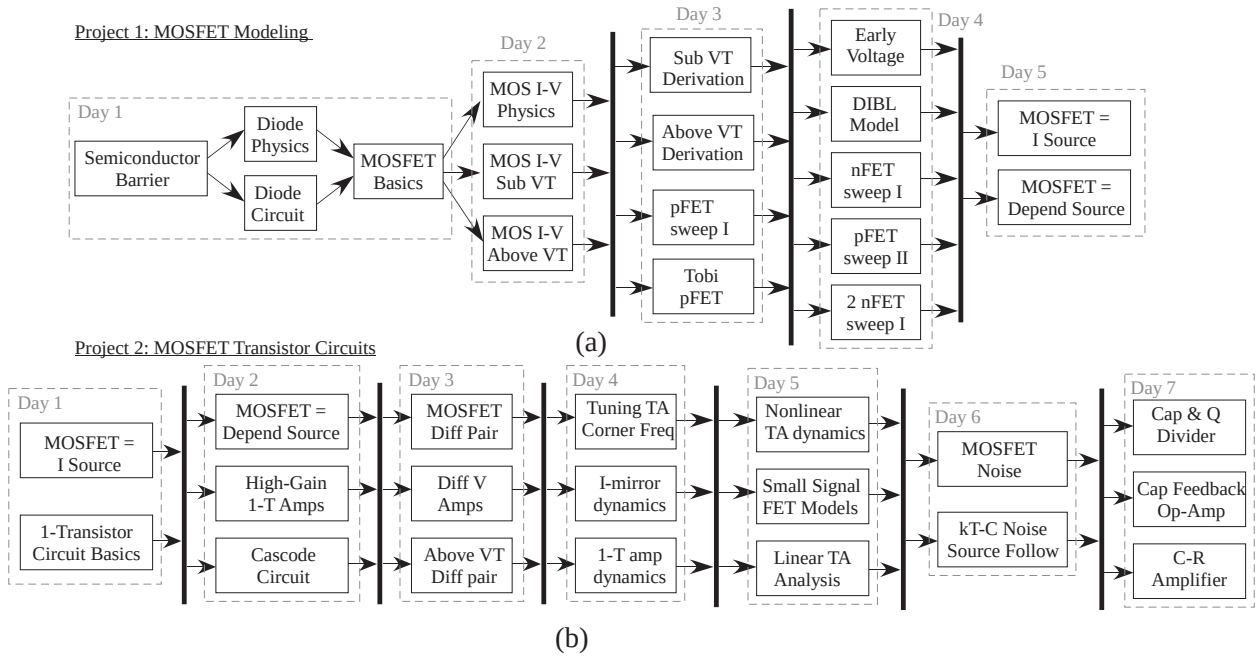

Figure 3: Video lecture nugget watching schedule for the first two projects (Semester 2, Fall 2021). (a) Project 1: Lecture watching for the first five lecture days. The last day is a review session. (b) Project 2: Lecture watching for the first seven lecture days. The last day is a review session.

weakly attending other in-person learning opportunities throughout the semester. Most students had watched the prescribed videos before the class discussion session, as qualitatively seen by the high amount of student discussions during the class sessions; there was no need for in-class quizes to motivate the students to watch the videos. The class did not use any incentives for watching these videos (e.g. daily quizes), as students realized not preparing for one class often put them significantly behind others in the class after just one lecture. The conversations built a strong community between all of the students in the class, far beyond a typical class at this institution. Developing on-line resources can be utilized in many future semesters in multiple courses to provide additional time for discussions, reviews, and synthesis with students.

Use of a few Virtual Sessions: A few sessions (five, semester 2) were chosen intentionally as virtual sessions primarily as spaces to discuss design tools. In these cases, the professor can demonstrate particular features of design tools, as well as have other students show their screen when they attempt to use the design tools during the discussion. One must be careful to carefully plan out the interactive dynamics for a virtual session to get all students to participate, as our experience shows that students can be more passive in these sessions.

3 ANALOG IC COURSE STRUCTURE

This Analog IC Course was structured around four core projects (Similar topics for Semester 1 and Semester 2):

Project 1: MOSFET device modeling & SPICE & layout
Project 2: MOSFET Transistor Circuits
Project 3: Dynamics, Stability, references
Project 4: Analog System Design

The course had no final exam, and finished during the last week of normal classes, two weeks before the official end of the semester. The projects were accomplished primarily in teams of two students. The graphical map of the lecture nuggets shows the flow of the topics taught in a particular project (Fig. 3).

The first project focuses on MOSFET device modeling as that provides the basis for all projects. This project involves using measured data from the 130nm IC process, regressing the data, and making their own spice model from the data. For Semester 1, we used a set of 130nm CMOS transistor data that we measured, while not correlating the IC process. For Semester 2, we used a set of openly available, on-line provided transistor measurements for the Skywater 130nm process; in future semesters, we will make available and use our own IC measurements from Skywater 130nm devices. The student developed spice model is used throughout the semester with some later additions (capacitance models). This project involves layout and schematic of a couple of nFET and pFET transistors, extraction, LVS (Layout vs. Schematic), and simulation of these transistors. The students start the remaining projects with knowledge of the IC design tools. This course focuses on only MOSFET devices to enable some system design at the end of the semester, and these are the devices easily available in the 130nm CMOS process.

The second project focuses on basic MOSFET transistor circuits. This project includes single-transistor amplifiers using ideal and transistor current sources (Common-Source, Common-Drain, and two Common-Gate configurations), differential transistor pairs, and Transconductance Amplifiers (TA). The students perform layout and post-layout simulation. For Semester 2, the vertical pitch of these cells and other core cells built in the projects was fixed to 6.5μm, with fixed power-supply (0V and 1.8V) supply lines in fixed

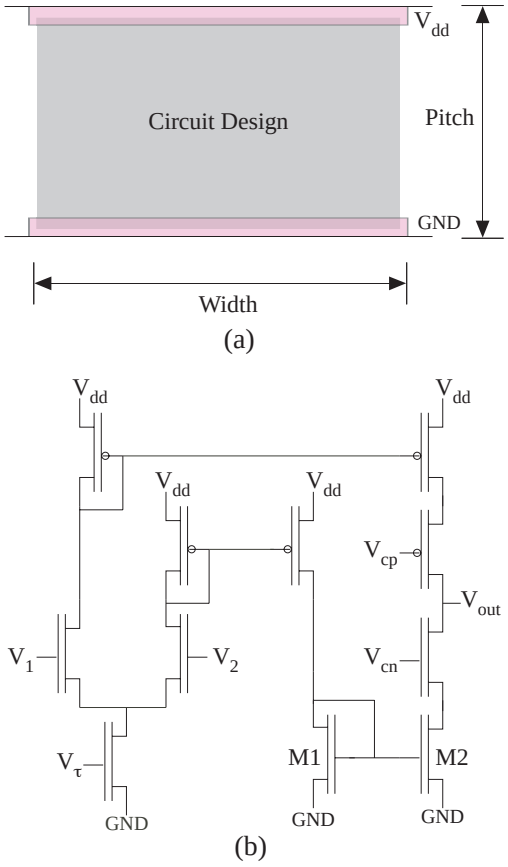

Figure 4: **Analog IC cell design framework. (a) All cell layout for the course were to correspond to a single pitch (6.5μm) with a particular cell design, and the students are required to minimize the cell width. A number of cells for the class (e.g. a bootstrap current source) were available and expected to be used by the class. (b) An example circuit used for the second project that would be designed in this standard framework. All parameters are optimized given this constraint. The bias current voltage (V_τ) and nFET and pFET cascode voltages (V_{cn} and V_{cp}, respectively) are generated from the bootstrap current source.**

positions at the boundary of the cell (Fig. 4). These circuit modules, effectively analog standard cell blocks, are potentially shared blocks for the class; with the development of analog standard cell libraries [11] and open-source 130nm libraries [12], the students can utilize some of these blocks in future projects. This course would not be the first time the students would have seen transistor-based circuits (ECE 3400), although it would be the first time students consider the analog aspects of IC design. This project begins the discussion about noise (e.g. [13]), and it is used in simulation and design. The second project includes the first design project of a single output pole (output capacitor) TA (similar approach as in [14]) for a given set of specifications that are assigned specifically to each group (Fig. 4). A complete design are the first cells that could be submitted for fabrication as part of a test chip.

The third project focuses on the linear dynamics, particularly stability, for analog IC circuit designs. One project requirement focuses on designing a 4-5 transistor, two-pole transimpedance amplfier topology (from [15]). Another project requirement would include designing another high-gain amplifier (folded-cascode topology), or designing a comparator. The specifications varied for each

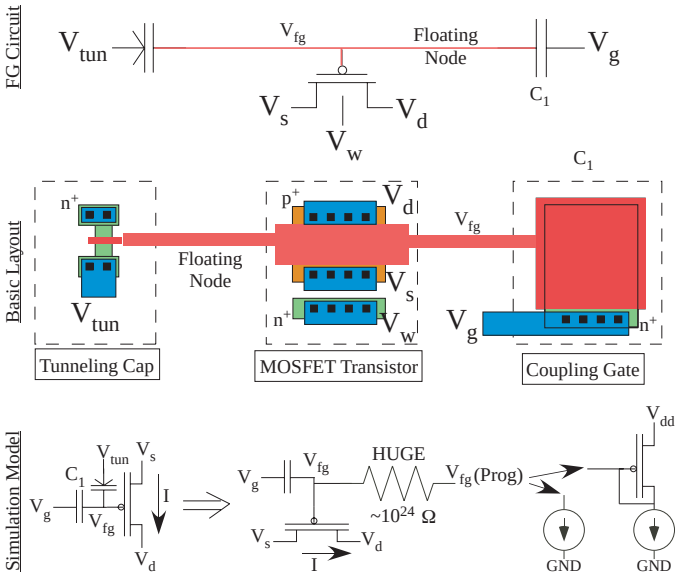

Figure 5: **Floating-Gate (FG) enable programmability for, and modularity in, analog circuit and system design. A FG Circuit is primarily a pFET transistor with multiple capacitors to the floating node, where the Basic Layout shows a pFET transistor, The FG transistor Simulation Model uses a HUGE resistor to set the programmed FG voltage through SPICE DC analysis, enabling correct measurements for other simulation modes (e.g. transient, sinusoidal). For 1pF capacitor, a large resistor of 10^24 Ohms results in $\approx 300\mu$V drop over 10 years for a 1V programmed voltage range.**

of the project teams. A two-stage op-amp is shown as one example of an analog design with significant design requirements for stability; no specific project question focuses on a two-stage op-amp design as it is not the ideal choice for typical IC design.

Continuing on the analog standard-cell theme, this unit introduced analog programmability using Floating-Gate (FG) circuits that can be built in the 130nm CMOS process (Fig. 5). FG simulation and basic layout techniques enable using programmability to directly address parameter variation in analog circuits and how to minimize the resulting temperature variation, particularly as threshold voltage mismatch is the biggest constraint in analog design. FG design becomes one motivation for discussing capacitors in a planar (e.g. 130nm Skywater) CMOS process, as well as a motivation for discussing and addressing threshold voltage offsets. Future classes should benefit from experimentally measured 130nm FG standard cells (in pitch) that can be directly used in the student designs, as well as the wider infrastructure integrating these cells into their design.

The fourth project focuses on classical analog system design components [16]. Each team focuses on one significant component design (e.g. medium speed ADC, Voltage DAC) or a low-frequency front-end sensing system. Semester 1 had teams developing parts of low-frequency (kHz) sensor chains that would interface to other team's designs. Semester 2 had teams design pipelined algorithmic ADCs, voltage and current DACs, as well as a neural amplifier sensing chain including a ramp ADC. Roughly 70% of the groups completed their full design to the target specifications, and the other groups had a significant number ($\approx$ 70%) of the subsystems

Question	Semester 1	Semester 2
My MOSFET transistor knowledge significantly increased this semester	1.8	1.71
My fundamental transistor circuit knowledge significantly increased this semester	2.07	1.24
My system analog circuit knowledge significantly increased this semester	2	1.5
I am comfortable designing circuits with two (or 1-2 more) transistors	2.4	2.24
I am comfortable designing circuits with five (or 1-3 more) transistors	2	1.71
I am comfortable designing circuits with ten (or 1-5 more) transistors	1.8	1
I am comfortable designing circuits with twenty (or 1-10 more) transistors	1.4	0.4
I have increased my circuit design ability this semester	1.8	2
Experimental measurements are important for learning circuit design	2.2	2.35
My knowledge of circuit tools/ simulation has increased this semester	2.27	2.29
Simulation techniques are a helpful tool, but not sufficient for learning circuit design	0.2	1.35
Useful circuit abstraction is essential for building system circuits	1.67	1.82
How likely would you take another circuit course if you had the opportunity	2.13	1.71

Figure 6: Some of the student survey statements and the respective average agreement response value above the neutral (0) level. The survey used 7 point Likert scale (-3 to 3) to see agreement with the statement (strongly agree (3), agree (2), somewhat agree (1), neutral (0), somewhat disagree (-1), disagree (-2), strongly disagree (-3)). Semester 1 and 2 has responses from the entire class (16 and 17, respectively).

designed for target specifications. These projects change each semester teaching this course, effectively expanding the full analog std. cell library. Semester 2 formally defined and used standard cell concepts, as well as enabling reuse of cells between groups for this project. Future semesters will build on these opportunities.

4 ANALOG IC DESIGN COURSE IMPACT AND ASSESSMENT

Part of the implementation of this course attempts to measure how the goals of the class have been reached. The achievement of most groups in this class to successfully design a system-level analog block in their first analog IC course shows significant comfort designing circuits with many transistors. In reviewing (and in some cases improving) the analog IC designs for fabrication, more than half of the students have system designs that are 80-90% ready for IC fabrication and should be near expected IC parameters. Many students mentioned they were enthusiastic about this course as it is the one analog circuit course at this institution that teaches IC transistor design and layout, and they were enthusiastic to learn these skills. From multiple discussions, the students felt confident they learned these design skills in this course. Multiple students taking this design course followed on with another senior-level or graduate-level circuits course in the following semester.

A second measure is through student surveys (Fig. 6) given at the during the last week of class before the fourth projects were due. The surveys were given with the faculty member out of the room with a nearly full class, and there was no identifying information of any individual, including any handwritten comments typed up so no information could be identified to a particular student. Comparisons with classically taught sessions (e.g. Homework, 3 exams, and a final) require these surveys to be taken in a similar manner by other professors teaching this class or similar type classes, and as of this stage, this author has not had this opportunity.

The results from two classes showed the students gained confidence in their overall design with transistor circuits (Fig. 6), with some average confidence for 10-20 transistor circuits. The expectation (although not able to be measured) for classically taught sessions is expected to be at far lower confidence levels,. In previous semesters when this class was taught by this author following a traditional homework and periodic exams, most students struggled having confidence building circuits of 5 transistors or more, as compared to significant confidence in Semester 1 and Semester 2 in designing circuits of 10 transistors or more. Unfortunately, the survey questions were not given to these students, as their struggle inspired making these specific questions used for these courses.

The scores do show a general decrease between Semester 1 and Semester 2. Semester 2 occurred after the Covid-19 lockdowns with the associated student stresses. The use of on-line lectures for discussion sections after the lockdowns had a similar impact to the pre-covid course. The score difference was likely affected between using an established CAD tool flow (Semester 1) and the first time using an open-source tool flow (Semester 2). The Cadence tool set is established, sometimes used by students in previous courses, with a large number of on-line resources. Further, the student culture simply accepts they must learn these tools and they expect no faculty assistance with learning these tools, leading to an acceptance of whatever issues are their issues. Introducing a different tool, even an open-source and free tools (e.g. Magic), is expected to have some issues in the first introduction and puts more responsibility on the professor. The students in Semester 2 stated more often about wanting additional documentation for the tools. The students were given options for their simulation tools due to the issues in the on-line tools; in future semesters, a single option would seem to improve the student's perception. Even though Semester 2 had all of the tools encapsulated in a single Ubuntu 20.04 Virtual Machine (VM), there was a higher initial stress adapting to an easier tool flow. Now that the VM is established and openly available, others outside of GT are using the VM. The students did state later that they appreciated this virtual machine, as well as students who knew both Cadence and Magic stated after the end of the semester that they preferred Magic for layout. Generally, the IC designs

developed in Semester 2 were significantly better developed than Semester 1 by almost all groups, with the exception of two individuals in Semester 1 who had extensive previous Cadence experience, including previous work experience.

As an initial comparison, informal use of the same survey questions and discussions with students taking a graduate level course (ECE 6412, Spring 2022) that resembles an earlier exam and test version of ECE 4430 provides an initial contrast of these techniques. Students who took Fall 2021 ECE 4430 were not included in these responses as they stated they had a mastery of the topics covered in this graduate course at the start of the course. The range of understanding transistor circuit knowledge is within the range between the two semester scores (Fig. 6), where the scores are negative values for increasing MOSFET knowledge and system knowledge. The level of comfort for analyzing, as opposed to designing circuits, with two to 5 transistors is in a similar range to the ECE 4430 class, the rough measure drops well below 1 for 10 transistors (analysis only), and the measure becomes negative for 20 transistors or more. The students felt their circuit design ability increased over the semester (Fig. 6), although with no improvement at the device or system level, where aspects like simulation or abstraction were not even discussed during the class. Faculty collaboration could enable more beneficial formal future comparisons.

From the experience of Semester 1 and Semester 2 courses, as well as this author's experience, additional questions should be added to the survey in future semesters probing further around the in-class discussion and on-line lecture format, as well as questions baselining the general use of on-line techniques. From written comments and post-class in-person discussions, several students liked the on-line lecture format and the discussion format. The short nugget format was different from other on-line lectures, where that difference was positive and challenging for different students. A few students (Semester 2) wanted traditional lectures, partially because that is the primary culture at this institution, and partially because traditional lecture constrains the content required to be learned, and in turn reduces the effort expended on the course. Those who at least stayed up with lectures before class saw class as positive. Those who did not watch the lecture nuggets before class struggled with this format. Inverted classroom approaches consistently requires more time from students taking the course, while increasing student involvement (e.g. [17]) although the professor's expected amount of effort for students in the course is identical. The on-line lecture and interactive classroom approach is not the culture at this institution.

5 SUMMARY AND DISCUSSION

We presented a first analog IC design course based on project-based learning and inverted classroom techniques taking advantage of open-source design files, tools, and course materials. The open-source IC design process (Skywater 130nm CMOS) and tools (magic, Xschem) enable fabricating working ICs, providing a realistic student design experience that builds student confidence in designing 10-100 transistor circuits. We overviewed the analog IC design course methodology, the use of hybrid format to increase student conversations, the course structure, and the analog IC design course impact and assessment. This approach enables ECE students to have more interest at higher system levels, abstracting device and circuit information in a careful and yet understandable framework. This analog IC course could be part of an entire circuit design curriculum with hands-on project-based design from the first linear circuits course through graduate level IC courses (e.g. [4, 6]). Having a similar focus starting from linear circuits (e.g. ECE 2040), through device physics (e.g. ECE 3040), and an initial transistor circuits class (e.g. ECE 3400), would set the student culture and expectations for this design course.

The analysis and reflection on the course implementation shows a number of next steps to further improve these techniques. Additional videos on using the open-source tools in the first few course weeks in the course would decrease some student stress. Additional top-level videos in a relaxed format (e.g. [12]) discussing the top-level unity perspective, as well as top-level discussion about design principles (many of our students had minimal design experience) would further improve student understanding. Future semesters would benefit from having industry speakers reinforcing the importance of the core concepts learned in the class, as well as benefit from hearing more about the IC test frame enabling the fabrication of the student's designs. These additions should improve the initial implementation of this analog IC design course.

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