

You have a friend who is a graduate student studying analog integrated circuit design (not at GT) who has made a unique op-amp with differential input and a single-ended output (Fig. 1). This friend learned from one of their classes that CMOS inverters have gain, and made showing such an op-amp (Fig. 1c) the centerpiece of their graduate research. Assume the CMOS inverter has a gain at this supply of 50 and a linear timeconstant, related to bias current, of 1.6ns; a friend did

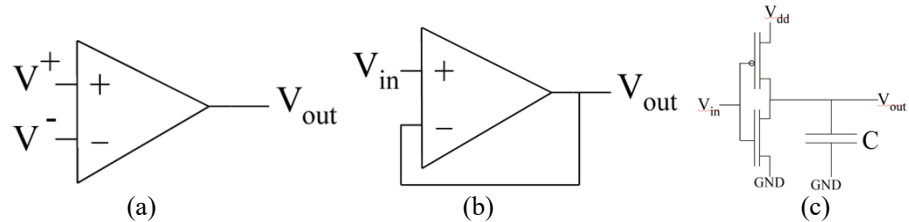


Figure 1: Op-Amp Pictures. (a) Open-loop Amplifier. (b) Unity-gain configuration. (c) CMOS Inverter that can be an amplifier.

the initial linearization for you just before leaving on a several week trip. This individual made an op-amp on an IC (one differential input, and one single output) using two CMOS inverters to achieve an op-amp with a low-frequency gain of 500,000 (Fig. 2). Your friend was very excited that they achieved a good

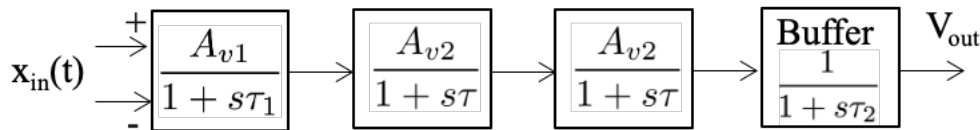


Figure 2: The four-stage CMOS op-amp block diagram. $A_{v1} = 200$, $A_{v2} = 50$. For this design, $\tau_2 = \tau = 1.6\text{ns}$, and $\tau_1 = 16\mu\text{s}$. The differential amplifier (from a differential pair circuit) is sufficiently linear for this discussion (e.g. we are not considering slew rate). The variance (s) of uncorrelated noise at each state variable (white noise) at $10\mu\text{V}$; the output does not experience any further noise.

stable frequency response for an amplifier with a gain of 101 using an ideal feedback divider (feedback of 1% or 0.01). Your friend is writing up this amplifier as a paper, although tells you privately that he had

some issues with making the amplifier connected as a unity gain configuration, but will deal with that question after finishing the paper. Your friend is moving forward with this paper, and excited about seems like a novel configuration.

As you have learned quite abit at GT, particularly in ECE 6550, you have some concerns, although you want to work through a few things before upsetting your friend unnecessarily. No one wants to publish something wrong. You have enough of the circuit structure (Fig. 2) to analyze this system and look at potential control solutions to help your friend's research directions. To help your friend, we come up with a set of questions that we will want to address:

- Create a state equation formulation for this amplifier, and then modify it for the feedback that gives a signal gain of 101 and signal gain of 1 (full feedback). Getting the right normalization will be essential for later analytic calculations. What is the stability of the state matrix in these cases?
- For the gain=1 signal gain case, find the optimal control regulator if you had of the input states and output in these cases, whether the case is stable or unstable. Analyze whether the system is controllable, as well as discuss if it is practically controllable. Assume that voltage measurement and supplies have an equal cost, and uncorrelated to other components.
- As your friend is not from GT, this individual did not think to add any testpoints. Therefore, to control the system, we need to estimate the states of this system. Check whether the system is observable, and create an optimal estimator block for this system.

- Combine the estimator and regulator block into a function. Find the resulting transfer function for your controller component, and discuss the computational elements. What is the transfer function for your entire system, op-amp and controller? Compare this frequency response to the original op-amp transfer function single state equation, and discuss the particular computational element.
- What is the margin of stability, including phase margin, for your resulting op-amp and control system?
- One major issue with CMOS inverters is that their frequency response as an amplifier with gain changes with the power supply. The power supply voltage is a major disturbance for this op-amp structure; if they were at GT, they would have known this issue as well as would have made an internal regulator (e.g. LDO) for the CMOS inverter power supply to achieve a stable bias condition. So a 20mV variation on the power supply (a moderate shift) results in a 2x change in the CMOS amplifier bias currents. What are the worst case transfer functions of your control system and how does your analysis change in this case?
- Your friend might appreciate advice on a new version of this chip to make this approach work. What would you improve or change about this design?

Write a complete report with figures integrated into the electronic document answering these questions.