

Circuit Implementations Teaching a Junior Level Circuits Course Utilizing the SoC FPAA

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Abstract—This paper is grounded in the experiences of our Fall 2016 full FPAA implementation in a junior level class Georgia Tech. This paper focuses on discussing the circuit design implications learned when teaching with a highly configurable IC (SoC FPAA), as well as implications for circuit education. Three questions are addressed in turn: subthreshold and near-threshold MOSFET design as a foundational circuit concept, moving past design of op-amps as a central IC design teaching focus, and programmable transconductance–capacitance filters as fundamental filter approach. Configurable hardware (FPAA) creates a unique position enabling these next directions in circuits and educational applications.

Fall 2016 was the first full implementation of ECE 3400 as a hands-on, design, devices-to-systems course. This first transistor circuits course approach, taught at the junior level, was empowered using large-scale Field Programmable Analog Arrays (FPAA) (ECE 3400) [1]. Utilizing FPAA devices enabled a bold shift towards system-level design. This course implementation started with three key objectives: enable hands-on measurement of multiple circuits, enable students to design different circuits and experimentally measure these components, and enable students to experimentally utilize on-chip system design concepts rather than classic discrete design approaches. The classroom implementation did not require any specialized laboratory spaces, additional human resources, or other technology other than the FPAA boards. Previous papers have discussed the introduction of FPAA devices, such as the SoC FPAA [2], into a graduate course (Analog VLSI, ECE 6435) at Georgia Tech [3], [4], [5], [6], including early discussions on assessment. Some other approaches (e.g. [8], [7]) have built related undergraduate hands-on course structures with multiple off-the-shelf matched components [7] or other potential components [8]. This study opened up the opportunity for wider FPAA deployment in undergraduate curriculums, including implementation in a follow-on mixed-signal analog IC design and layout course this fall semester. A previous paper describes the pedagogical approach transforming ECE 3400 [1]; this course material is available on-line¹.

This paper discusses the resulting circuit education and resulting design implications arising from these new capabilities. We will introduce the implications with a story from the Fall 2016 ECE 3400 class. Roughly two-thirds of the way through the semester, the lecture focused on designing references, starting with discussing the CMOS bootstrap current reference. After many of the students had understood the circuit function,

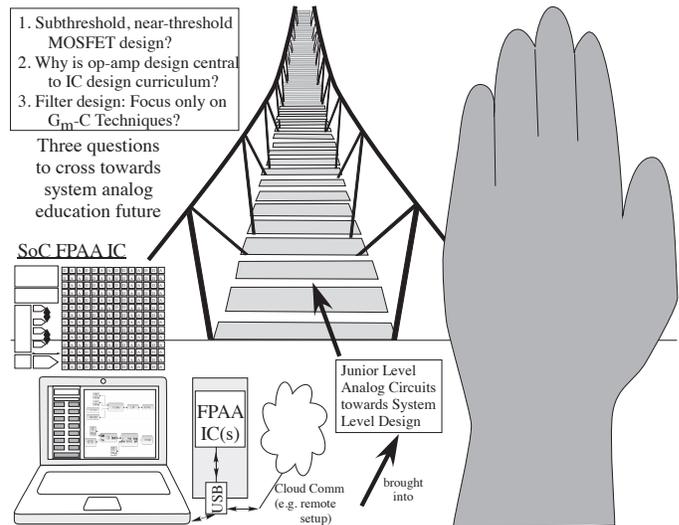


Fig. 1. The bridge to the next generation of circuits teaching as seen through viewing the current GT junior level class. The opportunity arises because of the opportunities for configurable and programmable mixed-signal devices, large-scale Field Programmable Analog Arrays (FPAA), and the maturity of the resulting tool set. Taking advantage of this opportunity requires rethinking (three) technical questions in circuits so that the effort does not end up in the canyon; these issues become clear after teaching a fully implemented course.

one student in the front-row asked in a perplexed manner “how do we program the bootstrap current source?” I gently mentioned the current would be set by the biasing resistor used and resulting transistor ratios. The student responded, “ok, yes, but how do I enter a current into Scilab that is programmed in the reference?” I had to just pause and smile before answering this question, because the teaching approach used for this first full circuits course, taught at the junior level, had made a profound difference in how students approached circuit design. The focus of this paper is to address this different circuit design perspective, birthed out of this unique teaching approach using novel programmable and configurable devices.

Figure 1 shows we must consider three technical questions to cross to move to the system-focused analog education future. Not addressing these questions will send our discussion into the canyon below. Figure 1 illustrates the opportunity arises from recent developments in FPAAs, programmable and configurable ICs, and resulting system infrastructure. The perspective is summarized through three questions.

- Subthreshold and near-threshold MOSFET design?
- Why is op-amp design central to IC design curriculum?

¹<http://users.ece.gatech.edu/phasler/ECE3400>

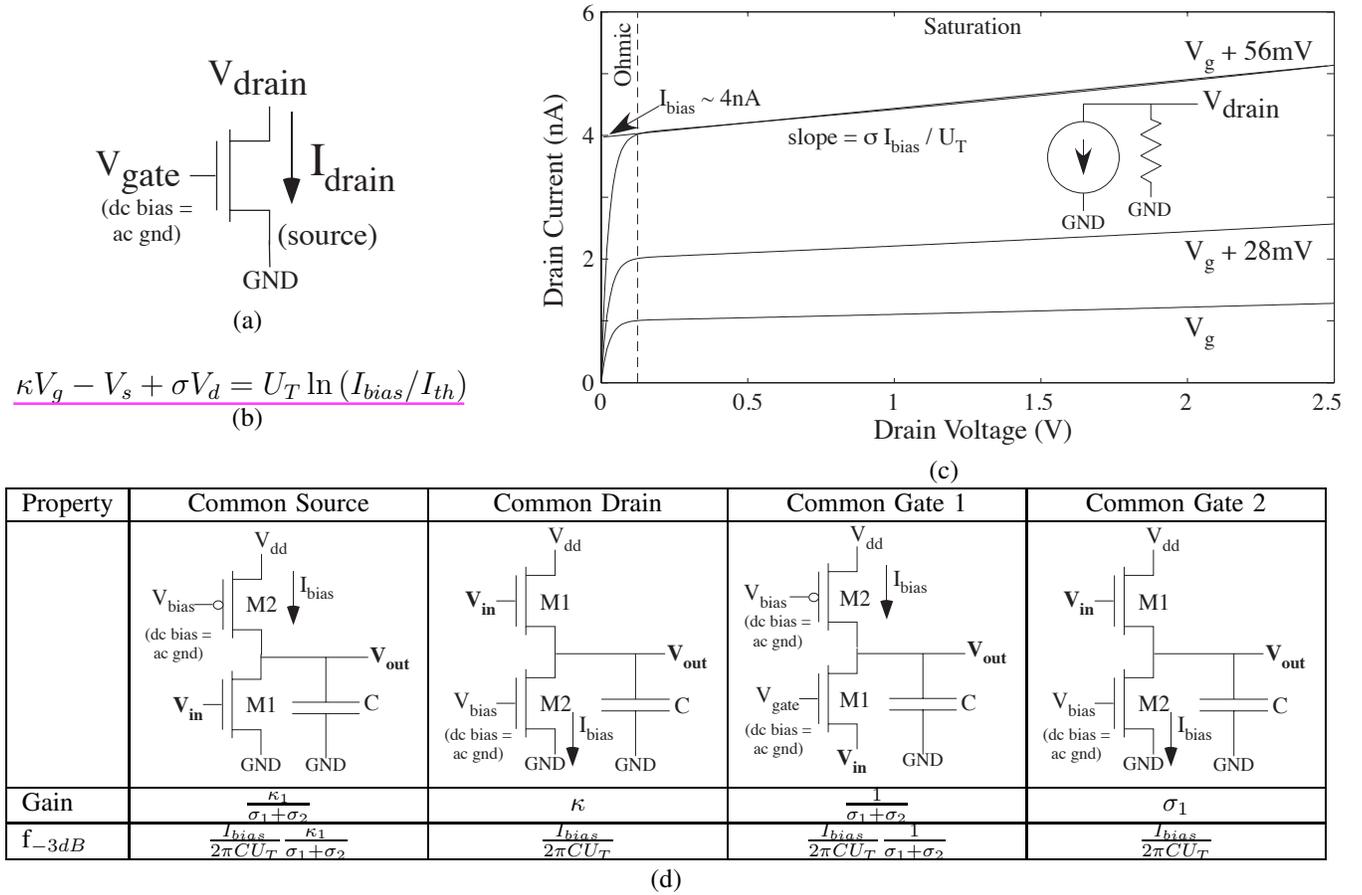


Fig. 2. MOSFET devices are the primary element for integrated circuits. (a) MOSFET circuit diagram. (b) For a fixed bias current (I_{bias}) at the source and drain terminals, we have a (large-signal, static) linear relationship between gate, source, and drain. (c) Drain current versus Drain voltage shows the MOSFET is a gate-controlled current source. (d) From the linear relationship, one gets *four* fundamental circuits by fixing one terminal, apply the input to one terminal, and the resulting equilibrium terminal is the output. The gain and 3dB corner frequency are directly solved and presented below.

- Given Floating-Gate (FG) techniques, why should one not just focus on Transconductance (G_m)–C techniques?

This unique position using configurable hardware enables the next directions in circuits design and education. The following sections address three questions in turn: subthreshold and near-threshold MOSFET design as foundational circuit concept, moving past design of op-amps as central IC design teaching focus, and programmable transconductance–capacitance filters as fundamental filter approach.

I. SUBTHRESHOLD AND NEAR-THRESHOLD MOSFET CURRENT SOURCE TECHNIQUES

The first section asserts that the starting transistor device and circuit concepts should be MOSFET transistors operating in sub threshold operation utilized as approximate current sources. A MOSFET operating with sub threshold bias currents (as in Fig. 2a) is the nearly ideal case of a single-band voltage-controlled barrier; because of the direct BJT connection to the base terminal, one must consider the interaction between two related (conduction and valence) barriers. Starting with a voltage-controlled barrier as an ideal active device generalizes to most active devices going forward, even newer nano electronic devices. MOSFET devices have a saturation and ohmic region both for subthreshold and for above-

threshold operation, with consistent modeling throughout the operating regimes [9]. For a subthreshold device operating in saturation [10], [11],

$$I_s = I_{th} e^{(\kappa(V_g - V_{T0}) - V_s + \sigma V_d) / U_T} \quad (1)$$

where κ is the coupling between the gate terminal and the surface potential at the source edge, σ is the coupling between the drain terminal and the surface potential at the source edge, V_{T0} is the threshold voltage, and I_{th} would be the threshold current, which is a weak function of temperature (T^n , where n is between 0 and $\frac{1}{2}$). One equation models the subthreshold MOSFET, where the source-to-channel barrier dominates the transistor operation. Data verifies the MOSFET model, including the temperature dependance [10], [11]. EKV simulation [9] within the FPAA tool framework is enabled [12]. As MOSFETs scale to smaller IC processes, one has less and less usable above-threshold operation, so the primary operation is subthreshold or near threshold operation. Once students understand subthreshold devices and fundamental circuits, then these students are prepared to understand above-threshold MOSFET operation, particularly the diminishing returns made as tradeoffs push to higher bias currents.

The approach moves towards using programmable transistors acting as approximate current sources. The common

Property	Transconductance Topology	Folded Cascode Topology	Two-Stage Amplifier Topology
Circuit			
Unity Gain Freq.	$\frac{I_{bias}}{2\pi C U_T}$	$\frac{I_{bias}}{2\pi C U_T}$	$\frac{I_{bias}}{2\pi C U_T}$
Gain	$\frac{\kappa_1/2}{\sigma_8\sigma_9+\sigma_5\sigma_{10}}$	$\frac{\kappa_1/2}{\sigma_8\sigma_{10}+\sigma_6(\sigma_3+\sigma_1)}$	$\frac{\kappa_1\kappa_5/2}{(\sigma_2+\sigma_4)(\sigma_5+\sigma_6)}$
Power	$2V_{dd}I_{bias}$	$2V_{dd}I_{bias}$	$2V_{dd}I_{bias}$
Noise/ \sqrt{Hz} (input ref.)	$(qU_T/\kappa_1)\sqrt{8 \times 2/(qI_{bias})}$ $= (4qU_T/\kappa_1)/\sqrt{(qI_{bias})}$	$= (4qU_T/\kappa_1)/\sqrt{(qI_{bias})}$	$= (2qU_T/\kappa_1)/\sqrt{(qI_{bias})}$
Slew Rate	I_{bias} / C	I_{bias} / C	I_{bias} / C

Fig. 3. Main amplifier topologies and typical op-amp parameters. Even with some small optimizations, one gets similar results in most cases. The Transconductance Amp (TA) topology gives the most flexibility, particularly regarding a range of output load capacitances. Parameters calculated for subthreshold I_{bias} and load capacitance C . For the two-stage amplifier, we assume $C_c = C$, resulting in phase margin of 45° ; larger capacitances decrease the phase margin. Noise improvement in two-stage amplifier can be accomplished in the other two topologies by getting voltage gain in the early stage (M1-M4).

lore among circuit's education for more than two decades is that struggle struggle with active current source design far more than resistive biasing, even though most would agree active current source techniques are central to *real* circuit design. The classical circuits perspective assumes that students struggle with using transistors as current sources until they have far more circuits knowledge (e.g. look at the presentation in classic IC design textbooks [13], [14]). Figure 2c, shows the transistor (drain) characteristic closely resembles a current source after 100mV; therefore, the device physics drives the circuit interpretation. The transistor is an ideal current source for $\sigma = 0$. Fundamentally, the issue seems historical. Solving transistors with resistive components is not easier than solving transistor-only circuits. The difference in functions (e^x vs. x) for transistor-resistive circuits seems harder, requiring all solutions using small-signal techniques, and students completely missing basic voltage biasing concepts.

MOSFET subthreshold saturation behavior from (1) establishes the four fundamental two transistor MOSFET circuits by roughly fixing the bias current (I_{bias}). Figure 2b shows a transistor has a linear relationship with a fixed bias current. Four fundamental circuit types (Fig. 2d) follow from a current source constraining a transistor, fixing one terminal, setting one terminal as the input, and allowing the remaining free parameter as the output. The gate voltage can not be an output. Consider one of the two-transistor circuits, the common-source amplifier (Fig. 2d) When M1 and M2 are in saturation

$$\begin{aligned}
& I_{th1}e^{(\kappa_1((V_{in}-V_{T0n})+\sigma_1V_{out}))/U_T} \\
& = I_{th2}e^{(\kappa_2(V_{dd}-V_{bias}-V_{T0p})+\sigma_2(V_{dd}-V_{out}))/U_T} \\
& \text{Gain} = \frac{\Delta V_{out}}{\Delta V_{in}} = -\frac{\kappa_1}{\sigma_1 + \sigma_2} \quad (2)
\end{aligned}$$

where ΔV_{out} , ΔV_{in} are the change from fixed potentials. The gain is large-signal linear, to first order insensitive of temperature, and independent of I_{bias} . The circuit is a balance between coupling of gate to surface potential and coupling of drain to surface potential. All four techniques in Fig. 2 have simple results composed of physical parameters, with time constants proportional to the chosen I_{bias} . FG techniques empowers subthreshold circuit design by countering the effect of V_{T0} mismatch, and enabling a range of designed linear-range possibilities. From a research or educational perspective, the SoC FPAA's (and related devices) utilize FG circuits everywhere. Above threshold is similar, although the Early effect and DIBL effect have different functional forms, leading to a lower maximum gain with increasing overdrive voltage.

II. MOVING PAST OP-AMP DESIGN AS CENTRAL IC DESIGN TEACHING FOCUS

The second section asserts that programming-enabled, system level design no longer centers around the historical op-amp design as the fundamental circuit goal. This issue became crystal clear while teaching a system-focus junior-level circuits course utilizing FPAA devices. Op-amp design has been the primary focus for analog circuit design for nearly 50 years, both in learning how to design op-amps, as well as building circuits with op-amps. After teaching fundamental circuits in Fig. 2 and related elements (e.g. differential-pairs, cascode, source-degeneration), the number of different op-amp designs are both straight-forward and all techniques yield similar results (Fig. 3), particularly for sub threshold bias currents. Further, experience teaching graduate system-level IC design courses rarely make use of traditional op-amps, and the resulting design must be entirely redone.

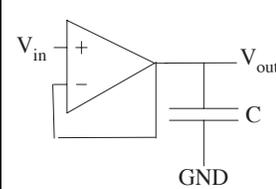
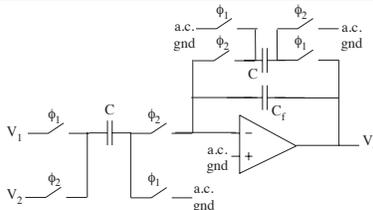
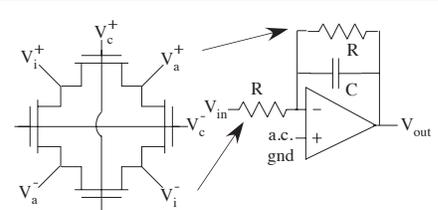
Property	Transcond-Cap Filters	Switched Cap filters	Linearized MOSFET filters
			
Corner Frequency	$\frac{I_{bias}}{2\pi C U_T} \frac{C_1}{C_T}$	$\frac{C_f}{fC}$	$\frac{C U_T}{\sigma_R I_{bias}}$
Linear Range	$\frac{U_T}{\kappa} \frac{C_T}{C_1}$	V_{dd} - headroom	$\frac{U_T}{\sigma_R}$
Total Noise (Output, V)	$\sqrt{\frac{q U_T}{C}}$	$\sqrt{\frac{2q U_T}{C}} + \sqrt{\frac{q U_T}{C_f}}$ + Amp noise + charge feedthrough	$\sqrt{\frac{q U_T}{C}}$ + Amp noise
Power	$2 I_{bias} V_{dd}$	$\gg 2 I_{bias} V_{dd}$	$\gg 2 I_{bias} V_{dd}$

Fig. 4. Comparison of unity gain, first-order filter topologies. Transistor-Capacitor Circuit: FG OTA device, C_1 is input FG cap, C_T is total cap at FG node. FG programmed current source sets the corner frequency. Switched-Capacitor Circuit: Switches and capacitors emulate resistive devices in this configuration. Capacitor matching is an essential technique, often resulting in large capacitors. f is the clock frequency, setting the resulting corner frequency. The amplifier must operate at a frequency (unity gain) much higher than the corner frequency. Linearized-Resistor Circuit: Linearized transistors, the 4-transistor circuit, are used as programmable resistive devices. The subthreshold, saturated linearized MOSFET filter calculations [15], enable a large linear range for subthreshold bias currents. σ_R the sigma setting the linearized resistor. The amplifier operate at a frequency (unity gain) much higher than the corner frequency.

The resulting material is roughly a week of lectures, focusing heavily on one topology and then showing differences in the other two cases. From our experience, shown by the analysis in Fig. 3, the Transconductance Amplifier (TA) topology becomes the most effective topology, particularly for a wide range of potential capacitance loads, and directly follows previous circuit discussions (diff-pair, cascodes). Subthreshold approach enables large-signal calculations for each of the structures in Fig. 3. These concepts illustrate the design of these structures could be completely automated if needed. For FPAA devices, one finds only a few programmable TA amplifier designs seem to cover most applications. Biasing is already available in these FPAA devices, including biasing of cascade voltages; one can teach bias structures (e.g. bootstrap current source) by illustrating the FPAA IC infrastructure.

FPAA devices already have programmable TA devices available. Doing a project to design such a structure just with transistors becomes awkward. A reasonable approach seems to include op-amp circuits for a week of lecture, probably part of a set of exam questions, and the class can proceed on from that point. Op-amps are also used at the classic problem for two-pole stability with feedback, even though one can find many simpler circuits (e.g. Delbruck's adaptive photoreceptor [16]) to directly illustrate this issue. One can cover all of the advanced op-amp topologies in advanced graduate courses for the experts who are excited about those opportunities.

III. PROGRAMMABLE G_m -CAPACITANCE CIRCUITS AS FUNDAMENTAL FILTER / SYSTEM APPROACH

The third section asserts that concentrating on Transconductance (G_m)-Capacitance circuit approaches is both sufficient for developing filter and system circuits to use for teaching, and enables the highest performance possible for programmable analog design. G_m techniques elegantly uses the

available device physics and time constants for the resulting system. These techniques are known for the highest frequency corner for given I_{bias} , the lowest noise for a given I_{bias} , and resulting lowest system power. A single approach enables a simple configurable framework to teach that scales up to higher functions, enabling continuous-time processing. FPAA devices have many TA elements; TA elements and transistors require similar FPAA complexity (3 pins each).

The two issues about using G_m -C filters and systems are directly solved using FG techniques. Figure 4 shows the parameters for a FG based G_m -C approach. First, G_m -C elements require a method of setting the bias voltages to account for fabrication variations in transistors and capacitors. FG biasing set nonvolatile analog devices to compensate for these effects as well as other biases. FPAAs recently demonstrated G_m -C built-in self-test capability [17]. Second, G_m -C filters and systems often have limited linearity, resulting in distortion, particularly from differential transistor-pairs. Any improvement in linearity requires decreasing the G_m / I_{bias} by the same amount of the increasing linearity. FG approaches allow for capacitive dividers to decrease this ratio exactly by the amount required with no additional added transistor noise; one wants to use just enough linearity to not degrade G_m / I_{bias} and therefore degrade other metrics (noise, frequency response, power). Typical FPAA approaches allow for a few linear-range choices, giving sufficient linearity (and not too much) for most applications. Other approaches (Fig. 4) utilize oversampling and slew-rate based circuits (e.g. switched capacitor filters) with corresponding high power requirements and charge feedthrough limitations to achieve high SNR approaches, or linearized transistor elements, where linearity requires at least lower G_m / I_{bias} , additional noise, and requiring a sufficient op-amp circuit.

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