CHAPTER 9 -SWITCHED CAPACITOR CIRCUITS

Outline

9.1 - SWITCHED CAPACITOR CIRCUITS

RESISTOR EMULATION

Switched capacitor circuits are not new.
James Clerk Maxwell used switches and a capacitor to measure the equivalent resistance of a galvanometer in the 1860's.

Parallel Switched Capacitor Equivalent Resistor:

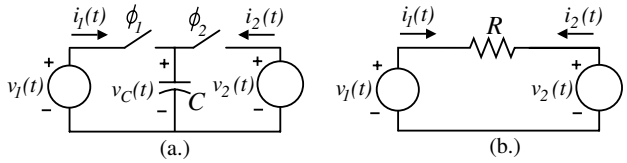


Figure 9.1-1 (a.) Parallel switched capacitor equivalent resistor.
(b.) Continuous time resistor of value R.

Two-Phase, Nonoverlapping Clock:

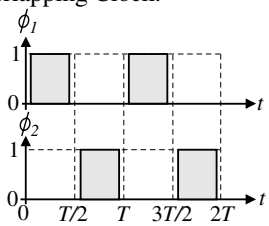


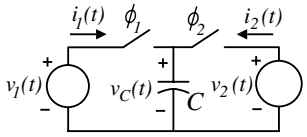
Figure 9.1-2 - Waveforms of a typical two-phase, nonoverlapping clock scheme.

EQUIVALENT RESISTANCE OF A SWITCHED CAPACITOR CIRCUIT

Assume that $v_1(t)$ and $v_2(t)$ are changing slowly with respect to the clock period.

The average current is,

$$i_1(average) = \frac{1}{T}\int_0^T i_1(t)dt = \frac{1}{T}\int_0^{T/2} i_1(t)dt$$



Charge and current are related as,

$$i_1(t) = \frac{dq_1(t)}{dt}$$

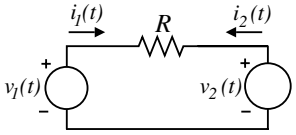
Substituting this in the above gives,

$$i_1(average) = \frac{1}{T}\int_0^{T/2} dq_1(t) = \frac{q_1(T/2)-q_1(0)}{T} = \frac{Cv_C(T/2)-Cv_C(0)}{T}$$

However, $v_C(T/2) = v_1(T/2)$ and $v_C(0) = v_2(0)$. Therefore,

$$i_1(average) = \frac{C\,[v_1(T/2)-v_2(0)]}{T} \approx \frac{C\,[V_1-V_2]}{T}$$

For the continuous time circuit:



$$\Rightarrow i_1(average) = \frac{V_1-V_2}{R} \quad \therefore \quad \boxed{R \approx \frac{T}{C}}$$

For $v_1(t) \approx V_1$ and $v_2(t) \approx V_2$, the signal frequency must be much less than f_c.

EXAMPLE 9.1 - Design of a Parallel Switched Capacitor Resistor Emulation

If the clock frequency of parallel switched capacitor equivalent resistor is 100kHz, find the value of the capacitor C that will emulate a 1MΩ resistor.

Solution

The period of a 100kHz clock waveform is 10μsec. Therefore, using the previous relationship, we get that

$$C = \frac{T}{R} = \frac{10^{-5}}{10^{6}} = 10\text{pF}$$

We know from previous considerations that the area required for 10pF capacitor is much less than for a 1MΩ resistor when implemented in CMOS technology.

POWER DISSIPATION IN THE RESISTANCE EMULATION

If the switched capacitor circuit is an equivalent resistance, how is the power dissipated?

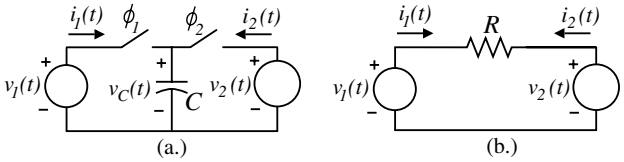


Figure 9.1-1 (a.) Parallel switched capacitor equivalent resistor.
(b.) Continuous time resistor of value R.

Continuous Time Resistor:

$$\text{Power} = \frac{(V_1 - V_2)^2}{R}$$

Discrete Time Resistor Emulation:

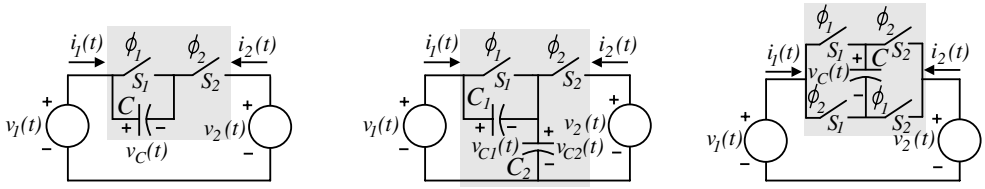
Assume the switches have an ON resistance of R_{on}. The power dissipated per clock cycle is,

$$\text{Power} = i_1(\text{aver.})(V_1 - V_2) \text{ where } i_{1\ (\text{aver.})} = \frac{(V_1 - V_2)}{R_{on}T}\int_0^T e^{-t/(R_{on}C)}dt$$

$$\therefore \quad \text{Power} = \frac{(V_1 - V_2)^2}{TR_{on}}\int_0^T e^{-t/(R_{on}C)}dt = \frac{(V_1 - V_2)^2}{(T/C)}\left[-e^{-T/(R_{on}C)} + 1\right] \approx \frac{(V_1 - V_2)^2}{(T/C)} \quad \text{if } T >> R_{on}C$$

Thus, if $R = T/C$, then the power dissipation is identical in the continuous time and discrete time realizations.

OTHER SWITCHED CAPACITOR EQUIVALENT RESISTANCE CIRCUITS



Series Series-Parallel Bilinear

Series-Parallel:

The current, $i_1(t)$, that flows during both the ϕ_1 and ϕ_2 clocks is:

$$i_1(average) = \frac{1}{T}\int_0^T i_1(t)dt = \frac{1}{T}\left(\int_0^{T/2} i_1(t)dt + \int_{T/2}^T i_1(t)dt\right) = \frac{q_1(T/2) - q_1(0)}{T} + \frac{q_1(T) - q_1(T/2)}{T}$$

Therefore, $i_1(average)$ can be written as,

$$i_1(average) = \frac{C_2[v_{C2}(T/2) - v_{C2}(0)]}{T} + \frac{C_1[v_{C1}(T) - v_{C1}(T/2)]}{T}$$

The sequence of switches cause, $v_{C2}(0) = V_2$, $v_{C2}(T/2) = V_1$, $v_{C1}(T/2) = 0$, and $v_{C1}(T) = V_1 - V_2$. Applying these results gives

$$i_1(average) = \frac{C_2[V_1 - V_2]}{T} + \frac{C_1[V_1 - V_2 - 0]}{T} = \frac{(C_1 + C_2)(V_1 - V_2)}{T}$$

Equating the average current to the continuous time circuit gives:

$$\boxed{R = \frac{T}{C_1 + C_2}}$$

EXAMPLE 9.1-2 - Design of a Series-Parallel Switched Capacitor Resistor Emulation

If $C1 = C2 = C$, find the value of C that will emulate a 1MΩ resistor if the clock frequency is 250kHz.

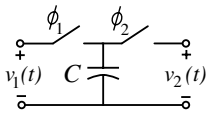
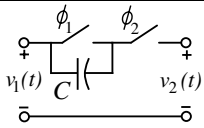
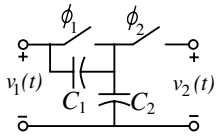
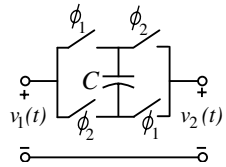
Solution

The period of the clock waveform is 4μsec. Using above relationship we find that C is given as,

$$2C = \frac{T}{R} = \frac{4\text{x}10^{-6}}{10^{6}} = 4\text{pF}$$

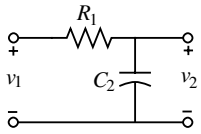
Therefore, $C1 = C2 = C = 2\text{pF}$.

SUMMARY OF THE FOUR SWITCHED CAPACITOR RESISTANCE CIRCUITS

Switched Capacitor Resistor Emulation Circuit	Schematic	Equivalent Resistance
Parallel		$\frac{T}{C}$
Series		$\frac{T}{C}$
Series-Parallel		$\frac{T}{C_1 + C_2}$
Bilinear		$\frac{T}{4C}$

ACCURACY OF SWITCHED CAPACITOR CIRCUITS

Consider the following continuous time, first-order, low pass circuit:



The transfer function of this simple circuit is,

$$H(j\omega) = \frac{V_2(j\omega)}{V_1(j\omega)} = \frac{1}{j\omega R_1 C_2 + 1} = \frac{1}{j\omega\tau_1 + 1}$$

where $\tau_1 = R_1C_2$ is the time constant of the circuit and determines the accuracy.

Continuous Time Accuracy

Let $\tau_1 = \tau_C$. The accuracy of τ_C can be expressed as,

$$\frac{d\tau_C}{\tau_C} = \frac{dR_1}{R_1} + \frac{dC_2}{C_2} \quad \Rightarrow \text{ 5\% to 20\% depending on the size of the components}$$

Discrete Time Accuracy

Let $\tau_1 = \tau_D = \left(\frac{T}{C_1}\right) C_2 = \left(\frac{1}{f_c C_1}\right) C_2$. The accuracy of τ_D can be expressed as,

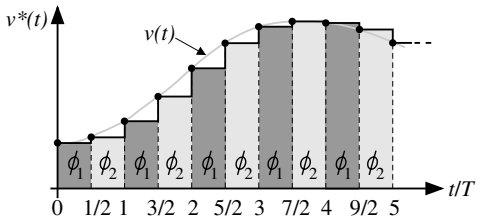
$$\frac{d\tau_D}{\tau_D} = \frac{dC_2}{C_2} - \frac{dC_1}{C_1} - \frac{df_c}{f_c} \quad \Rightarrow \quad \text{0.1\% to 1\% depending on the size of components}$$

The above is the primary reason for the success of switched capacitor circuits in CMOS technology.

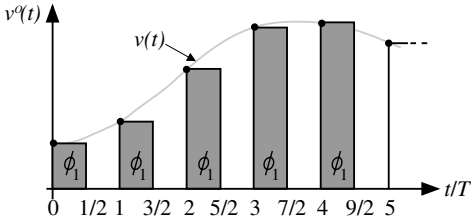
ANALYSIS METHODS FOR TWO-PHASE, NONOVERLAPPING CLOCKS

Sampled Data Voltage Waveforms for a Two-phase Clock:

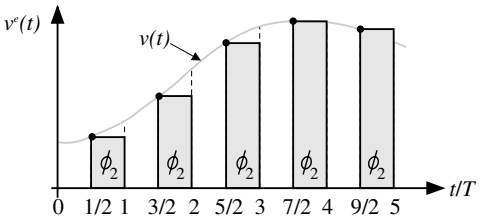
A sampled-data voltage waveform for a two-phase clock.



A sampled-data voltage waveform for the odd-phase clock.



A sampled-data voltage waveform for the even-phase clock.



ANALYSIS METHODS FOR TWO-PHASE, NONOVERLAPPING CLOCKS - CONT'D

Time-domain Relationships:

The previous figure showed that,

$$v^*(t) = v^o(t) + v^e(t)$$

where the superscript *o* denotes the odd phase (ϕ_1) and the superscript *e* denotes the even phase (ϕ_2).

For any given sample point, $t = nT/2$, the above may be expressed as

$$v^*\left(\frac{nT}{2}\right)_{n=1,2,3,4,5,6,\cdots} = v^o\left(\frac{nT}{2}\right)_{n=1,3,5,\cdots} + v^e\left(\frac{nT}{2}\right)_{n=2,4,5,\cdots}$$

z-domain Relationships:

Consider the one-sided z-transform of a sequence, $v(nT)$, defined as

$$V(z) = \sum_{n=0}^{\infty} v(nT)z^{-n} = v(0) + v(T)z^{-1} + v(2T)z^{-2} + \cdots$$

for all z for which the series $V(z)$ converges.

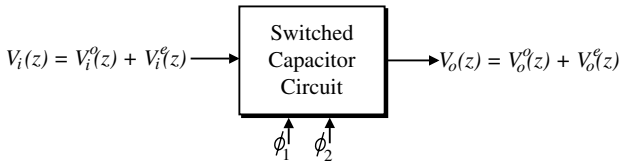
Now, this equation can be expressed in the z-domain as

$$V^*(z) = V^o(z) + V^e(z)\,.$$

The z-domain format for switched capacitor circuits will allow us to analyze transfer functions.

TRANSFER FUNCTION VIEWPOINT OF SWITCHED CAPACITOR CIRCUITS

Input-output voltages of a general switched capacitor circuit in the z-domain.



z-domain transfer functions:

$$H^{ij}(z) = \frac{V_o^j(z)}{V_i^i(z)}$$

where i and j can be either e or o. For example, $H^{oe}(z)$ represents $V_o^e(z)/V_i^o(z)$. Also, a transfer function, H(z) can be defined as

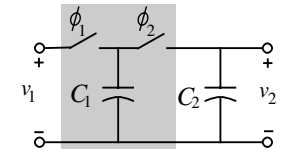
$$H(z) = \frac{V_o(z)}{V_i(z)} = \frac{V_o^e(z) + V_o^o(z)}{V_i^e(z) + V_i^o(z)}\,.$$

APPROACH FOR ANALYZING SWITCHED CAPACITOR CIRCUITS

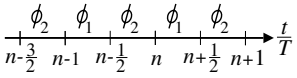
1.) Analyze the circuit in the time-domain during a selected phase period.
2.) The resulting equations are based on $q = Cv$.
3.) Analyze the following phase period carrying over the initial conditions from the previous analysis.
4.) Identify the time-domain equation that relates the desired voltage variables.
5.) Convert this equation to the z-domain.
6.) Solve for the desired z-domain transfer function.
7.) Replace z by $e^{j\omega T}$ and examine the frequency response.

EXAMPLE 9.1-3 - Analysis of a Switched Capacitor, First-order, Low pass Filter

Use the above approach to find the z-domain transfer function of the first-order, low pass switched capacitor circuit shown below. This circuit was developed by replacing the resistor, R_1, of the previous circuit with the parallel switched capacitor resistor circuit. The timing of the clocks is also shown. This timing is arbitrary and is used to assist the analysis and does not change the result.



Switched capacitor, low pass filter.

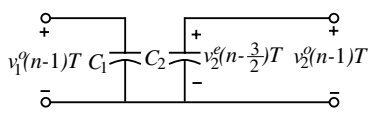


Clock phasing for this example.

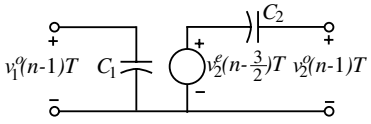
Solution

$\underline{\phi_1: (n\text{-}1)T < t < (n\text{-}0.5)T}$

Equivalent circuit:



Equivalent circuit.



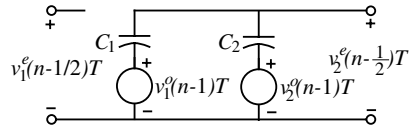
Simplified equivalent circuit.

The voltage at the output (across C_2) is $v_2^o(n\text{-}1)T = v_2^e(n\text{-}3/2)T$ (1)

EXAMPLE 9.1-3 - Continued

$\underline{\phi_2}$: $\underline{(n\text{-}0.5)T < t < nT}$

Equivalent circuit:



The output of this circuit can be expressed as the superposition of two voltage sources, $v_1^o\,(n\text{-}1)T$ and $v_2^o\,(n\text{-}1)T$ given as

$$v_2^e\,(n\text{-}1/2)T = \left(\frac{C_1}{C_1+C_2}\right) v_1^o\,(n\text{-}1)T + \left(\frac{C_2}{C_1+C_2}\right) v_2^o\,(n\text{-}1)T. \tag{2}$$

If we advance Eq. (1) by one full period, T, it can be rewritten as

$$v_2^o(n)T = v_2^e\,(n\text{-}1/2)T. \tag{3}$$

Substituting, Eq. (3) into Eq. (2) yields the desired result given as

$$v_2^o\,(nT) = \left(\frac{C_1}{C_1+C_2}\right) v_1^o\,(n\text{-}1)T + \left(\frac{C_2}{C_1+C_2}\right) v_2^o\,(n\text{-}1)T. \tag{4}$$

EXAMPLE 9.1-3 - Continued

$\underline{\text{z-domain Analysis}}$

The next step is to write the z-domain equivalent expression for Eq. (4). This can be done term by term using the sequence shifting property given as

$$v(n\text{-}n_1)T \;\leftrightarrow\; z^{-n_1}V(z)\,. \tag{5}$$

The result is

$$V_2^o(z) = \left(\frac{C_1}{C_1+C_2}\right) z^{-1}\; V_1^o(z) + \left(\frac{C_2}{C_1+C_2}\right) z^{-1}\; V_2^o(z). \tag{6}$$

Finally, solving for $V_2^o(z)/V_1^o(z)$ gives the desired z-domain transfer function for the switched capacitor circuit of this example as

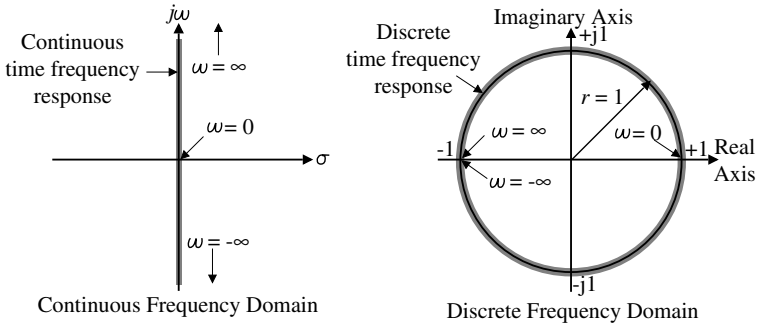
$$H^{oo}(z) = \frac{V_2^o(z)}{V_1^o(z)} = \frac{z^{-1}\left(\frac{C_1}{C_1+C_2}\right)}{1 - z^{-1}\left(\frac{C_2}{C_1+C_2}\right)} = \frac{z^{-1}}{1 + \alpha - \alpha z^{-1}}\;, \text{ where } \alpha = \frac{C_2}{C_1}. \tag{7}$$

DISCRETE-FREQUENCY DOMAIN ANALYSIS

Relationship between the continuous and discrete frequency domains:

$$z = e^{j\omega T}$$

Illustration:



EXAMPLE 9.1-4 - Frequency Response of Example 9.1-3

Use the results of the previous example to find the magnitude and phase of the discrete time frequency response for the switched capacitor circuit of Fig. 9.1-7a.

Solution

The first step is to replace z in Eq. (9) of Ex. 9.1-3 by $e^{j\omega T}$. The result is given below as

$$H^{oo}(e^{j\omega T}) = \frac{e^{-j\omega T}}{1+\alpha-\alpha\, e^{-j\omega T}} = \frac{1}{(1+\alpha)e^{j\omega T}-\alpha} = \frac{1}{(1+\alpha)cos(\omega T)-\alpha+j(1+\alpha)sin(\omega T)} \tag{1}$$

where we have used Eulers formula to replace $e^{j\omega T}$ by $cos(\omega T)+jsin(\omega T)$. The magnitude of Eq. (1) is found by taking the square root of the square of the real and imaginary components of the denominator to give

$$\begin{aligned} |H^{oo}| &= \frac{1}{\sqrt{(1+\alpha)^2cos^2(\omega T) - 2\alpha(1+\alpha)cos(\omega T) + \alpha^2 + (1+\alpha)^2sin^2(\omega T)}} \\ &= \frac{1}{\sqrt{(1+\alpha)^2[cos^2(\omega T)+sin^2(\omega T)]+\alpha^2-2\alpha(1+\alpha)cos(\omega T)}} \\ &= \frac{1}{\sqrt{1+2\alpha+\alpha^2-2\alpha(1+\alpha)cos(\omega T)}} = \frac{1}{\sqrt{1+2\alpha(1+\alpha)(1-cos(\omega T))}}\ . \end{aligned} \tag{2}$$

The phase shift of Eq. (1) is expressed as

$$\text{Arg}[H^{oo}] = -tan^{-1}\left[\frac{(1+\alpha)sin(\omega T)}{(1+\alpha)cos(\omega T)-\alpha}\right] = -tan^{-1}\left[\frac{sin(\omega T)}{cos(\omega T)-\frac{\alpha}{1+\alpha}}\right] \tag{3}$$

THE OVERSAMPLING ASSUMPTION

The oversampling assumption is simply to assume that $f_{signal} << f_{clock} = f_c$.

This means that,

$$f_{signal} = f << \frac{1}{T} \quad \Rightarrow \quad 2\pi f = \omega << \frac{2\pi}{T} \quad \Rightarrow \quad \omega T << 2\pi.$$

The importance of the oversampling assumption is that is permits the design of switched capacitor circuits that approximates the continuous time circuit until the signal frequency begins to approach the clock frequency.

EXAMPLE 9.1-5 - Design of Switched Capacitor Circuit and Resulting Frequency Response

Design the first-order, low pass, switched capacitor circuit of Ex. 9.1-3 to have a *-3dB* frequency at 1kHz. Assume that the clock frequency is 20kHz Plot the frequency response for the resulting discrete time circuit and compare with a first-order, low pass, continuous time filter.

Solution

If we assume that ωT is less than unity, then $cos(\omega T)$ approaches 1 and $sin(\omega T)$ approaches ωT. Substituting these approximations into the magnitude response of Eq. (2) of Ex. 9.1-4 results in

$$H^{oo}(e^{j\omega T}) \approx \frac{1}{(1+\alpha) - \alpha + j(1+\alpha)\omega T} = \frac{1}{1 + j(1+\alpha)\omega T}. \qquad (1)$$

Comparing this equation to the simple, first-order, low pass continuous time circuit results in the following relationship which permits the design of the circuit parameter α.

$$\omega\tau_1 = (1+\alpha)\omega T \qquad (2)$$

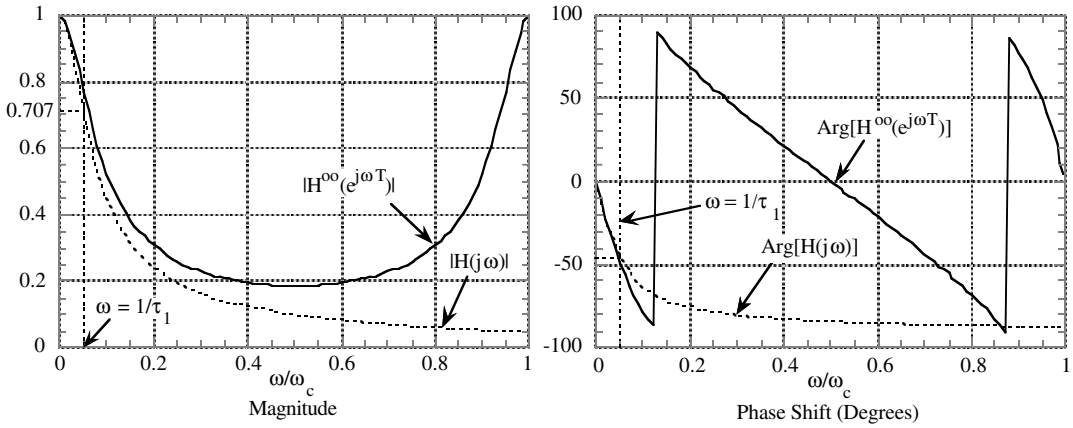
Solving for α gives

$$\alpha = \frac{\tau_1}{T} - 1 = f_c\tau_1 - 1 = \frac{f_c}{\omega_{-3dB}} - 1 = \frac{\omega_c}{2\pi\omega_{-3dB}} - 1 . \qquad (3)$$

Using the values given, we see that $\alpha = (20/6.28)-1 = 2.1831$. Therefore, $C_2 = 2.1831C_1$.

EXAMPLE 9.1-5 - Continued

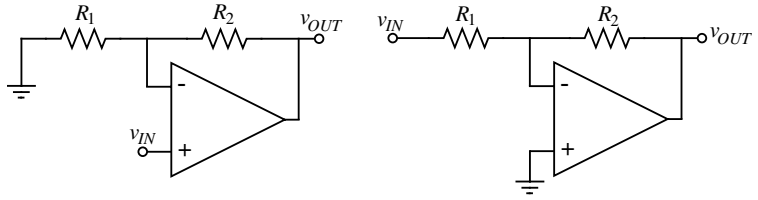
Frequency Response of the First-order, Switched Capacitor, Low Pass Circuit:



Better results would be obtained if $f_c > 20$kHz.

9.2- SWITCHED CAPACITOR AMPLIFIERS

CONTINUOUS TIME AMPLIFIERS



Gain and GB = ∞:

$$\frac{V_{out}}{V_{in}} = \frac{R_1+R_2}{R_1} \qquad \frac{V_{out}}{V_{in}} = -\frac{R_2}{R_1}$$

Gain ≠ ∞, GB = ∞:

$$\frac{V_{out}}{V_{in}} = \frac{A_{vd}(0)}{1+\frac{A_{vd}(0)R_1}{R_1+R_2}} = \left(\frac{R_1+R_2}{R_1}\right)\frac{\frac{A_{vd}(0)\,R_1}{R_1+R_2}}{1+\frac{A_{vd}(0)R_1}{R_1+R_2}} \qquad \frac{V_{out}}{V_{in}} = \frac{\frac{-R_2A_{vd}(0)}{R_1+R_2}}{1+\frac{A_{vd}(0)R_1}{R_1+R_2}} = -\left(\frac{R_2}{R_1}\right)\frac{\frac{R_1A_{vd}(0)}{R_1+R_2}}{1+\frac{A_{vd}(0)R_1}{R_1+R_2}}$$

Gain ≠ ∞, GB ≠ ∞:

$$\frac{V_{out}(s)}{V_{in}(s)} = \left(\frac{R_1+R_2}{R_1}\right)\frac{\frac{GB\cdot R_1}{R_1+R_2}}{s+\frac{GB\cdot R_1}{R_1+R_2}} = \left(\frac{R_1+R_2}{R_1}\right)\frac{\omega_H}{s+\omega_H} \qquad \frac{V_{out}(s)}{V_{in}(s)} = \left(-\frac{R_2}{R_1}\right)\frac{\frac{GB\cdot R_1}{R_1+R_2}}{s+\frac{GB\cdot R_1}{R_1+R_2}} = \left(-\frac{R_2}{R_1}\right)\frac{\omega_H}{s+\omega_H}$$

EXAMPLE 9.2-1- Accuracy Limitation of Voltage Amplifiers due to a Finite Voltage Gain

Assume that the noninverting and inverting voltage amplifiers have been designed for a voltage gain of +10 and -10. If $A_{vd}(0)$ is 1000, find the actual voltage gains for each amplifier.

Solution

For the noninverting amplifier, the ratio of R_2/R_1 is 9.

$$A_{vd}(0)R_1/(R_1+R_2) = \frac{1000}{1+9} = 100.$$

$$\therefore \quad \frac{V_{out}}{V_{in}} = 10\left(\frac{100}{101}\right) = 9.901 \text{ rather than } 10.$$

For the inverting amplifier, the ratio of R_2/R_1 is 10.

$$\frac{A_{vd}(0)R_1}{R_1+R_2} = \frac{1000}{1+10} = 90.909$$

$$\therefore \quad \frac{V_{out}}{V_{in}} = -(10)\left(\frac{90.909}{1+90.909}\right) = -9.891 \text{ rather than } -10.$$

EXAMPLE 9.2-2 - -3*dB* Frequency of Voltage Amplifiers due to Finite Unity-Gainbandwidth

Assume that the noninverting and inverting voltage amplifiers have been designed for a voltage gain of +1 and -1. If the unity-gainbandwidth, *GB*, of the op amps are 2πMrads/sec, find the upper -3*dB* frequency for each amplifier.

Solution

In both cases, the upper -3*dB* frequency is given by

$$\omega_H = \frac{GB \cdot R_1}{R_1+R_2}$$

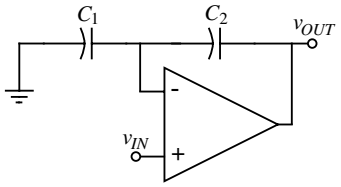
For the noninverting amplifier with an ideal gain of +1, the value of R_2/R_1 is zero.

$$\therefore \quad \omega_H = GB = 2\pi \text{ Mrads/sec (1MHz)}$$

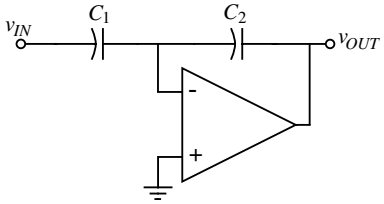
For the inverting amplifier with an ideal gain of -1, the value of R_2/R_1 is one.

$$\therefore \quad \omega_H = \frac{GB \cdot 1}{1+1} = \frac{GB}{2} = \pi \text{ Mrads/sec (500kHz)}$$

CHARGE AMPLIFIERS



Noninverting Charge Amplifier



Inverting Charge Amplifier

Gain and GB = ∞:

$$\frac{V_{out}}{V_{in}} = \frac{C_1+C_2}{C_2} \qquad \frac{V_{out}}{V_{in}} = -\frac{C_1}{C_2}$$

Gain ≠ ∞, GB = ∞:

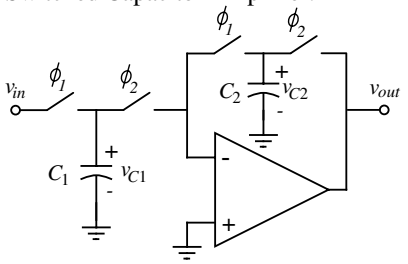
$$\frac{V_{out}}{V_{in}} = \left(\frac{C_1+C_2}{C_2}\right)\frac{\frac{A_{vd}(0)C_2}{C_1+C_2}}{1+\frac{A_{vd}(0)C_2}{C_1+C_2}} \qquad \frac{V_{out}}{V_{in}} = \left(-\frac{C_1}{C_2}\right)\frac{\frac{A_{vd}(0)C_2}{C_1+C_2}}{1+\frac{A_{vd}(0)C_2}{C_1+C_2}}$$

Gain ≠ ∞, GB ≠ ∞:

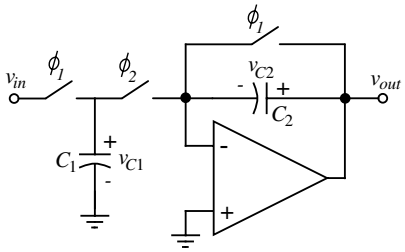
$$\frac{V_{out}}{V_{in}} = \left(\frac{C_1+C_2}{C_2}\right)\frac{\frac{GB\cdot C_2}{C_1+C_2}}{s+\frac{GB\cdot C_2}{C_1+C_2}} \qquad \frac{V_{out}}{V_{in}} = \left(-\frac{C_1}{C_2}\right)\frac{\frac{GB\cdot C_2}{C_1+C_2}}{s+\frac{GB\cdot C_2}{C_1+C_2}}$$

SWITCHED CAPACITOR AMPLIFIERS

Parallel Switched Capacitor Amplifier:



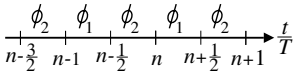
Inverting Switched Capacitor Amplifier



Modification to prevent open-loop operation

Analysis:

Find the *even-odd* and the *even-even* z-domain transfer function for the above switched capacitor inverting amplifier.



Clock phasing for this example.

$\underline{\phi_1}$: $(n-1)T < t < (n-0.5)T$

$$v_{C1}^{o}(n-1)T = v_{in}^{o}(n-1)T$$

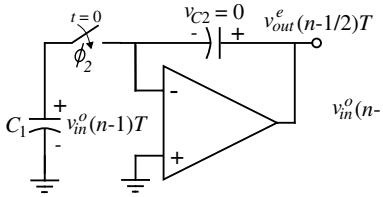
and

$$v_{C2}^{o}(n-1)T = 0$$

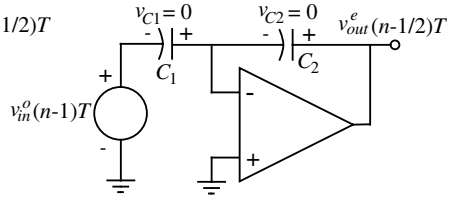
SWITCHED CAPACITOR AMPLIFIERS - Continued

$\underline{\phi_2: (n-0.5)T < t < nT}$

Equivalent circuit:



Equivalent circuit at the moment ϕ_2 closes.



Simplified equivalent circuit.

From the simplified equivalent circuit we write,

$$v_{out}^e(n\text{-}1/2)T = -\left(\frac{C_1}{C_2}\right) v_{in}^o(n\text{-}1)T$$

Converting to the z-domain gives,

$$z^{-1/2}\, V_{out}^e(z) = -\left(\frac{C_1}{C_2}\right) z^{-1}\, V_{in}^o(z)$$

Multiplying by $z^{-1/2}$ gives,

$$V_{out}^e(z) = -\left(\frac{C_1}{C_2}\right) z^{-1/2}\, V_{in}^o(z)$$

Solving for the even-odd transfer function, $H^{oe}(z)$, gives,

$$\boxed{H^{oe}(z) = \frac{V_{out}^e(z)}{V_{in}^o(z)} = -\left(\frac{C_1}{C_2}\right) z^{-1/2}}$$

SWITCHED CAPACITOR AMPLIFIERS - Continued

Solving for the even-even transfer function, $H^{ee}(z)$.

Assume that the applied input signal, $v_{in}^o(n\text{-}1)T$, was uncharged during the previous ϕ_2 phase period(from $t = (n\text{-}3/2)T$ to $t = (n\text{-}1)T$), then

$$v_{in}^o(n\text{-}1)T = v_{in}^e(n\text{-}3/2)T$$

which gives

$$V_{in}^o(z) = z^{-1/2}\, V_{in}^e(z)\ .$$

Substituting this relationship into $H^{oe}(z)$ gives

$$V_{out}^e(z) = -\left(\frac{C_1}{C_2}\right) z^{-1}\, V_{in}^e(z)$$

or

$$\boxed{H^{ee}(z) = \frac{V_{out}^e(z)}{V_{in}^e(z)} = -\left(\frac{C_1}{C_2}\right) z^{-1}}$$

FREQUENCY RESPONSE OF SWITCHED CAPACITOR AMPLIFIERS

Replace z by $e^{j\omega T}$.

$$H^{oe}(e^{j\omega T}) = \frac{V^{e}_{out}(e^{j\omega T})}{V^{o}_{in}(e^{j\omega T})} = -\left(\frac{C_1}{C_2}\right) e^{-j\omega T/2}$$

and

$$H^{ee}(e^{j\omega T}) = \frac{V^{e}_{out}(e^{j\omega T})}{V^{e}_{in}(e^{j\omega T})} = -\left(\frac{C_1}{C_2}\right) e^{-j\omega T}$$

If C_1/C_2 is equal to R_2/R_1, then the magnitude response is identical to inverting unity gain amplifier.

However, the phase shift of $H^{oe}(e^{j\omega T})$ is

$$\text{Arg}[H^{oe}(e^{j\omega T})] = \pm 180° - \omega T/2$$

and the phase shift of $H^{oe}(e^{j\omega T})$ is

$$\text{Arg}[H^{ee}(e^{j\omega T})] = \pm 180° - \omega T.$$

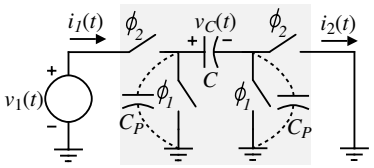
Comments:

- The phase shift of the switched capacitor inverting amplifier has an excess linear phase delay.
- When the frequency is equal to $0.5f_c$, this delay is 90°.
- One must be careful when using switched capacitor circuits in a feedback loop because of the excess phase delay.

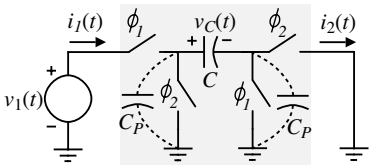
POSITIVE AND NEGATIVE TRANSRESISTANCE EQUIVALENT CIRCUITS

Transresistance circuits are two-port networks where the voltage across one port controls the current flowing between the ports. Typically, one of the ports is at zero potential (virtual ground).

Circuits:



Positive Transresistance Realization.



Negative Transresistance Realization.

Analysis (Negative transresistance realization):

$$R_T = \frac{v_1(t)}{i_2(t)} = \frac{v_1}{i_2(average)}$$

If we assume $v_1(t)$ is approximately constant over one period of the clock, then we can write

$$i_2(average) = \frac{1}{T}\int_{T/2}^{T} i_2(t)dt = \frac{q_2(T) - q_2(T/2)}{T} = \frac{Cv_C(T) - Cv_C(T/2)}{T} = \frac{-Cv_1}{T}$$

Substituting this expression into the one above shows that

$$\boxed{R_T = -T/C}$$

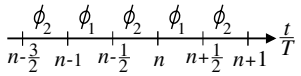
Similarly, it can be shown that the positive transresistance is T/C.

Comments:

- These results are only valid when $f_c >> f$.
- These circuits are insensitive to the parasitic capacitances shown as dotted capacitors.

NONINVERTING STRAY INSENSITIVE SWITCHED CAPACITOR AMPLIFIER

Analysis:



Clock phasing for this example.

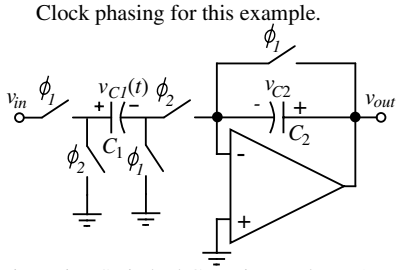
$\underline{\phi_1: (n-1)T < t < (n-0.5)T}$

The voltages across each capacitor can be written as

$$v_{C1}^o(n-1)T = v_{in}^o(n-1)T$$

and

$$v_{C2}^o(n-1)T = v_{out}^o(n-1)T = 0 .$$



Noninverting Switched Capacitor Voltage Amplifier.

$\underline{\phi_2: (n-0.5)T < t < nT}$

The voltage across C_2 is

$$v_{out}^e(n-1/2)T = \left(\frac{C_1}{C_2}\right) v_{in}^o(n-1)T$$

$$V_{out}^e(z) = \left(\frac{C_1}{C_2}\right) z^{-1/2}\, V_{in}^o(z) \quad \rightarrow \quad \boxed{H^{oe}(z) = \left(\frac{C_1}{C_2}\right) z^{-1/2}}$$

If the applied input signal, $v_{in}^o(n-1)T$, was unchanged during the previous ϕ_2 phase period above becomes

$$V_{out}^e(z) = \left(\frac{C_1}{C_2}\right) z^{-1}\, V_{in}^e(z) \quad \rightarrow \quad \boxed{H^{ee}(z) = \left(\frac{C_1}{C_2}\right) z^{-1}}$$

Comments:

- Excess phase of $H^{oe}(e^{j\omega T})$ is $-\omega T/2$ and for $H^{ee}(e^{j\omega T})$ is $-\omega T$

INVERTING STRAY INSENSITIVE SWITCHED CAPACITOR AMPLIFIER

Analysis:

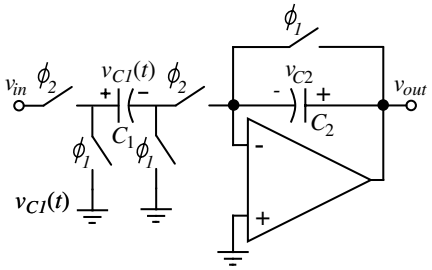
$\underline{\phi_1: (n-1)T < t < (n-0.5)T}$

The voltages across each capacitor can be written as

$$v_{C1}^o(n-1)T = 0$$

and

$$v_{C2}^o(n-1)T = v_{out}^o(n-1)T = 0 .$$



Inverting Switched Capacitor Voltage Amplifier.

$\underline{\phi_2: (n-0.5)T < t < nT}$

The voltage across C_2 is

$$v_{out}^e(n-1/2)T = -\left(\frac{C_1}{C_2}\right) v_{in}^e(n-1/2)T$$

$$V_{out}^e(z) = -\left(\frac{C_1}{C_2}\right) V_{in}^o(z) \quad \rightarrow \quad \boxed{H^{oe}(z) = -\left(\frac{C_1}{C_2}\right)}$$

Comments:

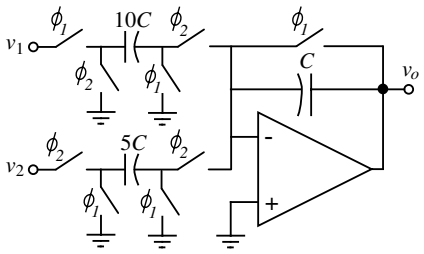
- The inverting switched capacitor amplifier has no excess phase delay.
- There is no transfer of charge during ϕ_1.

EXAMPLE 9.2-3 - DESIGN OF A SWITCHED CAPACITOR SUMMING AMPLIFIER

Design a switched capacitor summing amplifier using the circuits in stray insensitive transresistance circuits which gives the output voltage during the ϕ_2 phase period that is equal to $10v_1$ - $5v_2$, where v_1 and v_2 are held constant during a ϕ_2-ϕ_1 period and then resampled for the next period.

Solution

A possible solution is shown. Considering each of the inputs separately, we can write that



$$v_{o1}^{e}(n\text{-}1/2)T = 10v_1^{o}(n\text{-}1)T \quad (1)$$

and

$$v_{o2}^{e}(n\text{-}1/2)T = -5v_2^{e}(n\text{-}1/2)T\,. \qquad (2)$$

Because $v_1^{o}(n\text{-}1)T = v_1^{e}(n\text{-}3/2)T$, Eq. (1) can be rewritten as

$$v_{o1}^{e}(n\text{-}1/2)T = 10v_1^{e}(n\text{-}3/2)T\,. \qquad (3)$$

Combining Eqs. (2) and (3) gives

$$v_o^{e}(n\text{-}1/2)T = v_{o1}^{e}(n\text{-}1/2)T + v_{o2}^{e}(n\text{-}1/2)T = 10v_1^{e}(n\text{-}3/2)T - 5v_2^{e}(n\text{-}1/2)T\,. \qquad (4)$$

or

$$V_o^{e}(z) = 10z^{-1}V_1^{e}(z) - 5V_2^{e}(z)\,. \qquad (5)$$

Eqs. (4) and (5) verifies that proposed solution satisfies the specifications of the example.

NONIDEALITIES OF SWITCHED CAPACITOR CIRCUITS - CAPACITORS

See Chapter 2

NONIDEAL OP AMPS - FINITE GAIN

Finite Amplifier Gain

Consider the noninverting switched capacitor amplifier during ϕ_2:

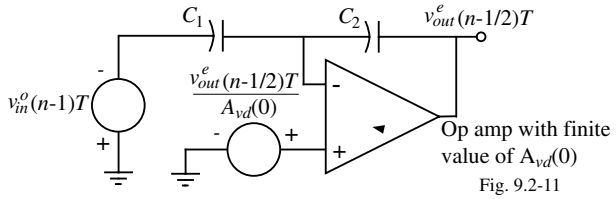


Fig. 9.2-11

The output during ϕ_2 can be written as,

$$v_{out}^e(n\text{-}1/2)T = \left(\frac{C_1}{C_2}\right) v_{in}^o(n\text{-}1)T + \left(\frac{C_1+C_2}{C_2}\right) \frac{v_{out}^e(n\text{-}1/2)T}{A_{vd}(0)}$$

Converting this to the z-domain and solving for the $H^{oe}(z)$ transfer function gives

$$H^{oe}(z) = \frac{V_{out}^e(z)}{V_{in}^o(z)} = \left(\frac{C_1}{C_2}\right) z^{-1/2} \left[\frac{1}{1 - \frac{C_1 + C_2}{A_{vd}(0)C_2}}\right].$$

Comments:

- The phase response is unaffected by the finite gain
- A gain of 1000 gives a magnitude of 0.998 rather than 1.0.

NONIDEAL OP AMPS - FINITE BANDWIDTH AND SLEW RATE

Finite *GB*:

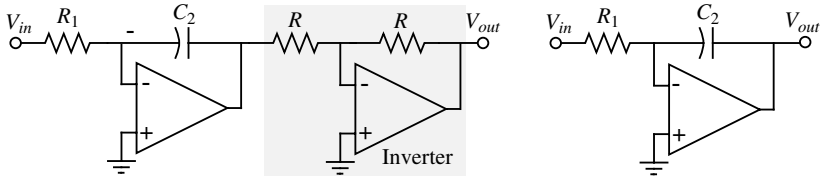
- In general the analysis is complicated. (We will provide more detail for integrators.)
- The clock period, *T*, should be equal to or less that 10/*GB*.
- The settling time of the op amp must be less that *T*/2.

Slew Rate:

- The slew rate of the op amp should be large enough so that the op amp can make a full swing within *T*/2.

9.3 - SWITCHED CAPACITOR INTEGRATORS

CONTINUOUS TIME INTEGRATORS



(a.) Noninverting and (b.) inverting continuous time integrators.

Ideal Performance:

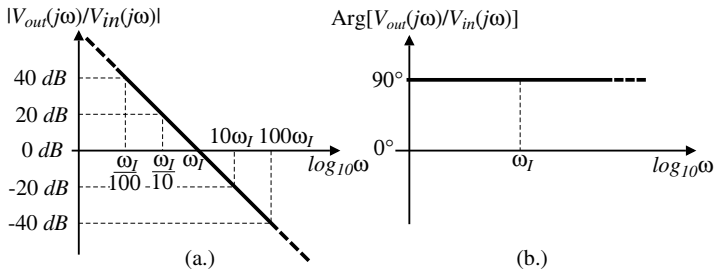
Noninverting-

$$\frac{V_{out}(j\omega)}{V_{in}(j\omega)} = \frac{1}{j\omega R_1 C_2} = \frac{\omega_I}{j\omega} = \frac{-j\omega_I}{\omega}$$

Inverting-

$$\frac{V_{out}(j\omega)}{V_{in}(j\omega)} = \frac{-1}{j\omega R_1 C_2} = \frac{-\omega_I}{j\omega} = \frac{j\omega_I}{\omega}$$

Frequency Response:



CONTINUOUS TIME INTEGRATORS - NONIDEAL PERFORMANCE

Finite Gain:

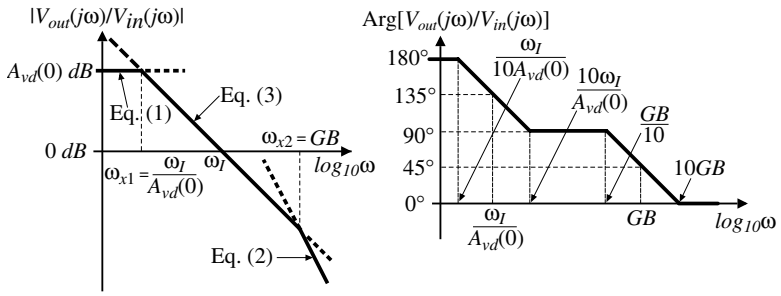
$$\frac{V_{out}}{V_{in}} = -\left(\frac{1}{sR_1C_2}\right)\frac{\frac{A_{vd}(s)\,sR_1C_2}{sR_1C_2+1}}{1+\frac{A_{vd}(s)\,sR_1C_2}{sR_1C_2+1}} = \left(-\frac{\omega_I}{s}\right)\frac{\frac{A_{vd}(s)\,(s/\omega_I)}{(s/\omega_I)+1}}{1+\frac{A_{vd}(s)\,(s/\omega_I)}{(s/\omega_I)+1}}$$

where $A_{vd}(s) = \frac{A_{vd}(0)\omega_a}{s+\omega_a} = \frac{GB}{s+\omega_a} \approx \frac{GB}{s}$

Case 1: $s \rightarrow 0 \Rightarrow A_{vd}(s) = A_{vd}(0) \Rightarrow \frac{V_{out}}{V_{in}} \approx -A_{vd}(0)$ (1)

Case 2: $s \rightarrow \infty \Rightarrow A_{vd}(s) = \frac{GB}{s} \Rightarrow \frac{V_{out}}{V_{in}} \approx -\left(\frac{GB}{s}\right)\left(\frac{\omega_I}{s}\right)$ (2)

Case 3: $0 < s < \infty \Rightarrow A_{vd}(s) = \infty \Rightarrow \frac{V_{out}}{V_{in}} \approx -\frac{\omega_I}{s}$ (3)



EXAMPLE 9.3-1 - Frequency Range over which the Continuous Time Integrator is Ideal

Find the range of frequencies over which the continuous time integrator approximates ideal behavior if $A_{vd}(0)$ and GB of the op amp are 1000 and 1MHz, respectively. Assume that ω_I is 2000π radians/sec.

Solution

The "idealness" of an integrator is determined by how close the phase shift is to ±90° (+90° for an inverting integrator and -90° for a noninverting integrator).

The actual phase shift in the asymptotic plot of the integrator is approximately 6° above 90° at the frequency $10\omega_I/A_{vd}(0)$ and approximately 6° below 90° at GB /10.

Assume for this example that a ±6° tolerance is satisfactory. The frequency range can be found by evaluating $10\omega_I/A_{vd}(0)$ and $GB/10$.

Therefore the range over which the integrator approximates ideal behavior is from 10Hz to 100kHz. This range will decrease as the phase tolerance is decreased.

NONINVERTING SWITCHED CAPACITOR INTEGRATOR

Analysis:

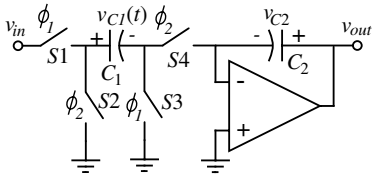
$\underline{\phi_1}$: $(n-1)T < t < (n-0.5)T$

The voltage across each capacitor is

$$v_{c1}^o(n\text{-}1)T = v_{in}^o(n\text{-}1)T$$

and

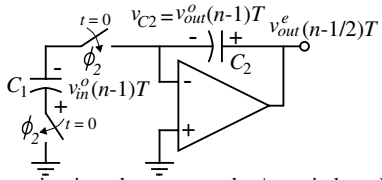
$$v_{c2}^o(n\text{-}1)T = v_{out}^o(n\text{-}1)T\,.$$



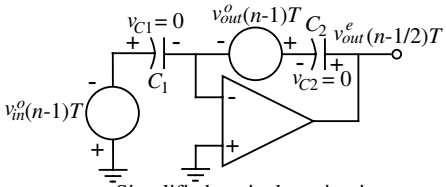
Noninverting, stray insensitive integrator.

$\underline{\phi_2}$: $(n-0.5)T < t < n\,T$

Equivalent circuit:



Equivalent circuit at the moment the $\phi 2$ switches close.



Simplified equivalent circuit.

We can write that, $v_{out}^e(n-1/2)T = \left(\frac{C_1}{C_2}\right) v_{in}^o(n-1)T + v_{out}^o(n-1)T$

NONINVERTING SWITCHED CAPACITOR INTEGRATOR - Continued

$\underline{\phi_1}$: $nT < t < (n + 0.5)T$

If we advance one more phase period, i.e. t = (n)T to t = (n-1/2)T, we see that the voltage at the output is unchanged. Thus, we may write

$$v_{out}^{o}(n)T = v_{out}^{e}(n\text{-}1/2)T\,.$$

Substituting this relationship into the previous gives the desired time relationship expressed as

$$v_{out}^{o}(n)T = \left(\frac{C_1}{C_2}\right) v_{in}^{o}(n\text{ -}1)T + v_{out}^{o}(n\text{ -}1)T\,.$$

Transferring this equation to the z-domain gives,

$$V_{out}^{o}(z) = \left(\frac{C_1}{C_2}\right) z^{-1} V_{in}^{o}(z) + z^{-1} V_{out}^{o}(z) \quad \rightarrow \quad H^{oo}(z) = \frac{V_{out}^{o}(z)}{V_{in}^{o}(z)} = \left(\frac{C_1}{C_2}\right) \frac{z^{-1}}{1\text{-}z^{-1}} = \left(\frac{C_1}{C_2}\right) \frac{1}{z\text{-}1}$$

Replacing z by $e^{j\omega T}$ gives,

$$H^{oo}(e^{j\omega T}) = \frac{V_{out}^{o}(e^{j\omega T})}{V_{in}^{o}(e^{j\omega T})} = \left(\frac{C_1}{C_2}\right) \frac{1}{e^{j\omega T}\text{ -}1} = \left(\frac{C_1}{C_2}\right) \frac{e^{-j\omega T/2}}{e^{j\omega T/2} - e^{-j\omega T/2}}$$

Replacing $e^{j\omega T/2} - e^{-j\omega T/2}$ by its equivalent trigonometric identity, the above becomes

$$H^{oo}(e^{j\omega T}) = \frac{V_{out}^{o}(e^{j\omega T})}{V_{in}^{o}(e^{j\omega T})} = \left(\frac{C_1}{C_2}\right) \frac{e^{-j\omega T/2}}{j2\,sin(\omega T/2)} \left(\frac{\omega T}{\omega T}\right) = \left(\frac{C_1}{j\omega T C_2}\right) \left(\frac{\omega T/2}{sin(\omega T/2)}\right) (e^{-j\omega T/2})$$

$H^{oo}(e^{j\omega T})$ = (Ideal)x(Magnitude error)x(Phase error) where $\omega_I = \frac{C_1}{TC_2} \Rightarrow$ Ideal $= \frac{\omega_I}{j\omega}$

EXAMPLE 9.3-2 - Comparison of a Continuous Time and Switched Capacitor Integrator

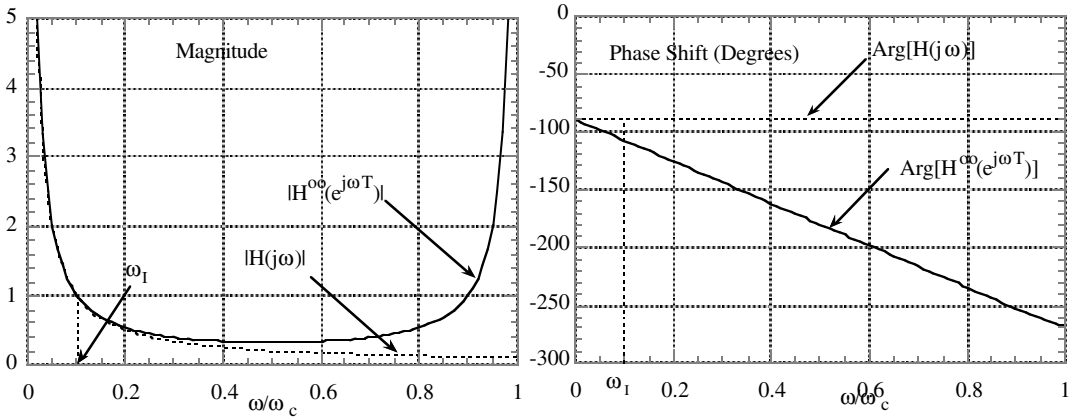
Assume that ω_I is equal to $0.1\omega_c$ and plot the magnitude and phase response of the noninverting continuous time and switched capacitor integrator from 0 to ω_I.

Solution

Letting ω_I be $0.1\omega_c$ gives

$$H(j\omega) = \frac{1}{10j\omega/\omega_c} \quad \text{and} \quad H^{oo}(e^{j\omega T}) = \left(\frac{1}{10j\omega/\omega_c}\right) \left(\frac{\pi\omega/\omega_c}{sin(\pi\omega/\omega_c)}\right) (e^{-j\pi\omega/\omega_c})$$

Plots:



INVERTING SWITCHED CAPACITOR INTEGRATOR

Analysis:

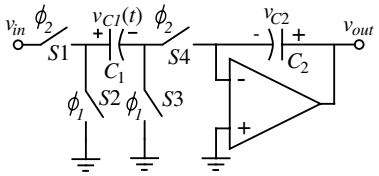
$\underline{\phi_1: (n-1)T < t < (n-0.5)T}$

The voltage across each capacitor is

$$v_{c1}^{o}(n-1)T = 0$$

and

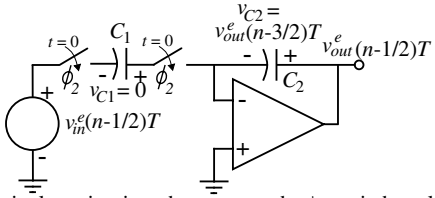
$$v_{c2}^{o}(n-1)T = v_{out}^{o}(n-1)T = v_{out}^{e}(n-\frac{3}{2})T.$$



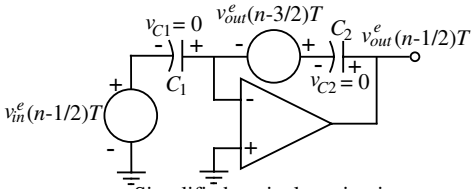
Inverting, stray insensitive integrator.

$\underline{\phi_2: (n-0.5)T < t < n\,T}$

Equivalent circuit:



Equivalent circuit at the moment the ϕ_2 switches close.



Simplified equivalent circuit.

Now we can write that,

$$v_{out}^{e}(n-1/2)T = v_{out}^{e}(n-3/2)T - \left(\frac{C_1}{C_2}\right) v_{in}^{e}(n-1/2)T. \quad (22)$$

INVERTING SWITCHED CAPACITOR INTEGRATOR - Continued

Expressing the previous equation in terms of the z-domain equivalent gives,

$$V_{out}^{e}(z) = z^{-1}V_{out}^{e}(z) - \left(\frac{C_1}{C_2}\right)V_{in}^{e}(z) \quad \rightarrow \quad H^{ee}(z) = \frac{V_{out}^{e}(z)}{V_{in}^{e}(z)} = -\left(\frac{C_1}{C_2}\right)\frac{1}{1-z^{-1}} = -\left(\frac{C_1}{C_2}\right)\frac{z}{z-1}$$

To get the frequency response, we replace z by $e^{j\omega T}$ giving,

$$H^{ee}(e^{j\omega T}) = \frac{V_{out}^{e}(e^{j\omega T})}{V_{in}^{e}(e^{j\omega T})} = -\left(\frac{C_1}{C_2}\right)\frac{e^{j\omega T}}{e^{j\omega T}-1} = -\left(\frac{C_1}{C_2}\right)\frac{e^{j\omega T/2}}{e^{j\omega T/2}-e^{-j\omega T/2}}$$

Replacing $e^{j\omega T/2} - e^{-j\omega T/2}$ by $2j\,sin(\omega T/2)$ and simplifying gives,

$$H^{ee}(e^{j\omega T}) = \frac{V_{out}^{e}(e^{j\omega T})}{V_{in}^{e}(e^{j\omega T})} = -\left(\frac{C_1}{j\omega T C_2}\right)\left(\frac{\omega T/2}{sin(\omega T/2)}\right)(e^{j\omega T/2})$$

Same as noninverting integrator except for phase error.

Consequently, the magnitude response is identical but the phase response is given as

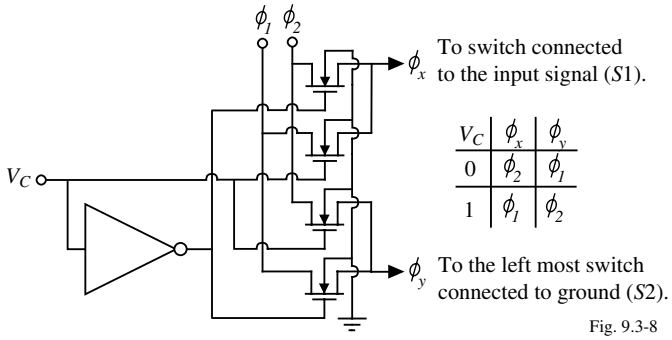
$$\text{Arg}[H^{ee}(e^{j\omega T})] = \frac{\pi}{2} + \frac{\omega T}{2}.$$

Comments:

- Note that the phase error is positive for the inverting integrator and negative for the noninverting integrator.
- The cascade of an inverting and noninverting switched capacitor integrator has no phase error.

A SIGN MULTIPLEXER

A circuit that changes the ϕ_1 and ϕ_2 of the leftmost switches of the stray insensitive, switched capacitor integrator.



V_C	ϕ_x	ϕ_y
0	ϕ_2	ϕ_1
1	ϕ_1	ϕ_2

Fig. 9.3-8

This circuit steers the ϕ_1 and ϕ_2 clocks to the input switch ($S1$) and the leftmost switch connected to ground ($S2$) as a function of whether V_c is high or low.

SWITCHED CAPACITOR INTEGRATORS - FINITE OP AMP GAIN

Consider the following circuit which is equivalent of the noninverting integrator at the beginning of the ϕ_2 phase period.

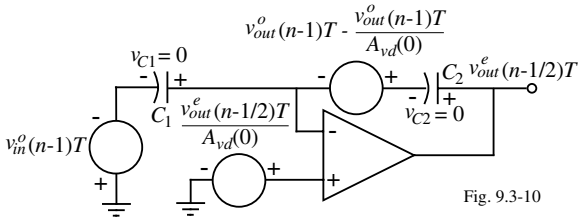


Fig. 9.3-10

The expression for $v^e_{out}(n\text{-}1/2)T$ can be written as

$$v^e_{out}(n\text{-}1/2)T = \left(\frac{C_1}{C_2}\right) v^o_{in}(n\text{-}1)T + v^o_{out}(n\text{-}1)T - \frac{v^o_{out}(n\text{-}1)T}{A_{vd}(0)} + \frac{v^e_{out}(n\text{-}1/2)T}{A_{vd}(0)}\left(\frac{C_1+C_2}{C_2}\right)$$

Substituting $v^o_{out}(n)T = v^e_{out}(n\text{-}0.5)T$ into this equation gives

$$v^o_{out}(n)T = \left(\frac{C_1}{C_2}\right) v^o_{in}(n\text{-}1)T + v^o_{out}(n\text{-}1)T - \frac{v^o_{out}(n\text{-}1)T}{A_{vd}(0)} + \frac{v^o_{out}(n)T}{A_{vd}(0)}\left(\frac{C_1+C_2}{C_2}\right)$$

Using the previous procedures to solve for the z-domain transfer function results in,

$$H^{oo}(z) = \frac{V^o_{out}(z)}{V^o_{in}(z)} = \frac{\frac{C_1}{C_2} z^{-1}}{1 - z^{-1} + \frac{z^{-1}}{A_{vd}(0)} - \frac{C_1}{A_{vd}(0)C_2}\frac{z^{-1}}{z^{-1}} + \frac{1}{A_{vd}(0)}\frac{z^{-1}}{z^{-1}}}$$

or

$$H^{oo}(z) = \frac{V^o_{out}(z)}{V^o_{in}(z)} = \left(\frac{(C_1/C_2)\, z^{-1}}{1 - z^{-1}}\right)\left(\frac{1}{1 - \frac{1}{A_{vd}(0)} - \frac{C_1}{A_{vd}(0)C_2(1\text{-}z^{-1})}}\right) = \frac{H_I(z)}{1 - \frac{1}{A_{vd}(0)} - \frac{C_1}{A_{vd}(0)C_2(1\text{-}z^{-1})}}$$

FINITE OP AMP GAIN - Continued

Substitute the z-domain variable, z, with e^{jwT} to get

$$H^{oo}(e^{j\omega T}) = \frac{H_I(e^{j\omega T})}{1 - \frac{1}{A_{vd}(0)}\left[1 + \frac{C_1}{2C_2}\right] - j\frac{C_1/C_2}{2A_{vd}(0)\ tan\left(\frac{\omega T}{2}\right)}} \quad (1)$$

where now $H_I(e^{j\omega T})$ is the integrator transfer function for $A_{vd}(0) = \infty$.

The error of an integrator can be expressed as

$$H(j\omega) = \frac{H_I(j\omega)}{[1-m(\omega)]\ e^{-j\theta(\omega)}}$$

where

$m(\omega)$ = the magnitude error due to $A_{vd}(0)$

$\theta(\omega)$ = the phase error due to $A_{vd}(0)$

If $\theta(\omega)$ is much less than unity, then this expression can be approximated by

$$H(j\omega) \approx \frac{H_I(j\omega)}{1 - m(\omega) - j\theta(\omega)} \quad (2)$$

Comparing Eq. (1) with Eq. (2) gives the magnitude and phase error due to a finite value of $A_{vd}(0)$ as

$$m(j\omega) = -\frac{1}{A_{vd}(0)}\left[1 + \frac{C_1}{2C_2}\right] \quad \text{and} \quad \theta(j\omega) = \frac{C_1/C_2}{2A_{vd}(0)\ tan\left(\frac{\omega T}{2}\right)}$$

EXAMPLE 9.3-3 - Evaluation of the Integrator Errors due to a finite value of $A_{vd}(0)$

Assume that the clock frequency and integrator frequency of a switch capacitor integrator is 100kHz and 10kHz, respectively. If the value of $A_{vd}(0)$ is 100, find the value of $m(j\omega)$ and $\theta(j\omega)$ at 10kHz.

Solution

The ratio of C_1 to C_2 is found as

$$\frac{C_1}{C_2} = \omega_I T = \frac{2\pi \cdot 10{,}000}{100{,}000} = 0.6283\ .$$

Substituting this value along with that for $A_{vd}(0)$ into $m(j\omega)$ and $\theta(j\omega)$ gives

$$m(j\omega) = -\left[1 + \frac{0.6283}{2}\right] = -0.0131$$

and

$$\theta(j\omega) = \frac{0.6283}{2 \cdot 100 \cdot \tan(18°)} = 0.554°\ .$$

The "ideal" switched capacitor transfer function, $H_I(j\omega)$, will be multiplied by a value of approximately 1/1.0131 = 0.987 and will have an additional phase lag of approximately 0.554°.

In general, the phase shift error is more serious than the magnitude error.

SWITCHED CAPACITOR INTEGRATORS - FINITE OP AMP *GB*

The precise analysis of the influence of *GB* can be found elsewhere[†] . The results of such an analysis can be summarized in the following table.

Noninverting Integrator	Inverting Integrator
$m(\omega) \approx -e^{-k_1}\left(\frac{C_2}{C_1+C_2}\right)$ $\theta(\omega) \approx 0$	$m(\omega) \approx -e^{-k_1}\left[1 - \left(\frac{C_2}{C_1+C_2}\right)cos(\omega T)\right]$ $\theta(\omega) \approx -e^{-k_1}\left(\frac{C_2}{C_1+C_2}\right)cos(\omega T)$
$k_1 \approx \pi\left(\frac{C_2}{C_1+C_2}\right)\left(\frac{GB}{f_c}\right)$	

If ωT is much less than unity, the expressions in table reduce to

$$m(\omega) \approx -2\pi\left(\frac{f}{f_c}\right)e^{-\pi(GB/f_c)}$$

[†] K. Martin and A.S. Sedra, "Effects of the Op Amp Finite Gain and Bandwidth on the Performance of Switched-Capacitor Filters," *IEEE Trans. on Circuits and Systems*, vol. CAS-28, no. 8, August 1981, pp. 822-829.

SWITCHED CAPACITOR CIRCUITS - *kT/C* NOISE

Switched capacitors generate an inherent thermal noise given by *kT/C*. This noise is verified as follows. An equivalent circuit for a switched capacitor:

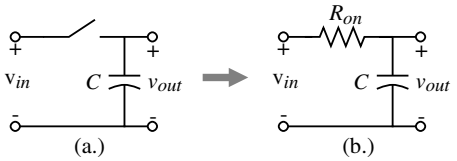


Figure 9.3-11 - (a.) Simple switched capacitor circuit. (b.) Approximation of (a.).

The noise voltage spectral density of Fig. 9.3-11b is given as

$$\overline{e_{R_{on}}^2} = 4kTR_{on}\ \text{Volts}^2/\text{Hz} = \frac{2kTR_{on}}{\pi}\ \text{Volt}^2/\text{Rad./sec.} \tag{1}$$

The rms noise voltage is found by integrating this spectral density from 0 to ∞ to give

$$v_{R_{on}}^2 = \frac{2kTR_{on}}{\pi}\int_0^\infty \frac{\omega_1^2 d\omega}{\omega_1^2+\omega^2} = \frac{2kTR_{on}}{\pi}\left(\frac{\pi\omega_1}{2}\right) = \frac{kT}{C}\ \text{Volts(rms)}^2 \tag{2}$$

where $\omega_1 = 1/(R_{on}C)$. Note that the switch has an effective noise bandwidth of

$$f_{sw} = \frac{1}{4R_{on}C}\ \text{Hz} \tag{3}$$

which is found by dividing Eq. (2) by Eq. (1).

9.4 Z-DOMAIN MODELS OF TWO-PHASE, SWITCHED CAPACITOR CIRCUITS

Objective:

- Allow easy analysis of complex switched capacitor circuits
- Develop methods suitable for simulation by computer
- Will constrain our focus to two-phase, nonoverlapping clocks

General Two-Port Characterization of Switched Capacitor Circuits:

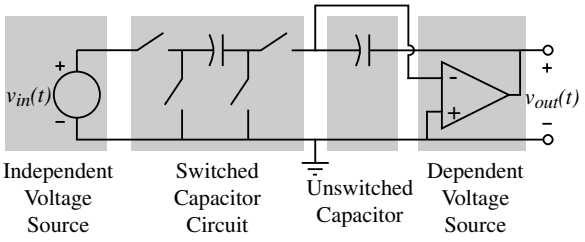
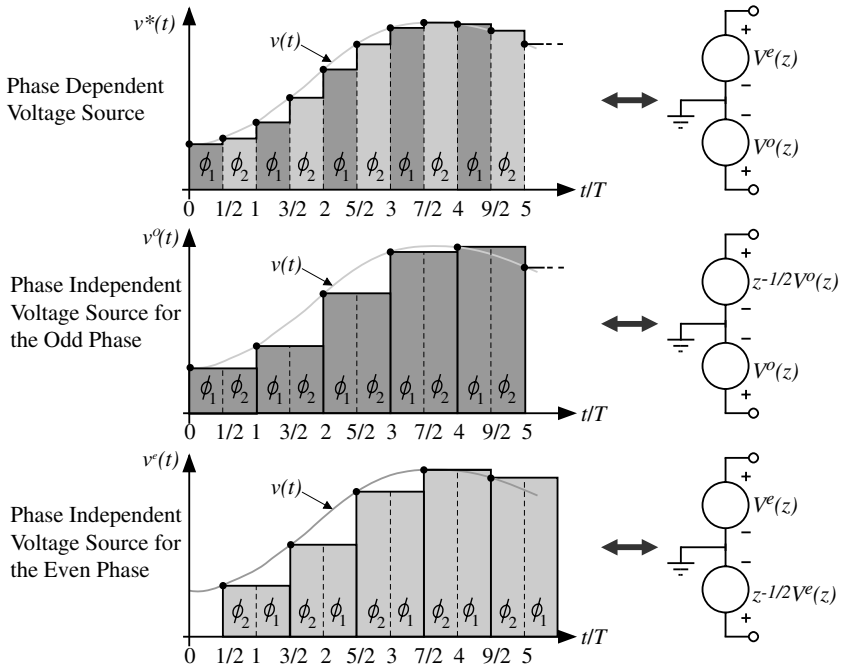


Figure 9.4-1 - Two-port characterization of a general switched capacitor circuit.

Approach:

- Four port - allows both phases to be examined
- Two-port - simplifies the models but not as general

INDEPENDENT VOLTAGE SOURCES



SWITCHED CAPACITOR FOUR-PORT CIRCUITS AND Z-DOMAIN MODELS†

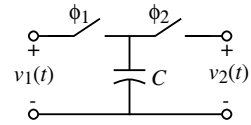
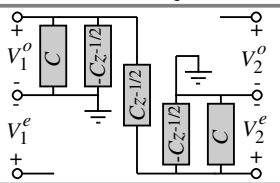
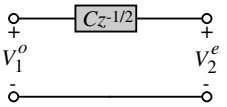
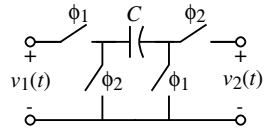
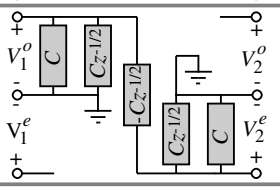
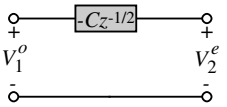
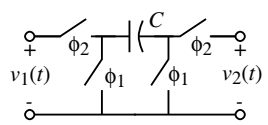
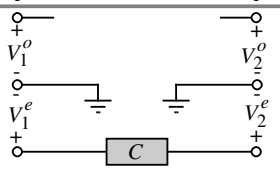
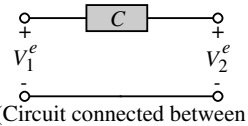
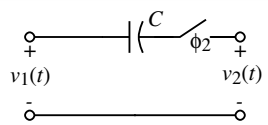
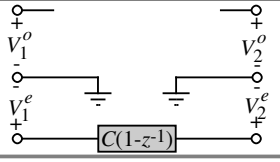
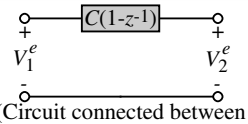
Switched Capacitor, Two-Port Circuit	Four-Port, z-domain Equivalent Model	Simplified, Two-Port z-domain Model
 Parallel Switched Capacitor		 (Circuit connected between defined voltages)
 Negative SC Transresistance		 (Circuit connected between defined voltages)
 Positive SC Transresistance		 (Circuit connected between defined voltages)
 Capacitor and Series Switch		 (Circuit connected between defined voltages)

Fig. 9.4-3

† K.R. Laker, "Equivalent Circuits for Analysis and Synthesis of Switched Capacitor Networks," *Bell System Technical Journal*, vol. 58, no. 3, March 1979, pp. 729-769.

Z-DOMAIN MODELS FOR CIRCUITS THAT MUST BE FOUR-PORT

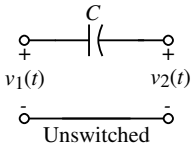
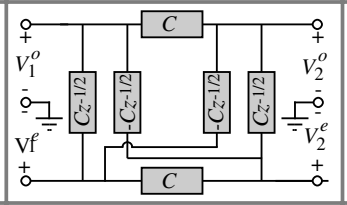
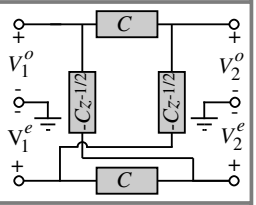
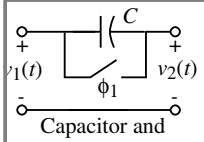
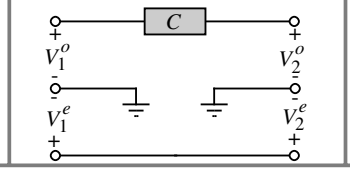
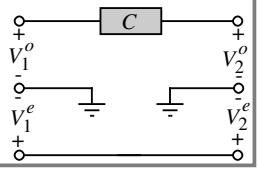
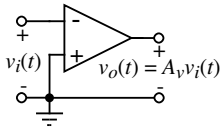
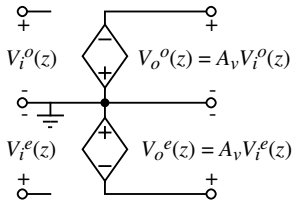
Switched Capacitor Circuit	Four-port z-domain Model	Simplified Four-port z-domain Model
 Unswitched Capacitor		
 Capacitor and Shunt Switch		

Fig. 9.4-4

Z-DOMAIN MODEL FOR THE IDEAL OP AMP



Time domain op amp model.



z-domain op amp model

Figure 9.4-5

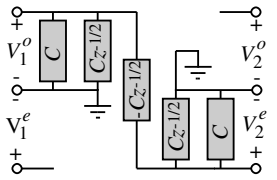
EXAMPLE 9.4-1- Illustration of the Validity of the z-domain Models

Show that the z-domain four-port model for the negative switched capacitor transresistance circuit of Fig. 9.4-3 is equivalent to the two-port switched capacitor circuit.

Solution

For the two-port switched capacitor circuit, we observe that during the ϕ_1 phase, the capacitor C is charged to $v_1(t)$. Let us assume that the time reference for this phase is t - T/2 so that the capacitor voltage is

$$v_C = v_1(t - T/2).$$



Negative SC Transresistance Model

During the next phase, ϕ_2, the capacitor is inverted and v_2 can be expressed as

$$v_2(t) = -v_C = -v_1(t - T/2).$$

Next, let us sum the currents flowing away from the positive V_2^e node of the four-port z-domain model in Fig. 9.4-3. This equation is,

$$-Cz^{-1/2}(V_2^e - V_1^o) + Cz^{-1/2}V_2^e + CV_2^e = 0.$$

This equation can be simplified as

$$V_2^e = -z^{-1/2}V_1^o$$

which when translated to the time domain gives

$$v_2(t) = -v_C = -v_1(t - T/2).$$

Thus, we have shown that the four-port z-domain model is equivalent to the time domain circuit for the above consideration.

Z-DOMAIN, HAND-ANALYSIS OF SWITCHED CAPACITOR CIRCUITS

General, time-variant, switched capacitor circuit.

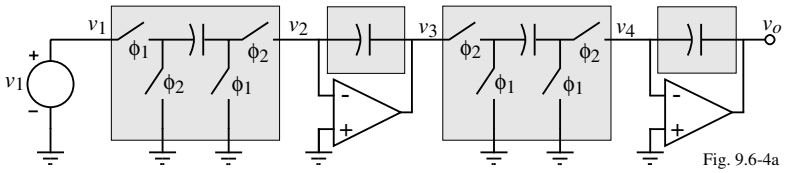


Fig. 9.6-4a

Four-port, model of the above circuit.

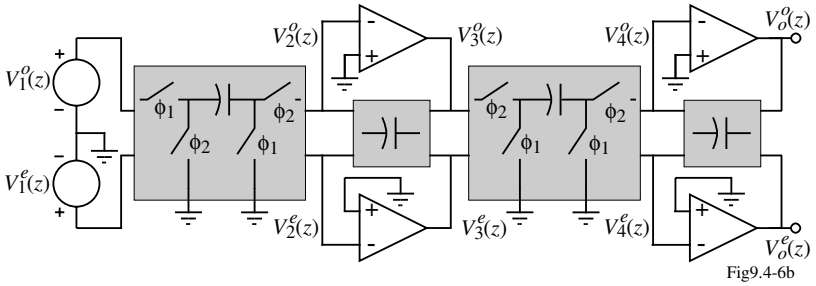


Fig9.4-6b

Simplification of the above circuit to a two-port, time-invariant model.

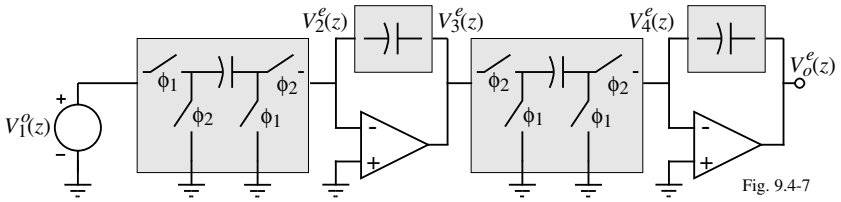


Fig. 9.4-7

EXAMPLE 9.4-2 - z-domain Analysis of the Noninverting Switched Capacitor Integrator

Find the z-domain transfer function $V_o^e(z)/V_i^o(z)$ and $V_o^o(z)/V_i^o(z)$ of the noninverting switched capacitor integrator using the above methods.

Solution

First redraw Fig. 9.3-4a as shown in Fig. 9.4-8a. We have added an additional ϕ_2 switch to help in using Fig. 9.4-3. Because this circuit is time-invariant, we may use the two-port modeling approach of Fig. 9.4-7. Note that C_2 and the indicated ϕ_2 switch are modeled by the bottom row, right column of Fig 9.4-3. The resulting z-domain model for Fig. 9.4-8a is shown in Fig. 9.4-8b.

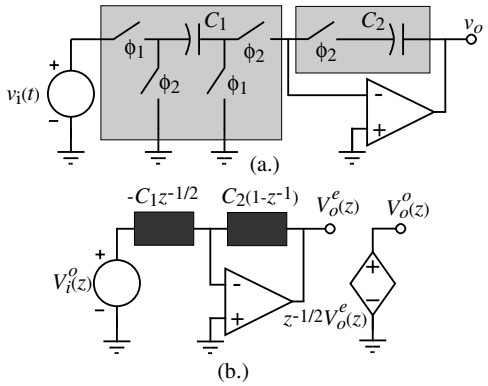


Figure 9.4-8 - (a.) Modified equivalent circuit of Fig. 9.3-4a. (b.) Two-port, z-domain model for Fig. 9.4-8a.

Recalling that the z-domain models are of admittance form, it is easy to write

$$-C_1z^{-1/2}V_i^o(z) + C_2(1-z^{-1})V_o^e(z) = 0 \rightarrow$$

$$H^{oe}(z) = \frac{V_o^e(z)}{V_i^o(z)} = \frac{C_1z^{-1/2}}{C_2(1-z^{-1})} .$$

$H^{oo}(z)$ is found by using the relationship that $V_o^o(z) = z^{-1/2}V_o^e(z)$ to get

$$H^{oo}(z) = \frac{V_o^o(z)}{V_i^o(z)} = \frac{C_1z^{-1}}{C_2(1-z^{-1})}$$

which is equal to z-domain transfer function of the noninverting switched capacitor integrator.

EXAMPLE 9.4-3 - z-domain Analysis of the Inverting Switched Capacitor Integrator

Find the z-domain transfer function $V_o^e(z)/V_i^e(z)$ and $V_o^o(z)/V_i^e(z)$ of Fig. 9.3-4a using the above methods.

Solution

Fig. 9.4-9a shows the modified equivalent circuit of Fig. 9.3-4b. The two-port, z-domain model for Fig. 9.4-9a is shown in Fig. 9.4-9b. Summing the currents flowing to the inverting node of the op amp gives

$$C_1 V_i^e(z) + C_2(1\text{-}z^{-1})V_o^e(z) = 0$$

which can be rearranged to give

$$H^{ee}(z) = \frac{V_o^e(z)}{V_i^e(z)} = \frac{-C_1}{C_2(1\text{-}z^{-1})} .$$

which is equal to inverting, switched capacitor integrator z-domain transfer function.

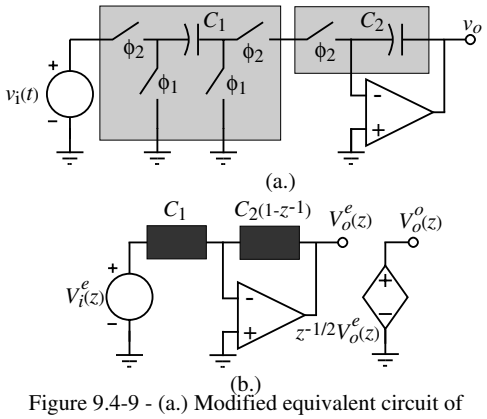


Figure 9.4-9 - (a.) Modified equivalent circuit of inverting SC integrator. (b.) Two-port, z-domain model for Fig. 9.4-9a

$H^{eo}(z)$ is found by using the relationship that $V_o^o(z) = z^{-1/2}V_o^e(z)$ to get

$$H^{eo}(z) = \frac{V_o^o(z)}{V_i^e(z)} = \frac{C_1 z^{-1/2}}{C_2(1\text{-}z^{-1})} .$$

EXAMPLE 9.4-4 - z-domain Analysis a Time-Variant Switched Capacitor Circuit

Find $V_o^o(z)$ and $V_o^e(z)$ as function of $V_1^o(z)$ and $V_2^o(z)$ for the summing, switched capacitor integrator of Fig. 9.4-10a.

Solution

This circuit is time-variant because C_3 is charged from a different circuit for each phase. Therefore, we must use a four-port model. The resulting z-domain model for Fig. 9.4-10a is shown in Fig. 9.4-10b.

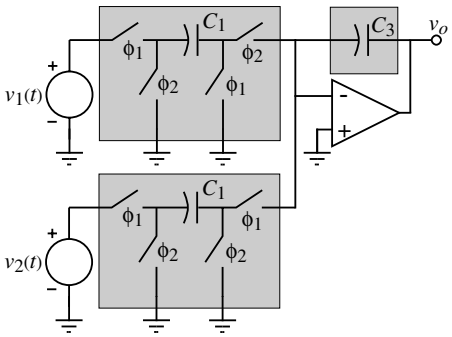


Fig. 9.4-10a - Summing Integrator.

EXAMPLE 9.4-4 - Continued

Summing the currents flowing away from the $V_i^o(z)$ node gives

$$C_2V_2^o(z) + C_3V_o^o(z) - C_3z^{-1/2}V_o^e(z) = 0 \qquad (1)$$

Summing the currents flowing away from the $V_i^e(z)$ nodes gives

$$-C_1z^{-1/2}V_1^o(z) - C_3z^{-1/2}V_o^o(z) + C_3V_o^e(z) = 0 \qquad (2)$$

Multiplying (2) by $z^{-1/2}$ and adding it to (1) gives

$$C_2V_2^o(z) + C_3V_o^o(z) - C_1z^{-1}V_1^o(z) - C_3z^{-1}V_o^o(z) = 0 \qquad (3)$$

Solving for $V_o^o(z)$ gives,

$$V_o^o(z) = \frac{C_1z^{-1}V_1^o(z)}{C_3(1-z^{-1})} - \frac{C_2V_2^o(z)}{C_3(1-z^{-1})}$$

Multiplying Eq. (1) by $z^{-1/2}$ and adding it to Eq. (2) gives

$$C_2z^{-1/2}V_2^o(z) - C_1z^{-1}V_1^o(z) - C_3z^{-1}V_o^e(z) + C_3V_o^e(z) = 0$$

Solving for $V_o^e(z)$ gives,

$$V_o^e(z) = \frac{C_1z^{-1/2}V_1^o(z)}{C_3(1-z^{-1})} - \frac{C_2z^{-1/2}V_2^o(z)}{C_3(1-z^{-1})} \ .$$

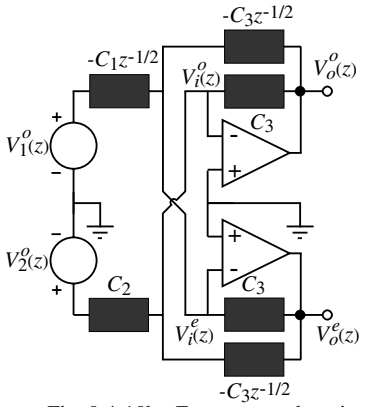


Fig. 9.4-10b - Four-port, z-domain model for Fig. 9.4-10a.

FREQUENCY DOMAIN SIMULATION OF SWITCHED CAPACITOR CIRCUITS USING SPICE

Storistors[†]

A storistor is a two-terminal element that has a current flow that occurs at some time after the voltage is applied across the storistor.

z-domain:

$$I(z) = \pm Cz^{-1/2}\,[V_1(z) - V_2(z)]$$

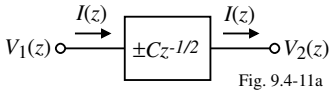


Fig. 9.4-11a

Time-domain:

$$i(t) = \pm C\left[v_1\left(t - \frac{T}{2}\right) - v_2\left(t - \frac{T}{2}\right)\right]$$

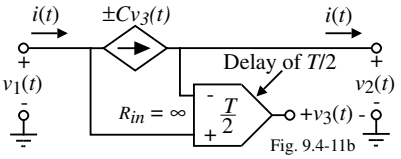


Fig. 9.4-11b

SPICE Primitives:

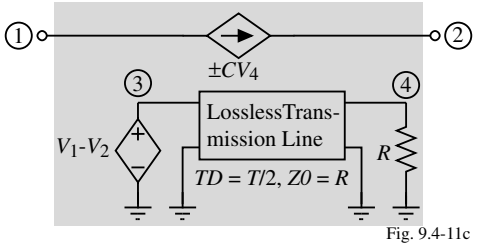


Fig. 9.4-11c

[†] B.D. Nelin, "Analysis of Switched-Capacitor Networks Using General-Purpose Circuit Simulation Programs," *IEEE Trans. on Circuits and Systems*, pp. 43-48, vol. CAS-30, No. 1, Jan. 1983.

EXAMPLE 9.4-5 - SPICE Simulation of Example 9.4-2

Use SPICE to obtain a frequency domain simulation of the noninverting, switched capacitor integrator. Assume that the clock frequency is 100kHz and design the ratio of C_1 and C_2 to give an integration frequency of 10kHz.

Solution

The design of C_1/C_2 is accomplished from the ideal integrator transfer function.

$$\frac{C_1}{C_2} = \omega_I T = \frac{2\pi f_I}{f_c} = 0.6283$$

Assume $C_2 = 1\text{F} \rightarrow C_1 = 0.6283\text{F}$.

Next we replace the switched capacitor C_1 and the unswitched capacitor of integrator by the z-domain model of the second row of Fig. 9.4-3 and the first row of Fig. 9.4-4 to obtain Fig. 9.4-12. Note that in addition we used Fig. 9.4-5 for the op amp and assumed that the op amp had a differential voltage gain of 10^6. Also, the unswitched C's are conductances.

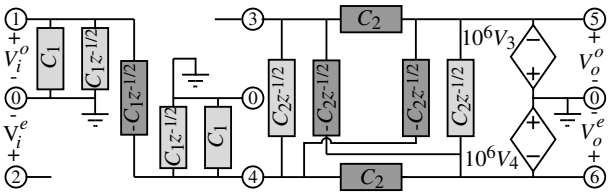


Figure 9.4-12 - z-domain model for noninverting switched capacitor integrator.

As the op amp gain becomes large, the important components are indicated by the darker shading.

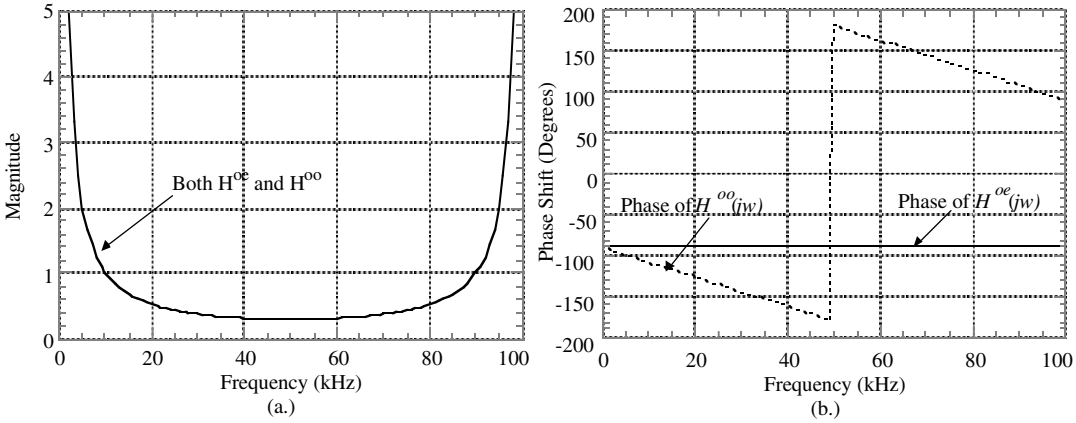
EXAMPLE 9.4-5 - Continued

The SPICE input file to perform a frequency domain simulation of Fig. 9.4-12 is shown below.

```
VIN 1 0 DC 0 AC 1
R10C1 1 0 1.592
X10PC1 1 0 10 DELAY
G10 1 0 10 0 0.6283
X14NC1 1 4 14 DELAY
G14 4 1 14 0 0.6283
R40C1 4 0 1.592
X40PC1 4 0 40 DELAY
G40 4 0 40 0 0.6283
X43PC2 4 3 43 DELAY
G43 4 3 43 0 1
R35 3 5 1.0
X56PC2 5 6 56 DELAY
G56 5 6 56 0 1
R46 4 6 1.0
X36NC2 3 6 36 DELAY
G36 6 3 36 0 1
X45NC2 4 5 45 DELAY
G45 5 4 45 0 1
EODD 6 0 4 0 -1E6
EVEN 5 0 3 0 -1E6
**********
.SUBCKT DELAY 1 2 3
ED 4 0 1 2 1
TD 4 0 3 0 ZO=1K TD=5U
RDO 3 0 1K
.ENDS DELAY
**********
.AC LIN 99 1K 99K
.PRINT AC V(6) VP(6) V(5) VP(5)
.PROBE
.END
```


EXAMPLE 9.4-5 - Continued

Simulation Results:



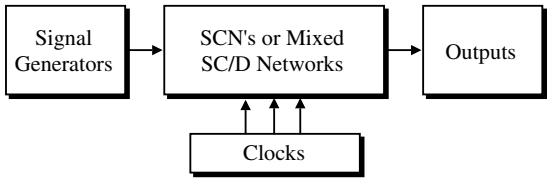
Comments:

- This approach is applicable to all switched capacitor circuits that use two-phase, nonoverlapping clocks.
- If the op amp gain is large, some simplification is possible in the four-port z-domain models.
- The primary advantage of this approach is that it is not necessary to learn a new simulator.

SIMULATION OF SWITCHED CAPACITOR CIRCUITS USING SWITCAP[†]

Introduction

SWITCAP is a general simulation program for analyzing linear switched capacitor networks (SCN's) and mixed switched capacitor/digital (SC/D) networks.



General Setup of SWITCAP

Major Features

1.) Switching Intervals - An arbitrary number of switching intervals per switching period is allowed. The durations of the switching intervals may be unequal and arbitrary.

2.) Network Elements -

ON-OFF switches, linear capacitors, linear VCVS's, and independent voltage sources.

The waveforms of the independent voltage sources may be continuous or piecewise-constant.

The switches in the linear SCN's are controlled by periodic clock waveforms only.

A mixed SC/D network may contain comparators, logic gates such as AND, OR, NOT, NAND, NOR, XOR, and XNOR. The ON-OFF switches in the SC/D network may be controlled not only by periodic waveforms but also by nonperiodic waveforms from the output of comparators and logic gates.

[†] K. Suyama, *Users' Manual for SWITCAP2, Version 1.1*, Dept. of Elect. Engr., Columbia University, New York, NY 10027, Feb. 1992.

SWITCAP - Major Features, Continued

3.) Time-Domain Analyses of Linear SCN's and Mixed SC/D Networks -

a.) Linear SCN's only: The transient response to any prescribed input waveform for $t \geq 0$ after computing the steady-state values for a set of dc inputs for $t < 0$.

b.) Both types of networks: Transient response without computing the steady-state values as initial conditions. A set of the initial condition of analog and digital nodes at $t = 0^-$ may be specified by the user.

4.) Various Waveforms for Time Domain Analyses - Pulse, pulse train, cosine, exponential, exponential cosine, piecewise linear, and dc sources.

5.) Frequency Domain Analyses of Linear SCN's - A single-frequency sinusoidal input can produce a steady-state output containing many frequency components. SWITCAP can determine all of these output frequency components for both continuous and piecewise-constant input waveforms. z-domain quantities can also be computed. Frequency-domain group delay and sensitivity analyses are also provided.

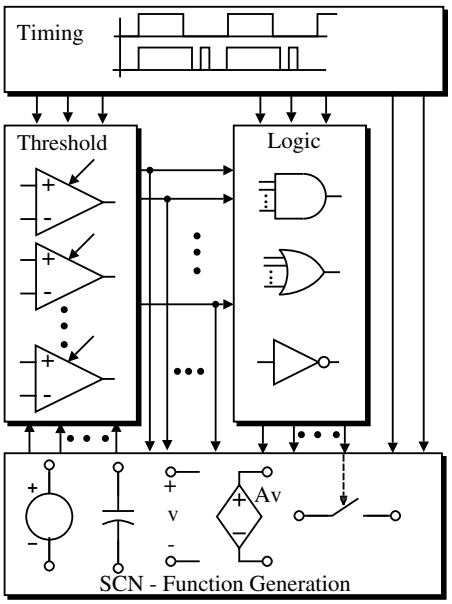
6.) Built-In Sampling Functions - Both the input and output waveforms may be sampled and held at arbitrary instants to produce the desired waveforms for time- and frequency-domain analyses of linear SCN's except for sensitivity analysis. The output waveforms may also be sampled with a train of impulse functions for z-domain analyses.

7.) Subcircuits - Subcircuits, including analog and/or digital elements, may be defined with symbolic values for capacitances, VCVS gains, clocks, and other parameters. Hierarchical use of subcircuits is allowed.

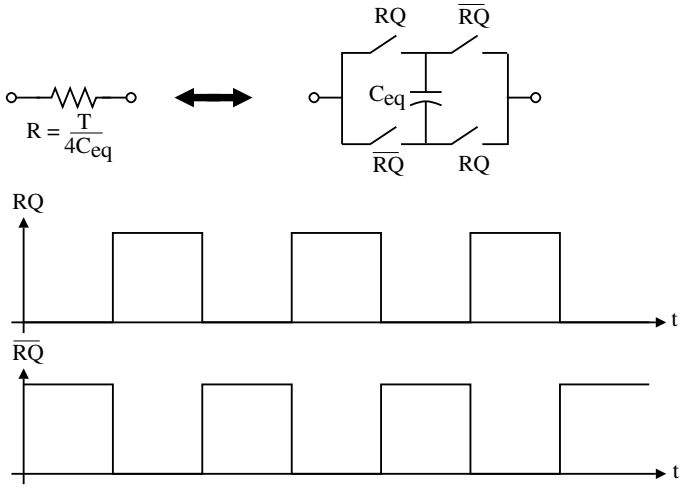
8.) Finite Resistances, Op Amp Poles, and Switch Parasitics - Finite resistance is modeled with SCN's operating at clock frequencies higher than the normal clock. These "resistors" permit the modeling of op amp poles. Capacitors are added to the switch model to represent clock feedthrough.

SWITCAP - MIXED SC/D NETWORKS

Structure of mixed SC/D networks as defined in SWITCAP2.



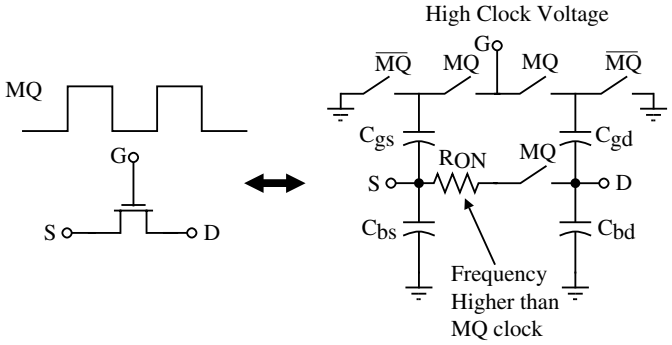
SWITCAP - RESISTORS



The clock, RQ, for the resistor is run at a frequency, much higher than the system clock in order to make the resistor model still approximate a resistor at frequencies near the system clock.

SWITCAP - MOS SWITCHES

MOS Transistor Switch Model:



More information:

SWITCAP Distribution Center
Columbia University
411 Low Memorial Library
New York, NY 10027

suyama@elab.columbia.edu

INFO ON SWITCAP3

Dear Prof. Allen:

Let me explain the latest regarding the development of SWITCAP3.

The current version of SWITCAP is SWITCAP2 version 1.2. It has time-domain and frequency-domain (sinusoidal stead-state, spectrum, frequency-component analyses) analyses, sensitivity analysis, group delay analysis for SCF's. It has also time-domain analysis of mixed switched-capacitor and digital networks so that you can simulate data converters including sigma-delta converters. We only have Sun and HP versions. We don't have a PC version for SWITCAP2.

We are distributing a graphic interface package for SWITCAP2 called XCAP. It has input schematic caption and postprocessing graphics. The package was developed by an outside company.

We have finished 95 percent of SWITCAP3 coding. It will include all the analyses in SWITCAP2 plus noise analysis of SCF's and time- and frequency-domain analyses of switched-current circuits that are modelled using actual MOSFET models (currently, we have BSIM3 and Level 3) and usual SCN ideal components. Although we are already running some examples, it will take a few more months to make a beta-site version available.

I hope the above information is sufficient for your purpose. If you or your students have further questions, please don't hesitate to contact me.

Regards,

Ken Suyama

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Department of Electrical Engineering, Columbia University
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TEL:212-854-6895 FAX:212-663-7203 EMAIL:suyama@elab.columbia.edu

9.5 - FIRST-ORDER, SWITCHED CAPACITOR CIRCUITS

GENERAL, FIRST-ORDER TRANSFER FUNCTIONS

A general first-order transfer function in the s-domain:

$$H(s) = \frac{sa_1 \pm a_0}{s + b_0}$$

$a_1 = 0 \Rightarrow$ Low pass, $a_0 = 0 \Rightarrow$ High Pass, $a_0 \neq 0$ and $a_1 \neq 0 \Rightarrow$ All pass

Note that the zero can be in the *RHP* or *LHP*.

A general first-order transfer function in the z-domain:

$$H(z) = \frac{zA_1 \pm A_0}{z - B_0} = \frac{A_1 \pm A_0 z^{-1}}{1 - B_0 z^{-1}}$$

NONINVERTING, FIRST-ORDER, LOW PASS CIRCUIT

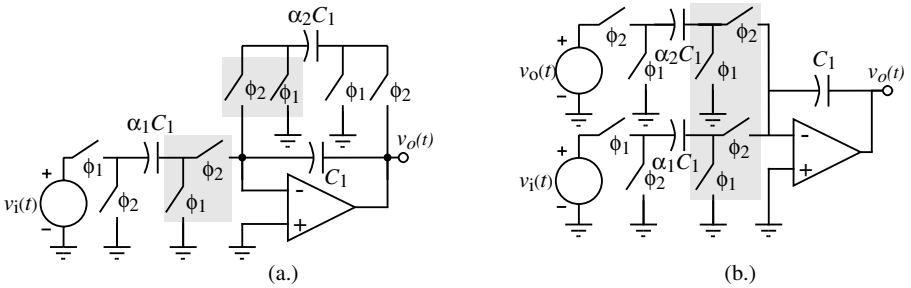


Figure 9.5-1 - (a.) Noninverting, first-order low pass circuit. (b.) Equivalent circuit of Fig. 9.5-1a.

Transfer function:

Summing currents flowing toward the inverting op amp terminal gives

$$\alpha_2 C_1 V_o^e(z) - \alpha_1 C_1 z^{-1/2} V_i^o(z) + C_1(1-z^{-1}) V_o^e(z) = 0$$

Solving for $V_o^o(z)/V_i^o(z)$ gives

$$\frac{V_o^o(z)}{V_i^o(z)} = \frac{\alpha_1 z^{-1}}{1 + \alpha_2 - z^{-1}} = \frac{\dfrac{\alpha_1 z^{-1}}{1+\alpha_2}}{1 - \dfrac{z^{-1}}{1+\alpha_2}}$$

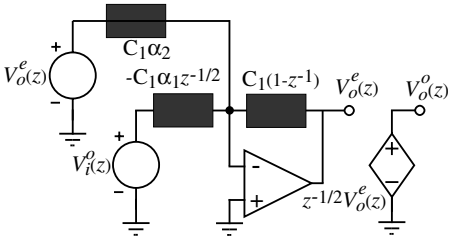


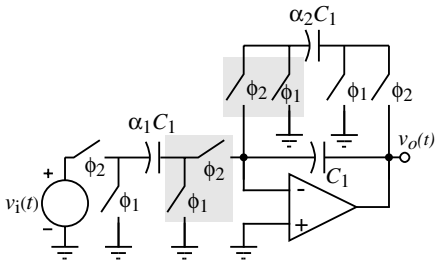
Figure 9.5-2 - z-domain model of Fig. 9.5-1b.

Equating the above to the *H(z)* of the previous page gives the design equations for Fig. 9.5-2 as

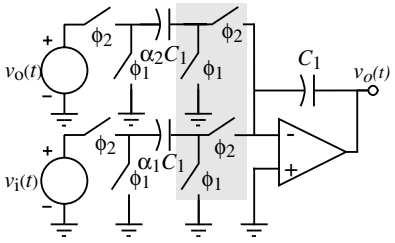
$$\alpha_1 = \frac{A_0}{B_0} \qquad \text{and} \qquad \alpha_2 = \left(\frac{1-B_0}{B_0}\right)$$

INVERTING, FIRST-ORDER, LOW PASS CIRCUIT

An inverting low pass circuit can be obtained by reversing the phases of the leftmost two switches in Fig. 9.5-1a.



Inverting, first-order low pass circuit.



Equivalent circuit.

It can be shown that,

$$\frac{V_o^e(z)}{V_i^e(z)} = \frac{-\alpha_1}{1 + \alpha_2 - z^{-1}} = \frac{\dfrac{-\alpha_1}{1+\alpha_2}}{1 - \dfrac{z^{-1}}{1+\alpha_2}}$$

Equating to *H(z)* gives the design equations for the inverting low pass circuit as

$$\alpha_1 = \frac{-A_1}{B_0} \qquad \text{and} \qquad \alpha_2 = \left(\frac{1-B_0}{B_0}\right)$$

EXAMPLE 9.5-1 - Design of a Switched Capacitor First-Order Circuit

Design a switched capacitor first-order circuit that has a low frequency gain of +10 and a -3dB frequency of 1kHz. Give the value of the capacitor ratios α_1 and α_2. Use a clock frequency of 100kHz.

Solution

Assume that the clock frequency, f_c, is much larger than the -3dB frequency. In this example, the clock frequency is 100 times larger so this assumption should be valid.

Based on this assumption, we approximate z^{-1} as

$$z^{-1} = e^{-sT} \approx 1 - sT + \cdots \quad (1)$$

Rewrite the z-domain transfer function as

$$\frac{V_o^o(z)}{V_i^o(z)} = \frac{\alpha_1 z^{-1}}{\alpha_2 + 1 - z^{-1}} \quad (2)$$

Next, we note from Eq. (1) that $1-z^{-1} \approx sT$. Furthermore, if $sT<<1$, then $z^{-1} \approx 1$. (Note that $sT<<1$ is equivalent to $\omega << f_c$ which is valid.)

Making these substitutions in Eq. (2), we get

$$\frac{V_o^o(z)}{V_i^o(z)} \approx \frac{\alpha_1}{\alpha_2 + sT} = \frac{\alpha_1/\alpha_2}{1 + s(T/\alpha_2)} \quad (3)$$

Equating Eq. (3) to the specifications gives $\alpha_1 = 10\alpha_2$ and $\alpha_2 = \dfrac{\omega_{-3dB}}{f_c}$

$\therefore$ $\boxed{\alpha_2 = 6283/100{,}000 = 0.0628 \text{ and } \alpha_1 = 0.6283}$

FIRST-ORDER, HIGH PASS CIRCUIT

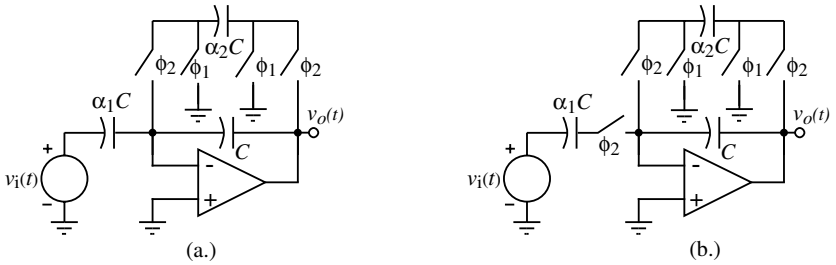


Figure 9.5-3 - (a.) Switched-capacitor, high pass circuit. (b.) Version of Fig. 9.5-3a that constrains the charging of C_1 to the ϕ_2 phase.

Transfer function:

Summing currents at the inverting input node of the op amp gives

$$\alpha_1(1-z^{-1})V_o^e(z) + \alpha_2 V_o^e(z) + (1-z^{-1})V_i^e(z) = 0 \quad (1)$$

Solving for the $H^{ee}(z)$ transfer function gives

$$H^{ee}(z) = \frac{V_o^e(z)}{V_i^e(z)} = \frac{-\alpha_1(1-z^{-1})}{\alpha_2+1-z^{-1}} = \frac{\dfrac{\alpha_1}{\alpha_2+1}(1-z^{-1})}{1 - \dfrac{1}{\alpha_2+1}z^{-1}} \quad (2)$$

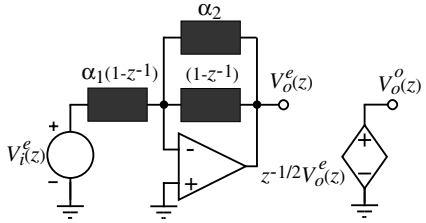


Figure 9.5-4 - z-domain model for Fig. 9.5-3.

Equating Eq. (2) to $H(z)$ gives,

$$\alpha_1 = \frac{-A_1}{B_0} \qquad \text{and} \qquad \alpha_2 = 1 - \frac{1}{B_0}$$

FIRST-ORDER, ALLPASS CIRCUIT

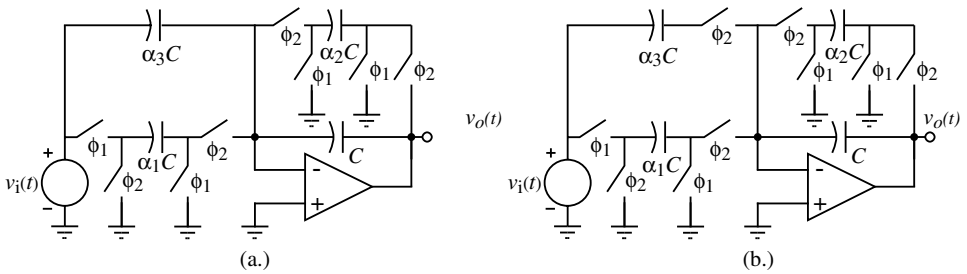


Figure 9.5-5 - (a.) High or low frequency boost circuit. (b.) Modification of (a.) to simplify the z-domain modeling

Transfer function:

Summing the currents flowing into the inverting input of the op amp gives

$$-\alpha_1 z^{-1/2}V_i^o(z)+\alpha_3 z^{-1/2}V_i^e(z)+\alpha_2 V_o^e(z)+(1-z^{-1})V_o^e(z) = 0$$

Since $V_i^o(z) = z^{-1/2}V_i^e(z)$, then the above becomes

$$V_o^e(z)\left[\alpha_2+1-\alpha z^{-1}\right] = \alpha_1 z^{-1}V_i^e(z) - \alpha_3(1-z^{-1})V_i^e(z)$$

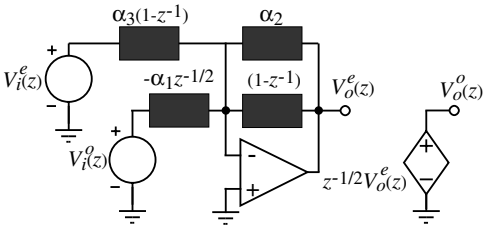


Figure 9.5-6 - z-domain model for Fig. 9.5-5b.

Solving for $H^{ee}(z)$ gives

$$H^{ee}(z) = \frac{\alpha_1 z^{-1} - \alpha_3(1-z^{-1})}{\alpha_2 + (1-z^{-1})} = \left(\frac{-\alpha_3}{\alpha_2+1}\right)\frac{1 - \dfrac{\alpha_1+\alpha_3}{\alpha_3}z^{-1}}{1 - \dfrac{z^{-1}}{\alpha_2+1}} \quad \Rightarrow \quad \alpha_1 = \frac{A_1+A_0}{B_0},\ \alpha_2 = 1 - \frac{1}{B_0} \ \text{ and } \ \alpha_3 = \frac{-A_0}{B_0}$$

EXAMPLE 9.5-2 - Design of a Switched Capacitor Bass Boost Circuit

Find the values of the capacitor ratios α_1, α_2, and α_3 using a 100kHz clock for Fig. 9.5-5 that will realize the asymptotic frequency response shown in Fig. 9.5-7.

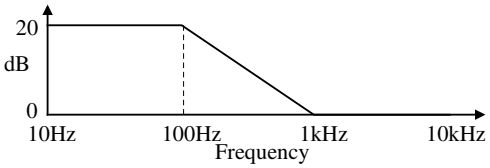


Figure 9.5-7 - Bass boost response for Ex. 9.5-2.

Solution

Since the specification for the example is given in the continuous time frequency domain, let us use the approximation that $z^{-1} \approx 1$ and $1-z^{-1} \approx sT$, where T is the period of the clock frequency. Therefore, the allpass transfer function can be written as

$$H^{ee}(s) \approx \frac{-sT\alpha_3 + \alpha_1}{sT + \alpha_2} = -\frac{\alpha_1}{\alpha_2}\left(\frac{sT\alpha_3/\alpha_1 - 1}{sT/\alpha_2 + 1}\right)$$

From Fig. 9.5-7, we see that the desired response has a dc gain of 10, a right-half plane zero at 2π kHz and a pole at -200π Hz. Thus, we see that the following relationships must hold.

$$\frac{\alpha_1}{\alpha_2} = 10\ , \qquad \frac{\alpha_1}{T\alpha_3} = 2000\pi\ , \qquad \text{and} \qquad \frac{\alpha_2}{T} = 200\pi$$

From these relationships we get the desired values as

$$\boxed{\alpha_1 = \frac{2000\pi}{f_c}, \quad \alpha_2 = \frac{200\pi}{f_c}, \ \text{and} \ \ \alpha_3 = 1}$$

PRACTICAL IMPLEMENTATIONS OF THE FIRST-ORDER CIRCUITS

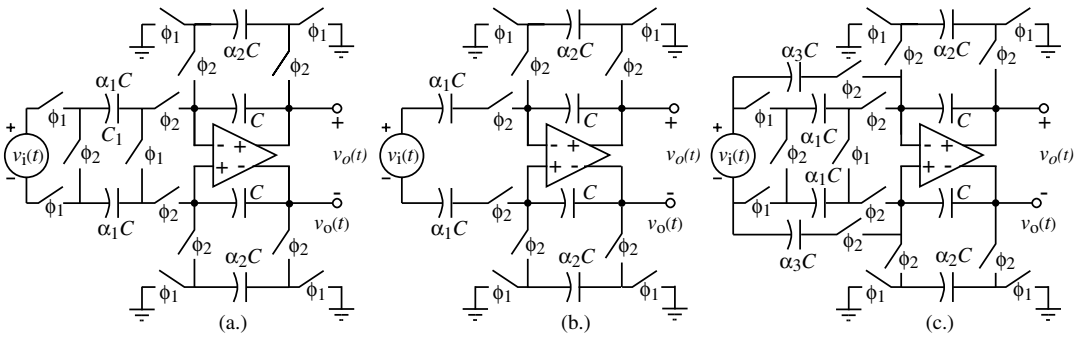


Figure 9.5-8 - Differential implementations of (a.) Fig. 9.5-1, (b.) Fig. 9.5-3, and (c.) Fig. 9.5-5.

Comments:

- Differential operation reduces clock feedthrough, common mode noise sources and enhances the signal swing.
- Differential operation requires op amps or OTAs with differential outputs which in turn requires a means of stabilizing the output common mode voltage.

9.6 - SECOND-ORDER SWITCHED CAPACITOR CIRCUITS

WHY SECOND-ORDER CIRCUITS?

They are fundamental blocks in switched capacitor filters.

Switched Capacitor Filter Design Approaches

- Cascade design

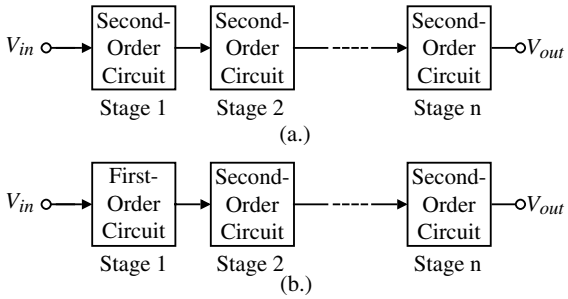


Figure 9.6-1 - (a.) Cascade design when n is even. (b.) Cascade designwhen n is odd.

- Ladder design

  Also uses first- and second-order circuits

There are also other applications of first- and second-order circuits:

- Oscillators
- Converters

BIQUAD TRANSFER FUNCTION

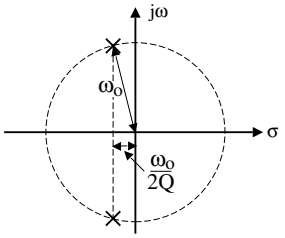
A biquad has two poles and two zeros.

Poles are complex and always in the LHP.

The zeros may or may not be complex and may be in the LHP or the RHP.

Transfer function:

$$H_a(s) = \frac{V_{out}(s)}{V_{in}(s)} = \frac{-(K_2 s^2 + K_1 s + K_0)}{s^2 + \frac{\omega_o}{Q} s + \omega_o^2} = K\left(\frac{(s-z_1)(s-z_2)}{(s-p_1)(s-p_2)}\right)$$



Low pass: zeros at ∞

High pass: zeros at 0

Bandpass: One zero at 0 and the other at ∞

Bandstop: zeros at $\pm j\omega_o$

Allpass: Poles and zeros are complex conjugates

LOW-Q, SWITCHED CAPACITOR BIQUAD

Development of the Biquad:

Rewrite H_a(s) as:

$$s^2 V_{out}(s) + \frac{\omega_o s}{Q} V_{out}(s) + \omega_o^2 V_{out}(s) = -(K_2 s^2 + K_1 s + K_0) V_{in}(s)$$

Dividing through by s^2 and solving for $V_{out}(s)$, gives

$$V_{out}(s) = \frac{-1}{s}\left[(K_1 + K_2 s) V_{in}(s) + \frac{\omega_o}{Q} V_{out}(s) + \frac{1}{s}(K_0 V_{in}(s) + \omega_o^2 V_{out}(s))\right]$$

If we define the voltage V_1(s) as

$$V_1(s) = \frac{-1}{s}\left[\frac{K_0}{\omega_o} V_{in}(s) + \omega_o V_{out}(s)\right]$$

then $V_{out}(s)$ can be expressed as

$$V_{out}(s) = \frac{-1}{s}\left[(K_1 + K_2 s)\, V_{in}(s) + \frac{\omega_o}{Q} V_{out}(s) - \omega_o V_1(s)\right]$$

Synthesizing the voltages $V_1(s)$ and $V_{out}(s)$, gives

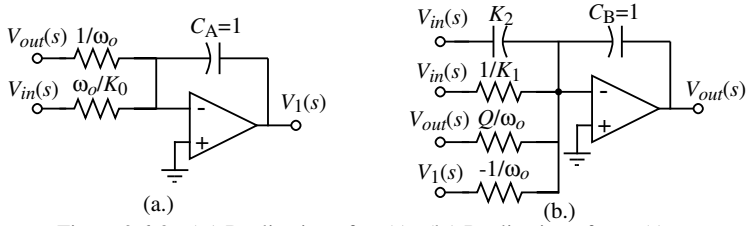


Figure 9.6-2 - (a.) Realization of $V_1(s)$. (b.) Realization of $V_{out}(s)$.

LOW-Q, SWITCHED CAPACITOR BIQUAD - Continued

Replace the continuous time integrators with switched capacitor integrators to get:

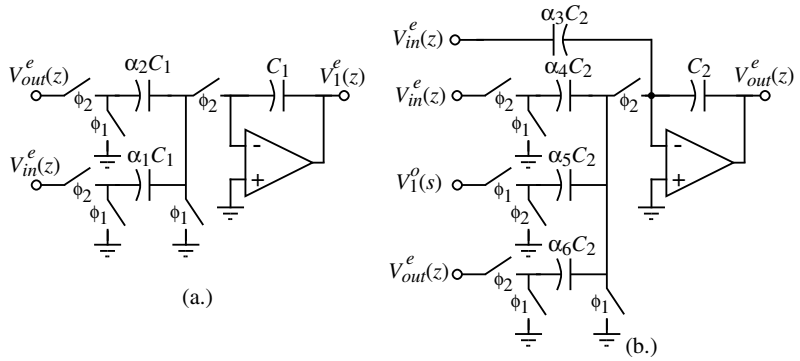


Figure 9.6-3 - (a.) Switched capacitor realization of Fig. 9.6-2a. (b.) Switched capacitor realization of Fig. 9.6-2b.

From these circuits we can write that:

$$V^e_1(z) = -\frac{\alpha_1}{1-z^{-1}} V^e_{in}(z) - \frac{\alpha_2}{1-z^{-1}} V^e_{out}(z)$$

and

$$V^e_{out}(z) = -\alpha_3 V^e_{in}(z) - \frac{\alpha_4}{1-z^{-1}} V^e_{in}(z) + \frac{\alpha_5 z^{-1}}{1-z^{-1}} V^e_1(z) - \frac{\alpha_6}{1-z^{-1}} V^e_{out}(z) .$$

Note that we multiplied the $V^o_1(z)$ input of Fig. 9.6-3b by $z^{-1/2}$ to convert it to $V^e_1(z)$.

LOW-Q, SWITCHED CAPACITOR BIQUAD - Continued

Connecting the two circuits of Fig. 9.6-3 together gives the desired, low-Q, biquad realization.

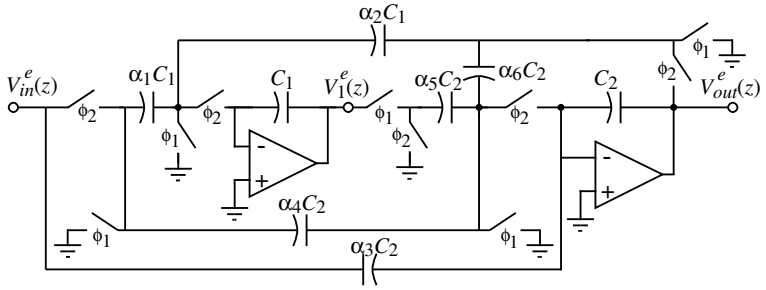


Figure 9.6-4 - Low Q, switched capacitor, biquad realization.

If we assume that $\omega T << 1$, then $1-z^{-1} \approx sT$ and $V^e_1(z)$ and $V^e_{out}(z)$ can be approximated as

$$V^e_1(s) \approx -\frac{\alpha_1}{sT} V^e_{in}(s) - \frac{\alpha_2}{sT} V^e_{out}(s) = \frac{-1}{s}\left[\frac{\alpha_1}{T} V^e_{in}(s) + \frac{\alpha_2}{T} V^e_{out}(s)\right]$$

and

$$V^e_{out}(s) \approx \frac{-1}{s}\left[(\frac{\alpha_4}{T} + s\alpha_3) V^e_{in}(s) + \frac{\alpha_5}{T} V^e_1(s) + \frac{\alpha_6}{sT} V^e_{out}(s)\right] .$$

These equations can be combined to give the transfer function, $H^{ee}(s)$ as follows.

$$H^{ee}(s) \approx \frac{-\left[\alpha_3 s^2 + \frac{s\alpha_4}{T} + \frac{\alpha_1\alpha_5}{T^2}\right]}{s^2 + \frac{s\alpha_6}{T} + \frac{\alpha_2\alpha_5}{T^2}}$$

LOW-Q, SWITCHED CAPACITOR BIQUAD - Continued

Equating $H^{ee}(s)$ to $H_a(s)$ gives

$$\frac{-\left[\alpha_3 s^2 + \frac{s\alpha_4}{T} + \frac{\alpha_1\alpha_5}{T^2}\right]}{s^2 + \frac{s\alpha_6}{T} + \frac{\alpha_2\alpha_5}{T^2}} = \frac{-(K_2 s^2 + K_1 s + K_0)}{s^2 + \frac{\omega_o}{Q}s + \omega_o^2}$$

which gives,

$$\alpha_1 = \frac{K_0 T}{\omega_o},\ \alpha_2 = |\alpha_5| = \omega_o T,\ \alpha_3 = K_2,\ \alpha_4 = K_1 T,\ \text{and}\ \alpha_6 = \frac{\omega_o T}{Q}\ .$$

Largest capacitor ratio:

If $Q > 1$ and $\omega_o T << 1$, the largest capacitor ratio is α_6.

For this reason, the low-Q, switched capacitor biquad is restricted to $Q < 5$.

Sum of capacitance:

To find this value, normalize all of the capacitors connected or switched into the inverting terminal of each op amp by the smallest capacitor, $\alpha_{min}C$. The sum of the normalized capacitors associated with each op amp will be the sum of the capacitance connected to that op amp. Thus,

$$\Sigma C = \frac{1}{\alpha_{min}} \sum_{i=1}^{n} \alpha_i$$

where there are n capacitors connected to the op amp inverting terminal, including the integrating capacitor.

EXAMPLE 9.6-1- Design of a Switched Capacitor, Low-Q, Biquad

Assume that the specifications of a biquad are f_o = 1kHz, Q = 2, $K_0 = K_2 = 0$, and $K_1 = 2\pi f_o/Q$ (a bandpass filter). The clock frequency is 100kHz. Design the capacitor ratios of Fig. 9.6-4 and determine the maximum capacitor ratio and the total capacitance assuming that C_1 and C_2 have unit values.

Solution

From the previous slide we have

$$\alpha_1 = \frac{K_0 T}{\omega_o},\ \alpha_2 = |\alpha_5| = \omega_o T,\ \alpha_3 = K_2,\ \alpha_4 = K_1 T,\ \text{and}\ \alpha_6 = \frac{\omega_o T}{Q}\ .$$

Setting $K_0 = K_2 = 0$, and $K_1 = 2\pi f_o/Q$ and letting f_o = 1kHz, Q = 2 gives

$\alpha_1 = \alpha_3 = 0$, $\alpha_2 = \alpha_5 = 0.0628$, and $\alpha_4 = \alpha_6 = 0.0314$.

The largest capacitor ratio is α_4 or α_6 and is 1/31.83.

Σ capacitors connected to the input op amp = 1/0.0628 + 1 = 16.916.

Σ capacitors connected to the second op amp = 0.0628/0.0314 + 1/0.0314 + 2 = 35.85.

Therefore, the total biquad capacitance is 52.76 units of capacitance.

(Note that this number will decrease as the clock frequency becomes closer to the signal frequencies.)

Z-DOMAIN CHARACTERIZATION OF THE LOW-Q, BIQUAD

Combining the following two equations,

$$V_1^e(z) = -\frac{\alpha_1}{1-z^{-1}} V_{in}^e(z) - \frac{\alpha_2}{1-z^{-1}} V_{out}^e(z)$$

and

$$V_{out}^e(z) = -\alpha_3 V_{in}^e(z) - \frac{\alpha_4}{1-z^{-1}} V_{in}^e(z) + \frac{\alpha_5 z^{-1}}{1-z^{-1}} V_1^e(z) - \frac{\alpha_6}{1-z^{-1}} V_{out}^e(z) .$$

gives,

$$\frac{V_{out}^e(z)}{V_{in}^e(z)} = H^{ee}(z) = -\frac{(\alpha_3 + \alpha_4)z^2 + (\alpha_1\alpha_5 - \alpha_4 - 2\alpha_3)z + \alpha_3}{(1 + \alpha_6)z^2 + (\alpha_2\alpha_5 - \alpha_6 - 2)z + 1}$$

A general z-domain specification for a biquad can be written as

$$H(z) = -\frac{a_2z^2 + a_1z + a_0}{b_2z^2 + b_1z + 1}$$

Equating coefficients gives

$\alpha_3 = a_0$, $\alpha_4 = a_2 - a_0$, $\alpha_1\alpha_5 = a_2 + a_1 + a_0$, $\alpha_6 = b_2 - 1$, and $\alpha_2\alpha_5 = b_2 + b_1 + 1$

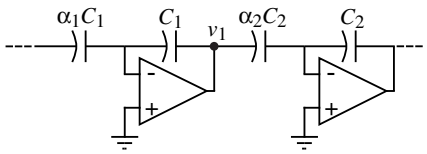
Because there are 5 equations and 6 unknowns, an additional relationship can be introduced. One approach would be to select $\alpha_5 = 1$ and solve for the remaining capacitor ratios. Alternately, one could let $\alpha_2 = \alpha_5$ which makes the integrator frequency of both integrators in the feedback loop equal.

VOLTAGE SCALING

It is desirable to keep the amplitudes of the output voltages of the two op amps approximately equal over the frequency range of interest. This can be done by voltage scaling.

If the voltage at the output node of an op amp in a switched capacitor circuit is to be scaled by a factor of k, then all switched and unswitched capacitors connected to that output node must be scaled by a factor of 1/k.

For example,



The charge associated with v_1 is:

$$Q(v_1) = C_1v_1 + \alpha_2C_2v_1$$

Suppose we wish to scale the value of v_1 by k_1 so that $v_1' = k_1v_1$. Therefore,

$$Q(v_1') = C_1v_1' + \alpha_2C_2v_1' = C_1k_1v_1 + \alpha_2C_2k_1v_1$$

But, $Q(v_1) = Q(v_1')$ so that $C_1' = C_1/k_1$ and $C_2' = C_2/k_1$.

This scaling is based on keeping the total charge associated with a node constant. The choice above of $\alpha_2 = \alpha_5$ results in a near-optimally scaled dynamic range realization.

HIGH-Q, SWITCHED CAPACITOR BIQUAD

Desired: A biquad capable of realizing higher values of Q without suffering large element spreads.

Development of such a biquad:

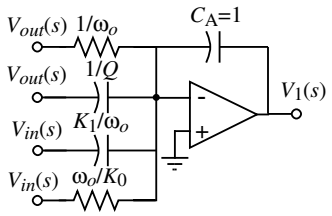
Reformulate the equations for $V_1(s)$ and $V_{out}(s)$ as follows,

$$V_{out}(s) = -\frac{1}{s}\left[K_2 s V_{in} - \omega_o V_1(s)\right]$$

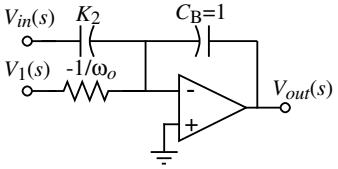
and

$$V_1(s) = -\frac{1}{s}\left[\left(\frac{K_0}{\omega_o} + \frac{K_1}{\omega_o}s\right)V_{in}(s) + \left(\omega_o + \frac{s}{Q}\right)V_{out}(s)\right]$$

Synthesizing these equations:



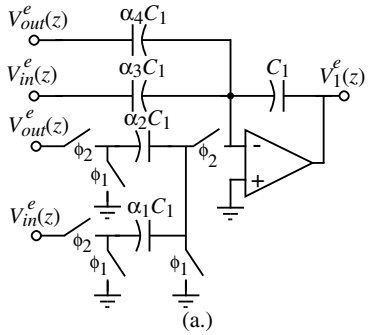
Realization of $V_1(s)$.



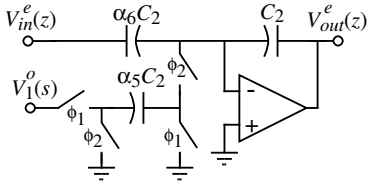
Realization of $V_{out}(s)$.

HIGH-Q, SWITCHED CAPACITOR BIQUAD - Continued

Replace the continuous time integrators with switched capacitor integrators to get:



(a.)



(b.)

Figure 9.6-6 - (a.) Switched capacitor realization of Fig. 9.6-5a. (b.) Switched capacitor realization of Fig. 9.6-5b.

From these circuits we can write that:

$$V^e_1(z) = -\frac{\alpha_1}{1-z^{-1}}V^e_{in}(z) - \frac{\alpha_2}{1-z^{-1}}V^e_{out}(z) - \alpha_3 V^e_{in}(z) - \alpha_4 V^e_{out}(z)$$

and

$$V^e_{out}(z) = -\alpha_6 V^e_{in}(z) + \frac{\alpha_5 z^{-1}}{1-z^{-1}}V^e_1(z)\,.$$

Note that we multiplied the $V^o_1(z)$ input of Fig. 9.6-6b by $z^{-1/2}$ to convert it to $V^e_1(z)$.

HIGH-Q, SWITCHED CAPACITOR BIQUAD - Continued

Connecting the two circuits of Fig. 9.6-6 together gives the desired, high-Q biquad realization.

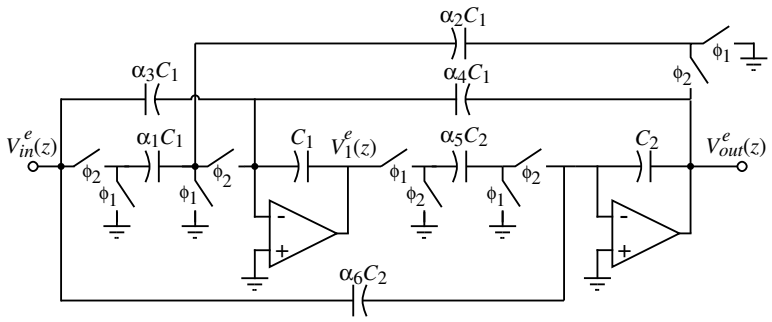


Figure 9.6-7 - High Q, switched capacitor, biquad realization.

If we assume that $\omega T << 1$, then $1-z^{-1} \approx sT$ and $V_1^e(z)$ and $V_{out}^e(z)$ can be approximated as

$$V_1^e(s) \approx -\frac{1}{s}\left(\frac{\alpha_1}{T} + s\alpha_3\right)V_{in}^e(s) - \frac{1}{s}\left(\frac{\alpha_2}{T} + s\alpha_4\right)V_{out}^e(s) \tag{19}$$

and

$$V_{out}^e(s) \approx \frac{-1}{s}\left[(s\alpha_6)V_{in}^e(s) - \frac{\alpha_5}{T}V_1^e(s)\right]. \tag{20}$$

These equations can be combined to give the transfer function, $H^{ee}(s)$ as follows.

$$H^{ee}(s) \approx \frac{-\left[\alpha_6 s^2 + \frac{s\alpha_3\alpha_5}{T} + \frac{\alpha_1\alpha_5}{T^2}\right]}{s^2 + \frac{s\alpha_4\alpha_5}{T} + \frac{\alpha_2\alpha_5}{T^2}}$$

HIGH-Q, SWITCHED CAPACITOR BIQUAD - Continued

Equating $H^{ee}(s)$ to $H_a(s)$ gives

$$\frac{-\left[\alpha_6 s^2 + \frac{s\alpha_3\alpha_5}{T} + \frac{\alpha_1\alpha_5}{T^2}\right]}{s^2 + \frac{s\alpha_4\alpha_5}{T} + \frac{\alpha_2\alpha_5}{T^2}} = \frac{-(K_2 s_2 + K_1 s + K_0)}{s^2 + \frac{\omega_o}{Q}s + \omega_o^2}$$

which gives,

$$\alpha_1 = \frac{K_0 T}{\omega_o}, \quad \alpha_2 = |\alpha_5| = \omega_o T, \quad \alpha_3 = \frac{K_1}{\omega_o}, \quad \alpha_4 = \frac{1}{Q}, \quad \text{and} \quad \alpha_6 = K_2 .$$

Largest capacitor ratio:

If $Q > 1$ and $\omega_o T << 1$, the largest capacitor ratio is α_2 (α_5) or α_4 depending on the values of Q and $\omega_o T$.

EXAMPLE 9.6-2 - Design of a Switched Capacitor, High-Q, Biquad

Assume that the specifications of a biquad are f_o = 1kHz, Q = 10, $K_0 = K_2 = 0$, and $K_1 = 2\pi f_o/Q$ (a bandpass filter). The clock frequency is 100kHz. Design the capacitor ratios of the high-Q biquad of Fig. 9.6-4 and determine the maximum capacitor ratio and the total capacitance assuming that C_1 and C_2 have unit values.

Solution

From the previous slide we have,

$$\alpha_1 = \frac{K_0 T}{\omega_o}, \quad \alpha_2 = |\alpha_5| = \omega_o T, \quad \alpha_3 = \frac{K_1}{\omega_o}, \quad \alpha_4 = \frac{1}{Q}, \text{ and } \quad \alpha_6 = K_2 .$$

Using f_o = 1kHz, Q = 10 and setting $K_0 = K_2 = 0$, and $K_1 = 2\pi f_o/Q$ (a bandpass filter) gives

$$\alpha_1 = \alpha_6 = 0, \ \alpha_2 = \alpha_5 = 0.0628, \text{ and } \alpha_3 = \alpha_4 = 0.1.$$

The largest capacitor ratio is α_2 or α_5 and is 1/15.92.

Σ capacitors connected to the input op amp = 1/0.0628 + 2(0.1/0.0628) + 1 = 20.103.

Σ capacitors connected to the second op amp = 1/0.0628 + 1 = 16.916.

Therefore, the total biquad capacitance is 36.02 units of capacitance.

Z-DOMAIN CHARACTERIZATION OF THE HIGH-Q, BIQUAD

Combining the following two equations,

$$V_1^e(z) = -\frac{\alpha_1}{1-z^{-1}} V_{in}^e(z) - \frac{\alpha_2}{1-z^{-1}} V_{out}^e(z) - \alpha_3 V_{in}^e(z) - \alpha_4 V_{out}^e(z)$$

and

$$V_{out}^e(z) = -\alpha_6 V_{in}^e(z) + \frac{\alpha_5 z^{-1}}{1-z^{-1}} V_1^e(z)$$

gives,

$$\frac{V_{out}^e(z)}{V_{in}^e(z)} = H^{ee}(z) = -\frac{\alpha_6 z^2 + (\alpha_3\alpha_5 - \alpha_1\alpha_5 - 2\alpha_6)z + (\alpha_6 - \alpha_3\alpha_5)}{z^2 + (\alpha_4\alpha_5 + \alpha_2\alpha_5 - 2)z + (1 - \alpha_4\alpha_5)}$$

A general z-domain specification for a biquad can be written as

$$H(z) = -\frac{a_2 z^2 + a_1 z + a_0}{b_2 z^2 + b_1 z + 1} = -\frac{(a_2/b_2)z^2 + (a_1/b_2)z + (a_0/b_2)}{z^2 + (b_1/b_2)z + (b_0/b_2)}$$

Equating coefficients gives

$$\alpha_6 = \frac{a_2}{b_2}, \ \alpha_3\alpha_5 = \frac{a_2 - a_0}{b_2}, \ \alpha_1\alpha_5 = \frac{a_2 + a_1 + a_0}{b_2}, \ \alpha_4\alpha_5 = 1 - \frac{1}{b_2} \text{ and } \alpha_2\alpha_5 = 1 + \frac{b_1 + 1}{2}$$

Because there are 5 equations and 6 unknowns, an additional relationship can be introduced. One approach would be to select $\alpha_5 = 1$ and solve for the remaining capacitor ratios. Alternately, one could let $\alpha_2 = \alpha_5$ which makes the integrator frequency of both integrators in the feedback loop equal.

FLEISCHER-LAKER, SWITCHED CAPACITOR BIQUAD†

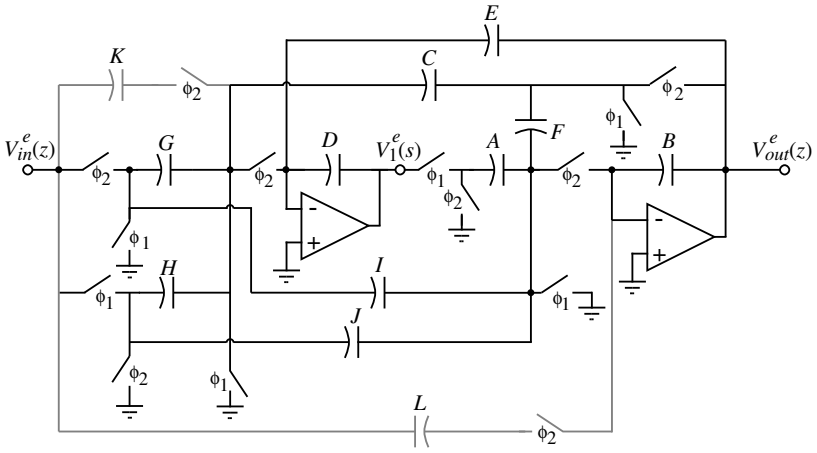


Figure 9.6-8 - Fleischer-Laker, switched capacitor biquad.

$$\frac{V^e_{out}(z)}{V^e_{in}(z)} = \frac{(D\hat{J} - A\hat{H})z^{-2} - [D(\hat{I} + \hat{J}) - A\hat{G}]z - D\hat{I}}{(DB - AE)z^{-2} - [2DB - A(C + E) + DF]z^{-1} + D(B + F)}$$

$$\frac{V^e_1(z)}{V^e_{in}(z)} = \frac{(E\hat{J} - B\hat{H})z^{-2} + [B(\hat{G} + \hat{H}) + F\hat{H} - E(\hat{I} + \hat{J}) - C\hat{J}]z^{-1} - [\hat{I}(C+E) - \hat{G}(F+B)]}{(DB - AE)z^{-2} - [2DB - A(C + E) + DF]z^{-1} + D(B + F)}$$

where $\hat{G} = G+L$, $\hat{H} = H+L$, $\hat{I} = I+K$ and $\hat{J} = J+L$

† P.E. Fleischer and K.R. Laker, "A Family of Active Switched Capacitor Biquad Building Blocks," *Bell System Technical Journal*, vol. 58, no. 10, Dec. 1979, pp. 2235-2269.

Z-DOMAIN MODEL OF THE FLEISCHER-LAKER BIQUAD

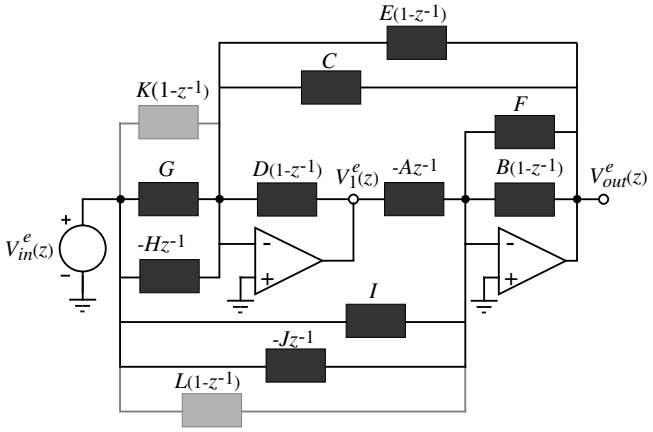


Figure 9.6-9 - z-domain equivalent circuit for the Fleischer-Laker biquad of Fig. 9.6-8.

Type 1E Biquad ($F = 0$)

$$\frac{V^e_{out}}{V^e_{in}} = \frac{z^{-2}(JD - HA) + z^{-1}(AG - DJ - DI) + DI}{z^{-2}(DB - AE) + z^{-1}(AC + AE - 2BD) + BD} \tag{1}$$

and

$$\frac{V^e_1}{V^e_{in}} = \frac{z^{-2}(EJ - HB) + z^{-1}(GB + HB - IE - CJ - EJ) + (IC + IE - GB)}{z^{-2}(DB - AE) + z^{-1}(AC + AE - 2BD) + BD} \tag{2}$$

Z-DOMAIN MODEL OF THE FLEISCHER-LAKER BIQUAD - Continued

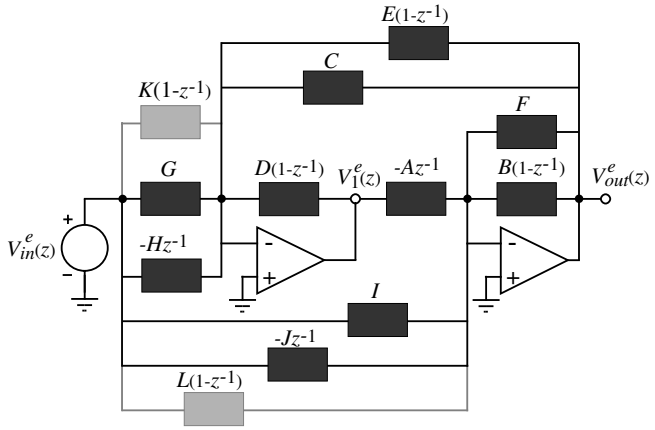


Figure 9.6-9 - z-domain equivalent circuit for the Fleischer-Laker biquad of Fig. 9.6-8.

Type 1F Biquad ($E = 0$)

$$\frac{V_{out}^e}{V_{in}^e} = \frac{z^{-2}(JD - HA) + z^{-1}(AG - DJ - DI) + DI}{z^{-2}DB + z^{-1}(AC - 2BD - DF) + (BD + DF)} \tag{3}$$

and

$$\frac{V_1^e}{V_{in}^e} = \frac{-z^{-2}HB + z^{-1}(GB + HB + HF - CJ) + (IC + GF - GB)}{z^{-2}DB + z^{-1}(AC - 2BD - DF) + (BD + DF)} \tag{4}$$

EXAMPLE 9.6-3 - Design of a Switched Capacitor, Fleischer-Laker Biquad

Use the Fleischer-Laker biquad to implement the following z-domain transfer function which has poles in the z-domain at $r = 0.98$ and $\theta = \pm 6.2°$.

$$H(z) = \frac{0.003z^{-2} + 0.006z^{-1} + 0.003}{0.9604z^{-2} - 1.9485z^{-1} + 1}$$

Solution

Let us begin by selecting a *Type 1E* Fleischer-Laker biquad. Equating the numerator of Eq. (1) with the numerator of H(z) gives

$DI = 0.003$ $AG\text{-}DJ\text{-}DI = 0.006 \rightarrow AG\text{-}DJ = 0.009$ $DJ\text{-}HA = 0.003$

If we arbitrarily choose $H = 0$, we get

$DI = 0.003$ $JD = 0.003$ $AG = 0.012$

Picking $D = A = 1$ gives $I = 0.003$, $J = 0.003$ and $G = 0.012$. Equating the denominator terms of Eq. (1) with the denominator of H(z), gives

$BD = 1$ $BD\text{-}AE = 0.9604 \rightarrow AE = 0.0396$

$AC\text{+}AE\text{-}2BD = -1.9485 \rightarrow AC\text{+}AE = 0.0515 \rightarrow AC = 0.0119$

Because we have selected $D = A = 1$, we get $B = 1$, $E = 0.0396$, and $C = 0.0119$. If any capacitor value was negative, the procedure would have to be changed by making different choices or choosing a different realization such as *Type 1F*.

Since each of the alphabetic symbols is a capacitor, the largest capacitor ratio will be D or A divided by I or J which gives 333. The large capacitor ratio is being caused by the term $BD = 1$. If we switch to the *Type 1F*, the term $BD = 0.9604$ will cause large capacitor ratios. This example is a case where both the E and F capacitors are needed to maintain a smaller capacitor ratio.

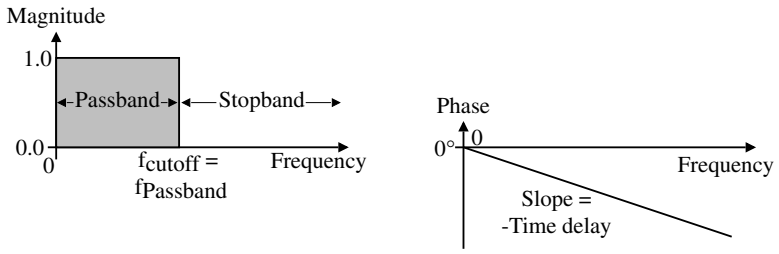
9.7 - SWITCHED CAPACITOR FILTERS

APPROACH

Today's switched capacitor filters are based on continuous time filters. Consequently, it is expedient to briefly review the subject of continuous time filters.

Filter Specifications → Continuous Time Filter → Switched Capacitor Filter

Ideal Filter:



This specification cannot be achieve by realizable filters because:

- An instantaneous transition from a gain of 1 to 0 is not possible.
- A band of zero gain is not possible.

Therefore, we develop *filter approximations* which closely approximate the ideal filter but are realizable.

CHARACTERIZATION OF FILTERS

A low pass filter magnitude response.

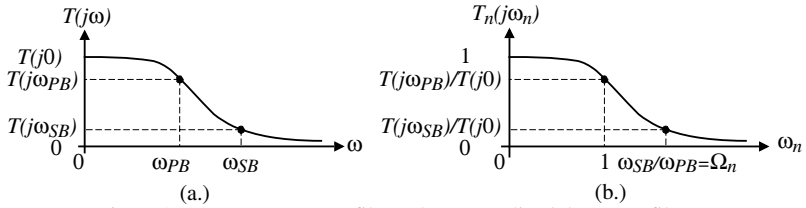


Figure 9.7-1 - (a.) Low pass filter. (b.) Normalized, low pass filter.

Three basic properties of filters.

1.) Passband ripple = $|T(j0) - T(j\omega_{PB})|$.

2.) Stopband frequency = ω_{SB}.

3.) Stopband gain/attenuation = $T(j\omega_{SB})$.

For a normalized filter the basic properties are:

1.) Passband ripple = $T(j\omega_{PB})/T(j0) = T(j\omega_{PB})$ if $T(j0) = 1$.

2.) Stopband frequency (called the transition frequency) = $\Omega_n = \omega_{SB}/\omega_{PB}$.

3.) Stopband gain = $T(j\omega_{SB})/T(j0) = T(j\omega_{SB})$ if $T(j0) = 1$.

FILTER SPECIFICATIONS IN TERMS OF BODE PLOTS (dB)

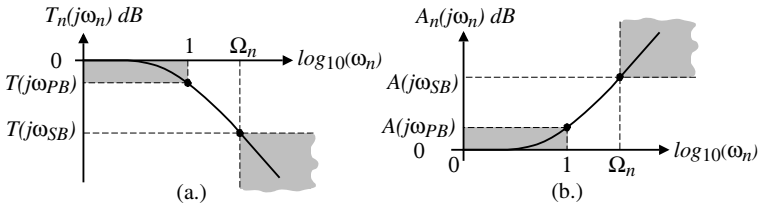


Figure 9.7-2 - (a.) Low pass filter of Fig. 9.7-1 as a Bode plot. (b.) Low pass filter of Fig. 9.7-2a shown in terms of attenuation *(A(jω) = 1/T(jω))*.

Therefore,

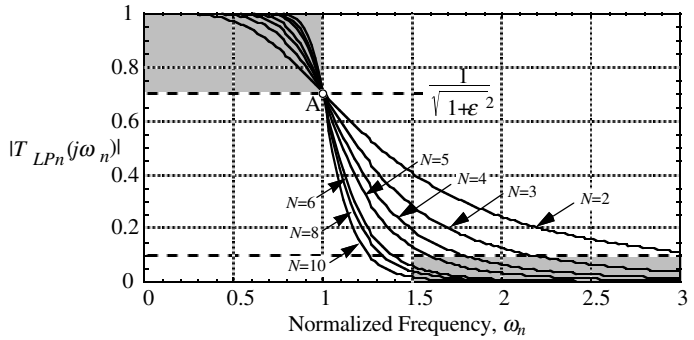
Passband ripple = $T(j\omega_{PB})$ dB

Stopband gain = $T(j\omega_{SB})$ dB or Stopband attenuation = $A(j\omega_{PB})$

Transition frequency is still = $\Omega_n = \omega_{SB}/\omega_{PB}$

BUTTERWORTH FILTER APPROXIMATION

This approximation is maximally flat in the passband.



Butterworth Magnitude Approximation:

$$\left|T_{LPn}(j\omega_n)\right| = \frac{1}{\sqrt{1 + \varepsilon^2\, \omega_n^{2N}}}$$

where N is the order of the approximation and ε is defined in the above plot.

The magnitude of the Butterworth filter approximation at ω_{SB} is given as

$$\left|T_{LPn}\left(\frac{j\omega_{SB}}{\omega_{PB}}\right)\right| = |T_{LPn}(j\Omega_n)| = T_{SB} = \frac{1}{\sqrt{1 + \varepsilon^2\, \Omega_n^{2N}}}$$

This equation in terms of dB is useful for finding N given the filter specifications.

$$20\, log_{10}(T_{SB}) = T_{SB}\,(dB) = -10\, log_{10}\left(1 + \varepsilon^2\, \Omega_n^{2N}\right)$$

EXAMPLE 9.7-1 - Determining the Order of A Butterworth Filter Approximation

Assume that a normalized, low-pass filter is specified as T_{PB} = -3dB, T_{SB} = -20 dB, and Ω_n = 1.5. Find the smallest integer value of N of the Butterworth filter approximation which will satisfy this specification.

Solution

T_{PB} = -3dB corresponds to T_{PB} = 0.707 which implies that ε = 1. Thus, substituting ε = 1 and Ω_n = 1.5 into the equation at the bottom of the previous slide gives

$$T_{SB}\,(dB) = -\,10\,log_{10}(\,1 + 1.5^{2N})$$

Substituting values of N into this equation gives,

T_{SB} = -7.83 dB for N = 2
-10.93 dB for N = 3
-14.25 dB for N = 4
-17.68 dB for N = 5
-21.16 dB for N = 6.

Thus, N must be 6 or greater to meet the filter specification.

POLES AND QUADRATIC FACTORS OF BUTTERWORTH FUNCTIONS

Table 9.7-1 - Pole locations and quadratic factors ($s_n^2 + a_1 s_n + 1$) of normalized, low pass Butterworth functions for ε = 1. Odd orders have a product (s_n+1).

N	Poles		a_1 coefficient	
2	-0.70711 ± j0.70711		1.41421	
3	-0.50000 ± j0.86603		1.00000	
4	-0.38268 ± j0.92388		0.76536	
	-0.92388 ± j0.38268		1.84776	
5	-0.30902 ± j0.95106		0.61804	
	-0.80902 ± j0.58779		1.61804	
6	-0.25882 ± j0.96593	-0.96593 ± j0.25882	0.51764	1.93186
	-0.70711 ± j0.70711		1.41421	
7	-0.22252 ± j0.97493	-0.90097 ± j0.43388	0.44505	1.80194
	-0.62349 ± j0.78183		1.24698	
8	-0.19509 ± j0.98079	-0.83147 ± j0.55557	0.39018	1.66294
	-0.55557 ± j0.83147	-0.98079 ± j0.19509	1.11114	1.96158
9	-0.17365 ± j0.98481	-0.76604 ± j0.64279	0.34730	1.53208
	-0.50000 ± j0.86603	-0.93969 ± j0.34202	1.00000	1.87938
10	-0.15643 ± j0.98769	-0.89101 ± j0.45399	0.31286	1.78202
	-0.45399 ± j0.89101	-0.98769 ± j0.15643	0.90798	1.97538
	-0.70711 ± j0.70711		1.41421	

Example 9.7-2 - Finding the Butterworth Roots and Polynomial for a given *N*

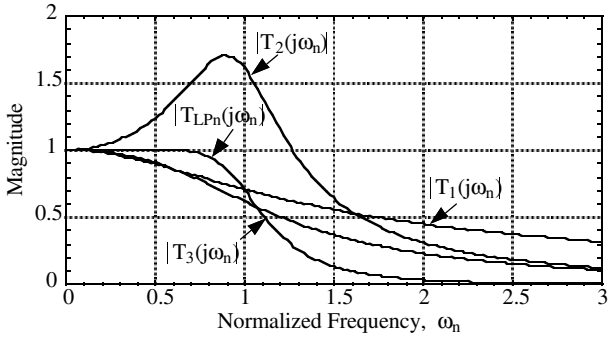
Find the roots for a Butterworth approximation with $\varepsilon = 1$ for $N = 5$.

Solution

For $N = 5$, the following first- and second-order products are obtained from Table 9.7-1

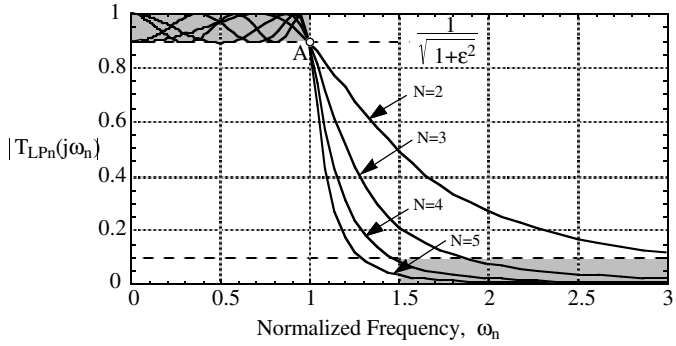
$$T_{LPn}(s_n) = T_1(s_n)T_2(s_n)T_3(s_n) = \left(\frac{1}{s_n+1}\right)\left(\frac{1}{s_n^2+0.6180s_n+1}\right)\left(\frac{1}{s_n^2+1.6180s_n+1}\right)$$

Illustration of the individual magnitude contributions of each product of $T_{LPn}(s_n)$.



CHEBYSHEV FILTER APPROXIMATION

The magnitude response of the Chebyshev filter approximation for ε = 0.5088.



The magnitude of the normalized, Chebyshev, low-pass, filter approximation can be expressed as

$$|T_{LPn}(j\omega_n)| = \frac{1}{\sqrt{1+\varepsilon^2\cos^2[N\cos^{-1}(\omega_n)]}} \quad , \quad \omega_n \le 1$$

and

$$|T_{LPn}(j\omega_n)| = \frac{1}{\sqrt{1+\varepsilon^2\cosh^2[N\cosh^{-1}(\omega_n)]}} \quad , \quad \omega_n > 1$$

where N is the order of the filter approximation and ε is defined as

$$|T_{LPn}(\omega_{PB})| = |T_{LPn}(1)| = T_{PB} = \frac{1}{\sqrt{1+\varepsilon^2}}.$$

N is determined from $\quad 20\log_{10}(T_{SB}) = T_{SB}(dB) = -10\log_{10}\{1+\varepsilon^2\cosh^2[N\cosh^{-1}(\Omega_n)]\}$

EXAMPLE 9.7-3 - Determining the Order of A Chebyshev Filter Approximation

Repeat Ex. 9.7-1 for the Chebyshev filter approximation.

Solution

In Ex. 9.7-2, $\varepsilon = 1$ which means the ripple width is 3 *dB* or $T_{PB} = 0.707$. Now we substitute $\varepsilon = 1$ into

$$20\,log_{10}(T_{SB}) = T_{SB}\,(dB) = -10log_{10}\{1 + \varepsilon^2 cosh^2[Ncosh^{-1}(\Omega_n)]\}$$

and find the value of N which satisfies $T_{SB} = -20dB$.

For $N = 2$, $\rightarrow T_{SB} = -11.22\ dB$.

For $N = 3$, $\rightarrow T_{SB} = -19.14\ dB$.

For $N = 4$, $\rightarrow T_{SB} = -27.43$ dB.

Thus $N = 4$ must be used although $N = 3$ almost satisfies the specifications. This result compares with $N = 6$ for the Butterworth approximation.

POLES AND QUADRATIC FACTORS OF CHEBYSHEV FUNCTIONS

Table 9.7-2 - Pole locations and quadratic factors ($a_0 + a_1 s_n + s_n^2$) of normalized, low pass Chebyshev functions for $\varepsilon = 0.5088$ (1*dB*).

N	Normalized Pole Locations	a_0	a_1
2	-0.54887 ± j0.89513	1.10251	1.09773
3	-0.24709 ± j0.96600 -0.49417	0.99420	0.49417
4	-0.13954 ± j0.98338 -0.33687 ± j0.40733	0.98650 0.27940	0.27907 0.67374
5	-0.08946 ± j0.99011 -0.23421 ± j0.61192 -0.28949	0.98831 0.42930	0.17892 0.46841
6	-0.06218 ± j0.99341 -0.16988 ± j0.72723 -0.23206 ± j0.26618	0.99073 0.55772 0.12471	0.12436 0.33976 0.46413
7	-0.04571 ± j0.99528 -0.12807 ± j0.79816 -0.18507 ± j0.44294 -0.20541	0.99268 0.65346 0.23045	0.09142 0.25615 0.37014

EXAMPLE 9.7-4 - Finding the Chebyshev Roots for a given *N*

Find the roots for the Chebyshev approximation with $\varepsilon = 1$ for $N = 5$.

Solution

For $N = 5$, we get the following quadratic factors which give the transfer function as

$$T_{LPn}(s_n) = T_1(s_n)T_2(s_n)T_3(s_n) = \left(\frac{0.2895}{s_n+0.2895}\right)\left(\frac{0.9883}{s_n^2+0.1789s_n+0.9883}\right)\left(\frac{0.4293}{s_n^2+0.4684s_n+0.4293}\right).$$

OTHER APPROXIMATIONS

Thomson Filters - Maximally flat magnitude and linear phase[1]

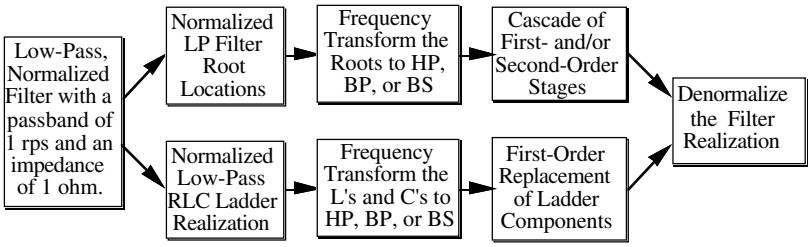
Elliptic Filters - Ripple both in the passband and stopband, the smallest transition region of all filters.[2]

An excellent collection of filter approximations and data is found in A.I. Zverev, *Handbook of Filter Synthesis*, John Wiley & Sons, Inc., New York, 1967.

[1] W.E. Thomson, "Delay Networks Having Maximally Flat Frequency Characteristics," *Proc. IEEE,* part 3, vol. 96, Nov. 1949, pp. 487-490.

[2] W. Cauer, *Synthesis of Linear Communication Networks*, McGraw-Hill Book Co., New York, NY, 1958.

GENERAL APPROACH FOR CONTINUOUS AND SC FILTER DESIGN



All designs start with a normalized, low pass filter with a passband of 1 radian/second and an impedance of 1Ω that will satisfy the filter specification.

1.) Cascade approach - starts with the normalized, low pass filter root locations.

2.) Ladder approach - starts with the normalized, low pass, *RLC* ladder realizations.

A DESIGN PROCEDURE FOR THE LOW PASS, SC FILTERS USING THE CASCADE APPROACH

1.) From T_{PB}, T_{SB}, and Ω_n (or A_{PB}, A_{SB}, and Ω_n) determine the required order of the filter approximation, N.

2.) From tables similar to Table 9.7-1 and 9.7-2 find the normalized poles of the approximation.

3.) Group the complex-conjugate poles into second-order realizations. For odd-order realizations there will be one first-order term.

4.) Realize each of the terms using the first- and second-order blocks of Secs. 9.5 and 9.6.

5.) Cascade the realizations in the order from input to output of the lowest-Q stage first (first-order stages generally should be first).

More information can be found elsewhere[1,2,3,4].

[1] K.R. Laker and W.M.C. Sansen, *Design of Analog Integrated Circuits and Systems*, McGraw Hill, New York, 1994.

[2] P.E. Allen and E. Sanchez-Sinencio, *Switched Capacitor Circuits*, Van Nostrand Reinhold, New York, 1984.

[3] R. Gregorian and G.C. Temes, *Analog MOS Integrated Circuits for Signal Processing*, John Wiley & Sons, New York, 1987.

[4] L.P. Huelsman and P.E. Allen, *Introduction to the Theory and Design of Active Filters*, McGraw Hill Book Company, New York, 1980.

EXAMPLE 9.7-5 - Fifth-order, Low Pass, Switched Capacitor Filter using the Cascade Approach

Design a cascade, switched capacitor realization for a Chebyshev filter approximation to the filter specifications of T_{PB} = -1dB, T_{SB} = -25dB, f_{PB} = 1kHz and f_{SB} = 1.5kHz. Give a schematic and component value for the realization. Also simulate the realization and compare to an ideal realization. Use a clock frequency of 20kHz.

Solution

First we see that Ω_n = 1.5. Next, recall that when T_{PB} = -1dB that this corresponds to ε = 0.5088. We find that N = 5 satisfies the specifications (T_{SB} = -29.9dB). Using the results of Ex. 9.7-4, we may write $T_{LPn}(s_n)$ as

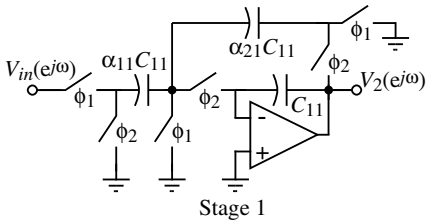
$$T_{LPn}(s_n) = \left(\frac{0.2895}{s_n+0.2895}\right)\left(\frac{0.9883}{s_n^2+0.1789s_n+0.9883}\right)\left(\frac{0.4293}{s_n^2+0.4684s_n+0.4293}\right). \quad (1)$$

Next, we design each of the three stages individually.

EXAMPLE 9.7-5 - Continued

Stage 1 - First-order Stage

Let us select Fig. 9.5-1 to realize the first-order stage. We will assume that f_c is much greater than f_{BP} (i.e. 100) and use Eq. (10) of Sec. 9.5 repeated below to accomplish the design.



$$T_1(s) \approx \frac{\alpha_{11}/\alpha_{21}}{1 + s(T/\alpha_{21})} \quad (2)$$

Note that we have used the second subscript 1 to denote the first stage. Before we can use this equation we must normalize the sT factor. This normalization is accomplished by

$$sT = \left(\frac{s}{\omega_{PB}}\right)\cdot(\omega_{PB}T) = s_nT_n\,. \quad (3)$$

Therefore, Eq. (2) can be written as

$$T_1(s_n) \approx \frac{\alpha_{11}/\alpha_{21}}{1 + s_n(T_n/\alpha_{21})} = \frac{\alpha_{11}/T_n}{s_n + \alpha_{21}/T_n} \quad (4)$$

where $\alpha_{11} = C_{11}/C$ and $\alpha_{21} = C_{21}/C$. Equating Eq. (4) to the first term in $T_{LPn}(s_n)$ gives the design of Fig. 9.5-1 as

$$\alpha_{21} = \alpha_{11} = 0.2895T_n = \frac{0.2895\cdot\omega_{PB}}{f_c} = \frac{0.2895\cdot 2000\pi}{20{,}000} = 0.0909$$

The sum of capacitances for the first stage is

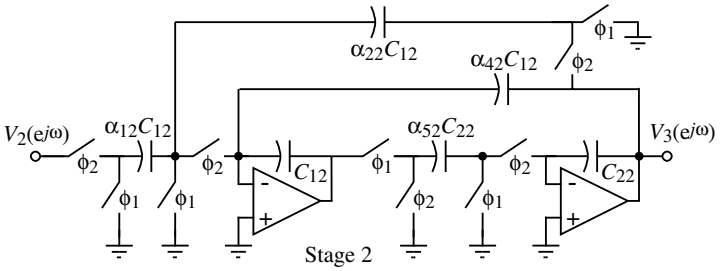
$$\text{First-stage capacitance} = 2 + \frac{1}{0.0909} = 13 \text{ units of capacitance}$$

EXAMPLE 9.7-5 - Continued

Stage 2 - Second-order, High-Q Stage

The next product of $T_{LPn}(s_n)$ is

$$\frac{0.9883}{s_n^2 + 0.1789s_n + 0.9883} = \frac{T(0)\omega_n^2}{s_n^2 + \frac{\omega_n}{Q}s_n + \omega_n^2} \quad (5)$$



where $T(0) = 1$, $\omega_n = 0.9941$ and $Q = (0.9941/0.1789) = 5.56$. Therefore, select the low pass version of the high-Q biquad of Fig. 9.6-7. First, apply the normalization of Eq. (3) to get

$$T_2(s_n) \approx \frac{-\left[\alpha_{62}s_n^2 + \frac{s_n\alpha_{32}\alpha_{52}}{T_n} + \frac{\alpha_{12}\alpha_{52}}{T_n^2}\right]}{s_n^2 + \frac{s_n\alpha_{42}\alpha_{52}}{T_n} + \frac{\alpha_{22}\alpha_{52}}{T_n^2}} \quad . \quad (6)$$

To get a low pass realization, select $\alpha_{32} = \alpha_{62} = 0$ to get

$$T_2(s_n) \approx \frac{-\frac{\alpha_{12}\alpha_{52}}{T_n^2}}{s_n^2 + \frac{s_n\alpha_{42}\alpha_{52}}{T_n} + \frac{\alpha_{22}\alpha_{52}}{T_n^2}} \quad . \quad (7)$$

EXAMPLE 9.7-5 - Continued

Equating Eq. (7) to the middle term of $T_{LPn}(s_n)$ gives

$$\alpha_{12}\alpha_{52} = \alpha_{22}\alpha_{52} = 0.9883T_n^2 = \frac{0.9883\cdot\omega_{PB}{}^2}{f_c^2} = \frac{0.9883\cdot 4\pi^2}{400} = 0.09754$$

and

$$\alpha_{42}\alpha_{52} = 0.1789T_n = \frac{0.1789\cdot\omega_{PB}}{f_c} = \frac{0.1789\cdot 2\pi}{20} = 0.05620$$

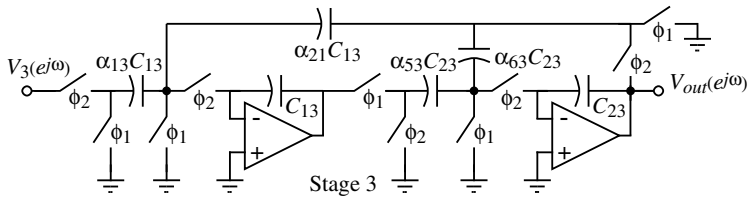
Choose $a_{12} = a_{22} = \alpha_{52}$ to get optimum voltage scaling. Thus we get, $\alpha_{12} = \alpha_{22} = \alpha_{52} = 0.3123$ and $\alpha_{42} = 0.05620/0.3123 = 0.1800$. The second-stage capacitance is

$$\text{Second-stage capacitance} = 1 + \frac{3(0.3123)}{0.1800} + \frac{2}{0.1800} = 17.316 \text{ units of capacitance}$$

Stage 3 - Second-order, Low-Q Stage

The last product of $T_{LPn}(s_n)$ is

$$\frac{0.4293}{s_n^2 + 0.4684s_n + 0.4293} = \frac{T(0)\omega_n^2}{s_n^2 + \frac{\omega_n}{Q}s_n + \omega_n^2} \quad (8)$$



where we see that $T(0) = 1$, $\omega_n = 0.6552$ and $Q = (0.6552/0.4684) = 1.3988$. Therefore, select the low pass version of the low-Q biquad. First, apply the normalization of Eq. (3) to get

EXAMPLE 9.7-5 - Continued

$$T_3(s_n) \approx \frac{-\left[\alpha_{33}s_n^2 + \frac{s_n\alpha_{43}}{T_n} + \frac{\alpha_{13}\alpha_{53}}{T_n^2}\right]}{s_n^2 + \frac{s_n\alpha_{63}}{T_n} + \frac{\alpha_{23}\alpha_{53}}{T_n^2}} \quad . \tag{9}$$

To get a low pass realization, select $\alpha_{33} = \alpha_{43} = 0$ to get

$$T_3(s_n) \approx \frac{-\frac{\alpha_{13}\alpha_{53}}{T_n^2}}{s_n^2 + \frac{s_n\alpha_{63}}{T_n} + \frac{\alpha_{23}\alpha_{53}}{T_n^2}} \quad . \tag{10}$$

Equating Eq. (10) to the last term of $T_{LPn}(s_n)$ gives

$$\alpha_{13}\alpha_{53} = \alpha_{23}\alpha_{53} = 0.4293T_n^2 = \frac{0.4293\cdot\omega_{PB}{}^2}{f_c^2} = \frac{0.4293\cdot 4\pi^2}{400} = 0.04237$$

and

$$\alpha_{63} = 0.4684T_n = \frac{0.4684\cdot\omega_{PB}}{f_c} = \frac{0.4684\cdot 2\pi}{20} = 0.1472$$

Choose $a_{13} = a_{23} = \alpha_{53}$ to get optimum voltage scaling. Thus , $\alpha_{13} = \alpha_{23} = \alpha_{53} = 0.2058$ and $\alpha_{63} = 0.1472$. The third-stage capacitance is

$$\text{Third-stage capacitance} = 1 + \frac{3(0.2058)}{0.1472} + \frac{2}{0.1472} = 18.78 \text{ units of capacitance}$$

The total capacitance of this design is 13 + 17.32 + 18.78 = 49.10 units of capacitance.

EXAMPLE 9.7-5 - Continued

Final design with stage 3 second to maximize the dynamic range.

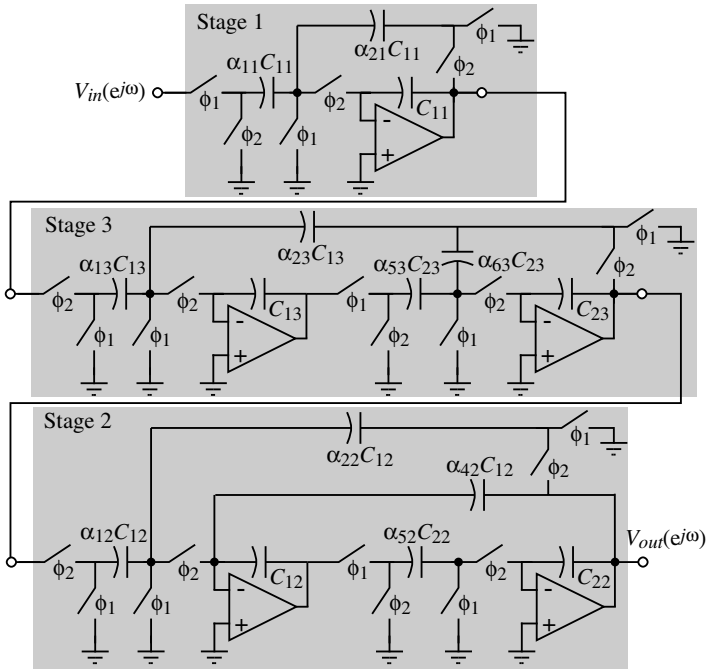


Figure 9.7-7 - Fifth-order, Chebyshev, low pass, switched capacitor filter of Example 9.7-5.

EXAMPLE 9.7-5 - Continued

Simulated Frequency Response:

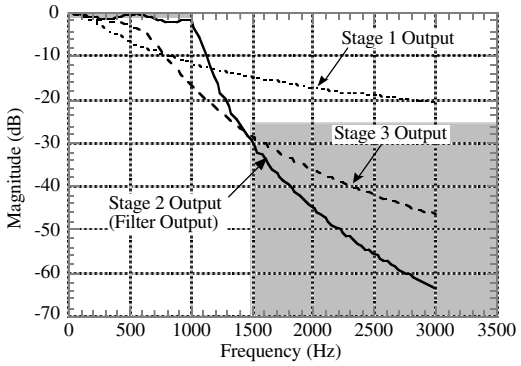


Figure 9.7-8a - Simulated magnitude response of Ex. 9.7-5

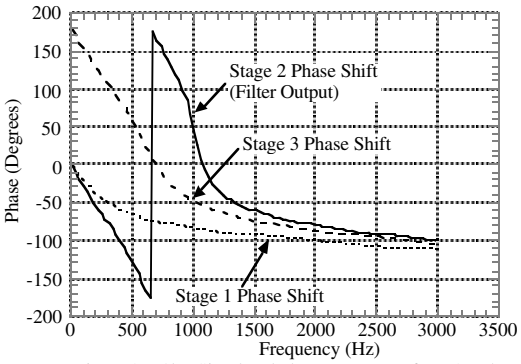


Figure 9.7-8b - Simulated phase response of Ex. 9.7-5

Comments:

- There appears to be a sinx/x effect on the magnitude which causes the passband specification to not be satisfied. This can be avoided by prewarping the specifications before designing the filter.
- Stopband specifications met
- None of the outputs of the biquads exceeds 0 dB (Need to check internal biquad nodes)

EXAMPLE 9.7-5 - Continued

SPICE Input File:

```
******** 08/29/97 13:17:44 *********
*******PSpice 5.2 (Jul 1992) ********

*SPICE FILE FOR EXAMPLE 9.7-5
*EXAMPLE 9-7-5: nodes 5 is the output
*of 1st stage, node 13 : second stage (in
*the figure it is second while in design it
*is third, low Q stage), and node 21 is the
*final output of the *filter.

**** CIRCUIT DESCRIPTION ****

VIN    1 0 DC 0 AC 1

*.PARAM CNC=1 CNC_1=1 CPC_1=1

XNC1    1 2 3 4 NC1
XUSCP1    3 4 5 6 USCP
XPC1    5 6 3 4 PC1
XAMP1    3 4 5 6 AMP

XPC2    5 6 7 8 PC2
XUSCP2    7 8 9 10 USCP
XAMP2    7 8 9 10 AMP
XNC3    9 10 11 12 NC3
XAMP3    11 12 13 14 AMP
XUSCP3    11 12 13 14 USCP
XPC4    13 14 11 12 PC4
XPC5    13 14 7 8 PC2

XPC6    13 14 15 16 PC6
XAMP4    15 16 17 18 AMP
XUSCP4    15 16 17 18 USCP
XNC7    17 18 19 20 NC7
XAMP5    19 20 21 22 AMP
XUSCP5 19 20 21 22 USCP
XUSCP6    21 22 15 16 USCP1
XPC8    21 22 15 16 PC6

.SUBCKT DELAY 1 2 3
ED    4 0 1 2 1
TD    4 0 3 0 ZO=1K TD=25US
RDO    3 0 1K
.ENDS DELAY

.SUBCKT NC1 1 2 3 4
RNC1    1 0 11.0011
XNC1    1 0 10 DELAY
GNC1    1 0 10 0 0.0909
XNC2    1 4 14 DELAY
GNC2    4 1 14 0 0.0909
XNC3    4 0 40 DELAY
GNC3    4 0 40 0 0.0909
RNC2    4 0 11.0011
.ENDS NC1

.SUBCKT NC3 1 2 3 4
RNC1    1 0 4.8581
XNC1    1 0 10 DELAY
GNC1    1 0 10 0 0.2058
XNC2    1 4 14 DELAY
GNC2    4 1 14 0 0.2058
XNC3    4 0 40 DELAY
GNC3    4 0 40 0 0.2058
RNC2    4 0 4.8581
Ends NC3
```


EXAMPLE 9.7-5 - Continued

Spice Input File - Continued

```
.SUBCKT NC7 1 2 3 4
RNC1    1 0 3.2018
XNC1    1 0 10 DELAY
GNC1    1 0 10 0 0.3123
XNC2    1 4 14 DELAY
GNC2    4 1 14 0 0.3123
XNC3    4 0 40 DELAY
GNC3    4 0 40 0 0.3123
RNC2    4 0 3.2018
.ENDS NC7

.SUBCKT PC1 1 2 3 4
RPC1    2 4 11.0011
.ENDS PC1

.SUBCKT PC2 1 2 3 4
RPC1    2 4 4.8581
.ENDS PC2

.SUBCKT PC4 1 2 3 4
RPC1    2 4 6.7980
.ENDS PC4

.SUBCKT PC6 1 2 3 4
RPC1    2 4 3.2018
.ENDS PC6

.SUBCKT USCP 1 2 3 4
R1    1 3 1
R2    2 4 1
XUSC1    1 2 12 DELAY
GUSC1    1 2 12 0 1
XUSC2    1 4 14 DELAY
GUSC2    4 1 14 0 1
XUSC3    3 2 32 DELAY
GUSC3    2 3 32 0 1
XUSC4    3 4 34 DELAY
GUSC4    3 4 34 0 1
.ENDS USCP

.SUBCKT USCP1 1 2 3 4
R1    1 3 5.5586
R2    2 4 5.5586
XUSC1    1 2 12 DELAY
GUSC1    1 2 12 0 0.1799
XUSC2    1 4 14 DELAY
GUSC2    4 1 14 0 .1799
XUSC3    3 2 32 DELAY
GUSC3    2 3 32 0 .1799
XUSC4    3 4 34 DELAY
GUSC4    3 4 34 0 .1799
.ENDS USCP1


.SUBCKT AMP 1 2 3 4
EODD    3 0 1 0 1E6
EVEN    4 0 2 0 1E6
.ENDS AMP

.AC LIN 100 10 3K
.PRINT AC V(5) VP(5) V(13) VP(13)
V(21) VP(21)
.PROBE
.END
```

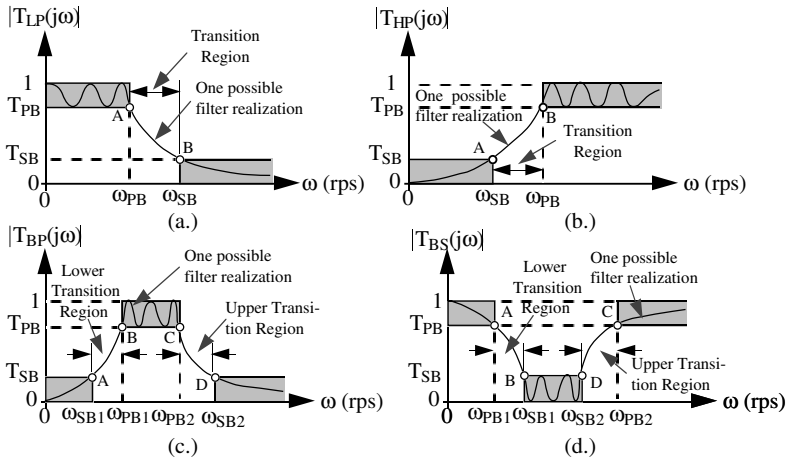

EXAMPLE 9.7-5 - Continued

Switcap2 Input File (The exact same results were obtained as for SPICE)

```
TITLE: EXAMPLE 9-7-5

OPTIONS;
 NOLIST;
 GRID;
 END;

TIMING;
 PERIOD 50E-6;
 CLOCK CLK 1 (0 25/50);
 END;

SUBCKT (1 100) STG1;
 S1        (1 2)        CLK;
 S2        (2 0)        #CLK;
 S3        (3 4)        #CLK;
 S4        (3 0)        CLK;
 S5        (5 100)      #CLK;
 S6        (5 0)        CLK;
 CL11      (2 3)        0.0909;
 CL21      (3 5)        0.0909;
 E1        (100 0 0 4)  1E6;
 END;

SUBCKT (200 300) STG2;
 S1        (200 2)      #CLK;
 S2        (2 0)        CLK;
 S3        (3 0)        CLK;
 S4        (3 4)        #CLK;
 S5        (6 5)        CLK;
 S6        (6 0)        #CLK;
 S7        (7 0)        CLK;
 S8        (7 8)        #CLK;
 S9        (300 9)      #CLK;
 S10       (9 0)        #CLK;
 CL12      (2 3)        0.3123;
 CL22      (3 9)        0.3123;
 CL42      (4 300)      0.1799;
 C12       (4 5)        1;
 CL52      (6 7)        0.3123;
 C22       (8 300)      1;
 E1        (5 0 0 4)    1E6;
 E2        (300 0 0 8)  1E6
 END;

SUBCKT (100 200) STG3;
 S1        (100 2)      #CLK;
 S2        (2 0)        CLK;
 S3        (3 0)        CLK;
 S4        (3 4)        #CLK;
 S5        (6 5)        CLK;
 S6        (6 0)        #CLK;
 S7        (7 0)        CLK;
 S8        (7 8)        #CLK;
 S9        (200 9)      #CLK;
 S10       (9 0)        #CLK;
 CL13      (2 3)        0.2058;
 CL23      (3 9)        0.2058;
 CL63      (9 7)        0.1471;
 C13       (4 5)        1;
 CL53      (6 7)        0.2058;
 C23       (8 200)      1;
 E1        (5 0 0 4)    1E6;
 E2        (200 0 0 8)  1E6
 END;

CIRCUIT;
 X1        (1 100)      STG1;
 X2        (100 200)    STG3;
 X3        (200 300)    STG2;
 V1        (2 0);
 END;

ANALYZE SSS;
 INFREQ  1  3000  LIN  150;
 SET V1 AC 1.0 0.0;
 PRINT vdb(100) vp(100);
 PRINT vdb(200) vp(200);
 PRINT vdb(300) vp(300);
 PLOT vdb(300);
 END;

END;
```

USING THE CASCADE APPROACH FOR OTHER TYPES OF FILTERS

Other types of filters are developed based on the low pass approach.



Practical magnitude responses of (a.) low pass, (b.) high pass, (c.) bandpass, and (d.) bandstop filter.

We will use transformations from the normalized, low pass filter to the normalized high pass, bandpass or bandstop to achieve other types of filters.

HIGH PASS, SC FILTERS USING THE CASCADE APPROACH

Normalized, low pass to normalized high pass transformation:

$$s_{ln} = \frac{1}{s_{hn}}$$

where s_{hn} is the normalized, high-pass frequency variable.

A general form of the normalized, low-pass transfer function is

$$T_{LPn}(s_{ln}) = \frac{p_{1ln}p_{2ln}p_{3ln}\cdots p_{Nln}}{(s_{ln}+p_{1ln})(s_{ln}+p_{2ln})(s_{ln}+p_{3ln})\cdots(s_{ln}+p_{Nln})}$$

where p_{kln} is the kth normalized, low-pass pole.

Applying the normalized, low-pass to high-pass transformation to$T_{LPn}(s_{ln})$ gives

$$T_{HPn}(s_{hn}) = \frac{p_{1ln}p_{2ln}p_{3ln}\cdots p_{Nln}}{\left(\frac{1}{s_{hn}}+p_{1ln}\right)\left(\frac{1}{s_{hn}}+p_{2ln}\right)\left(\frac{1}{s_{hn}}+p_{3ln}\right)\cdots\left(\frac{1}{s_{hn}}+p_{Nln}\right)} = \frac{s_{hn}^N}{\left(s_{hn}+\frac{1}{p_{1ln}}\right)\left(s_{hn}+\frac{1}{p_{2ln}}\right)\left(s_{hn}+\frac{1}{p_{3ln}}\right)\cdots\left(s_{hn}+\frac{1}{p_{Nln}}\right)}$$

$$= \frac{s_{hn}^N}{(s_{hn}+p_{1hn})(s_{hn}+p_{2hn})(s_{hn}+p_{3hn})\cdots(s_{hn}+p_{Nhn})}$$

where p_{khn} is the kth normalized high-pass pole.

Use the high pass switched capacitor circuits of Secs. 9.5 and 9.6 to achieve the implementation.

Ω_n is defined for the high pass normalized filter as: $\Omega_n = \frac{1}{\Omega_{hn}} = \frac{\omega_{PB}}{\omega_{SB}}$

EXAMPLE 9.7-7 - Design of a Butterworth, High-Pass Filter

Design a high-pass filter having a -3dB ripple bandwidth above 1 kHz and a gain of less than -35 dB below 500 Hz using the Butterworth approximation. Use a clock frequency of 100kHz.

Solution

From the specification, we know that T_{PB} = -3 dB and T_{SB} = -35 dB. Also, $\Omega_n = 2$ ($\Omega_{hn} = 0.5$). $\varepsilon = 1$ because T_{PB} = -3 dB. Therefore, find that $N = 6$ will give T_{SB} = -36.12 dB which is the lowest, integer value of N which meets the specifications.

Next, the normalized, low-pass poles are found from Table 9.7-1 as

$$p_{1ln}, p_{6ln} = -0.2588 \pm j\,0.9659$$

$$p_{2ln}, p_{5ln} = -0.7071 \pm j\,0.7071$$

and

$$p_{3ln}, p_{4ln} = -0.9659 \pm j\,0.2588$$

Inverting the normalized, low-pass poles gives the normalized, high-pass poles which are

$$p_{1hn}, p_{6hn} = -0.2588 \mp j\,0.9659$$

$$p_{2hn}, p_{5hn} = -0.7071 \mp j\,0.7071$$

and

$$p_{3hn}, p_{4hn} = -0.9659 \mp j\,0.2588 \quad .$$

We note the inversion of the Butterworth poles simply changes the sign of the imaginary part of the pole.

EXAMPLE 9.7-7 - Continued

The next step is to group the poles in second-order products, since there are no first-order products. This result gives the following normalized, high-pass transfer function.

$$T_{HPn}(s_{hn}) = T_1(s_{hn})T_2(s_{hn})T_3(s_{hn}) = \left(\frac{s_{hn}^2}{(s_{hn}+p_{1hn})(s_{hn}+p_{6hn})}\right)\left(\frac{s_{hn}^2}{(s_{hn}+p_{2hn})(s_{hn}+p_{5hn})}\right)\left(\frac{s_{hn}^2}{(s_{hn}+p_{3hn})(s_{hn}+p_{4hn})}\right)$$

$$= \left(\frac{s_{hn}^2}{s_{hn}^2+0.5176s_{hn}+1}\right)\left(\frac{s_{hn}^2}{s_{hn}^2+1.4141s_{hn}+1}\right)\left(\frac{s_{hn}^2}{s_{hn}^2+1.9318s_{hn}+1}\right) \quad .$$

Now we are in a position to do the stage-by-stage design. We see that the Q's of each stage are $Q_1 = 1/0.5176 = 1.932$, $Q_2 = 1/1.414 = 0.707$, and $Q_3 = 1/1.9318 = 0.5176$. Therefore, we will choose the low-Q biquad to implement the realization of this example.

The low-Q biquad design equations are:

$$\alpha_1 = \frac{K_0 T_n}{\omega_{on}},\ \alpha_2 = |\alpha_5| = \omega_{on}T_n,\ \alpha_3 = K_2,\ \alpha_4 = K_1 T_n,\ \text{and}\ \alpha_6 = \frac{\omega_{on}T_n}{Q} \quad .$$

For the high pass,

$K_0 = K_1 = 0$ and $K_2 = 1$, so that $\alpha_1 = \alpha_4 = 0$ and $\alpha_2 = |\alpha_5| = \omega_{on}T_n$, $\alpha_3 = K_2$ and $\alpha_6 = \dfrac{\omega_{on}T_n}{Q}$.

Stage 1

$$\alpha_{21} = \alpha_{51} = \frac{\omega_{PB}}{f_c} = \frac{2\pi\cdot 10^3}{10^5} = 0.06283,\ \ \alpha_{31} = 1,\ \text{and}\ \alpha_{61} = \frac{\omega_{PB}}{Qf_c} = \frac{0.06283}{1.932} = 0.03252$$

EXAMPLE 9.7-7 - Continued

Stage 2

$$\alpha_{22} = \alpha_{52} = \frac{\omega_{PB}}{f_c} = \frac{2\pi \cdot 10^3}{10^5} = 0.06283,$$

$\alpha_{32} = 1$, and

$$\alpha_{62} = \frac{\omega_{PB}}{Qf_c} = \frac{0.06283}{0.707} = 0.08884$$

Stage 3

$$\alpha_{23} = \alpha_{53} = \frac{\omega_{PB}}{f_c} = \frac{2\pi \cdot 10^3}{10^5} = 0.06283,$$

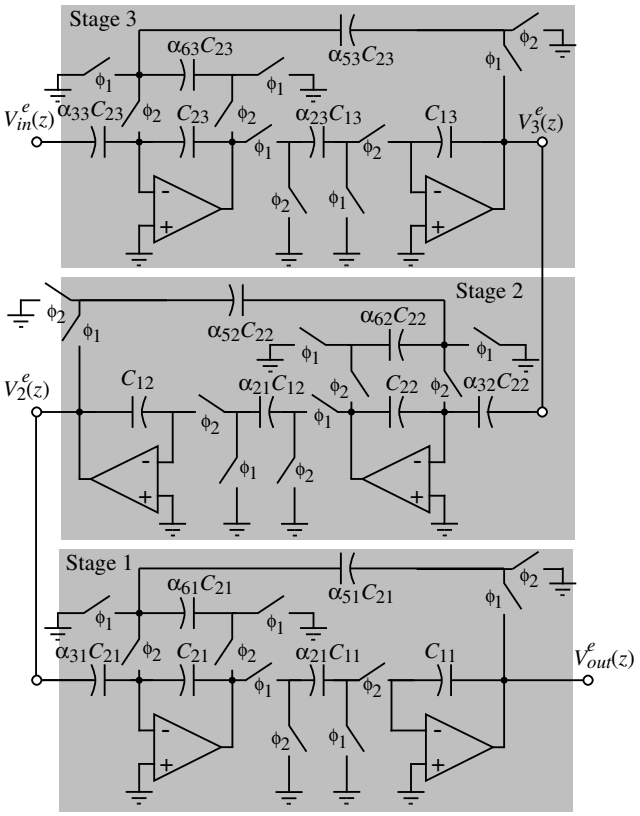
$\alpha_{33} = 1$, and

$$\alpha_{63} = \frac{\omega_{PB}}{Qf_c} = \frac{0.06283}{0.5176} = 0.1214$$

Realization $\rightarrow$

Lowest Q stages are first in the cascade realization.

Σ capacitances = 104.62 units of capacitance



BANDPASS, SC FILTERS USING THE CASCADE APPROACH

1.) Define the passband and stopband as

$$BW = \omega_{PB2} - \omega_{PB1} \qquad \text{and} \qquad SW = \omega_{SB2} - \omega_{SB1}$$

where ω_{PB2} is the larger passband frequency and ω_{PB1} is the smaller passband frequency of the bandpass filter. ω_{SB2} is the larger stopband frequency and ω_{SB1} is the smaller stopband frequency.

2.) Geometrically centered bandpass filters have the following relationship:

$$\omega_r = \sqrt{\omega_{PB1}\omega_{PB2}} \quad = \sqrt{\omega_{SB2}\omega_{SB1}}$$

3.) Define a normalized low-pass to unnormalized bandpass transformation as

$$s_{ln} = \frac{1}{BW}\left(\frac{s_b^2 + \omega_r^2}{s_b}\right) = \frac{1}{BW}\left(s_b + \frac{\omega_r^2}{s_b}\right).$$

4.) A *normalized low-pass to normalized bandpass transformation* is achieved by dividing the bandpass variable, s_b, by the geometric center frequency, ω_r, to get

$$s_{ln} = \left(\frac{\omega_r}{BW}\right)\left(\frac{s_b}{\omega_r} + \frac{1}{(s_b/\omega_r)}\right) = \left(\frac{\omega_r}{BW}\right)\left(s_{bn} + \frac{1}{s_{bn}}\right) \qquad \text{where} \qquad s_{bn} = \frac{s_b}{\omega_r} \ .$$

5.) Multiply by BW/ω_r and define yet a further normalization of the low-pass, complex frequency variable as

$$s_{ln}' = \left(\frac{BW}{\omega_r}\right) s_{ln} = \Omega_b s_{ln} = \Omega_b\left(\frac{s_l}{\omega_{PB}}\right) = \left(s_{bn} + \frac{1}{s_{bn}}\right) \qquad \text{where } \Omega_b = \frac{BW}{\omega_r} \ .$$

6.) Solve for s_{bn} in terms of s_{ln}' from the following quadratic equation.

$$s_{bn}^2 - s_{ln}' \, s_{bn} + 1 = 0 \qquad \rightarrow \qquad s_{bn} = \left(\frac{s_{ln}'}{2}\right) \pm \sqrt{\left(\frac{s_{ln}'}{2}\right)^2 - 1} \ .$$

ILLUSTRATION OF THE ABOVE APPROACH

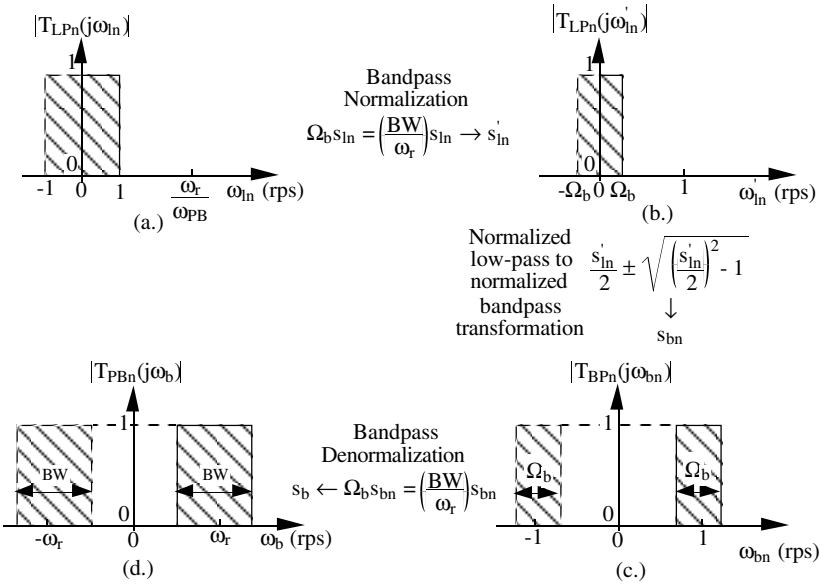


Figure 9.7-10 - Illustration of the development of a bandpass filter from a low-pass filter. (a.) Ideal normalized, low-pass filter. (b.) Normalization of (a.) for bandpass transformation. (c.) Application of low-pass to bandpass transformation. (d.) Denormalized bandpass filter.

BANDPASS DESIGN PROCEDURE FOR THE CASCADE APPROACH

1.) The ratio of the stop bandwidth to the pass bandwidth for the bandpass filter is defined as

$$\Omega_n = \frac{SW}{BW} = \frac{\omega_{SB2} - \omega_{SB1}}{\omega_{PB2} - \omega_{PB1}}.$$

2.) From T_{PB}, T_{SB}, and Ω_n, find the order N or the filter.

3.) Find the normalized, low-pass poles, p'_{kln}.

4.) The normalized bandpass poles can be found from the normalized, low pass poles, p'_{kln} using

$$p_{kbn} = \frac{p'_{kln}}{2} \pm \sqrt{\left(\frac{p'_{kln}}{2}\right)^2 - 1}\ .$$

For each pole of the low-pass filter, two poles result for the bandpass filter.

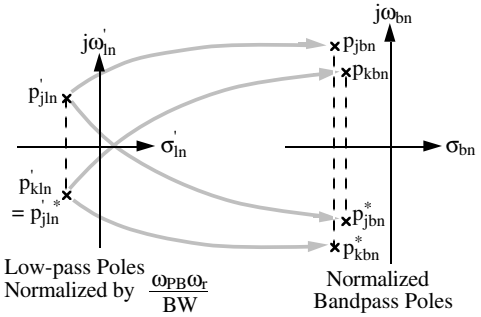


Figure 9.7-11 - Illustration of how the normalized, low-pass, complex conjugate poles are transformed into two normalized, bandpass, complex conjugate poles.

BANDPASS DESIGN PROCEDURE FOR THE CASCADE APPROACH - Continued

5.) Group the poles and zeros into second-order products having the following form

$$T_k(s_{bn}) = \frac{K_k\, s_{bn}}{(s_{bn} + p_{kbn})(s_{bn} + p^*_{jbn})} = \frac{K_k\, s_{bn}}{(s_{bn}+\sigma_{kbn}+j\omega_{kbn})(s_{bn}+\sigma_{kbn}-j\omega_{kbn})}$$

$$= \frac{K_k\, s_{bn}}{s^2_{bn}+(2\sigma_{kbn})s_{bn}+(\sigma^2_{bn}+\omega^2_{kbn})} = \frac{T_k(\omega_{kon})\left(\frac{\omega_{kon}}{Q_k}\right)s_{bn}}{s^2_{bn} + \left(\frac{\omega_{kon}}{Q_k}\right)s_{bn} + \omega^2_{kon}}$$

where j and k corresponds to the jth and kth low-pass poles which are a complex conjugate pair, K_k is a gain constant, and

$$\omega_{kon} = \sqrt{\sigma^2_{kbn}+\omega^2_{kbn}} \qquad \text{and} \qquad Q_k = \frac{\sqrt{\sigma^2_{bn}+\omega^2_{kbn}}}{2\sigma_{bn}} \quad .$$

6.) Realize each second-order product with a bandpass switched capacitor biquad and cascade in the order of increasing Q.

EXAMPLE 9.7-8 - Design of a Cascade Bandpass Switched Capacitor Filter

Design a bandpass, Butterworth filter having a -3dB ripple bandwidth of 200 Hz geometrically centered at 1 kHz and a stopband of 1 kHz with an attenuation of 40 dB or greater, geometrically centered at 1 kHz. The gain at 1 kHz is to be unity. Use a clock frequency of 100kHz.

Solution

From the specifications, we know that T_{PB} = -3 dB and T_{SB} = -40 dB. Also, $\Omega_n = 1000/200 = 5$. $\varepsilon = 1$ because T_{PB} = -3 dB. Therefore, we find that N = 3 will give T_{SB} = -41.94 dB which is the lowest, integer value of N which meets the specifications.

Next, we evaluate the normalized, low-pass poles from Table 9.7-1 as

$$p_{1ln}, p_{3ln} = -0.5000 \pm j0.8660 \quad \text{and} \quad p_{2ln} = -1.0000 \ .$$

Normalizing these poles by the bandpass normalization of $\Omega_b = 200/1000 = 0.2$ gives

$$p'_{1ln}, p'_{3ln} = -0.1000 \pm j\,0.1732 \quad \text{and} \quad p'_{2ln} = -0.2000 \ .$$

Each one of the p'_{kln} will contribute a second-order term. The normalized bandpass poles are found by using $s_{bn} = \left(s'_{ln}/2\right) \pm \sqrt{\left(s'_{ln}/2\right)^2 - 1}$ which results in 6 poles given as follows.

For p'_{1ln} = -0.1000 + j0.1732 → p_{1bn}, p_{2bn} = -0.0543 + j1.0891, -0.0457 - j0.9159.

For p'_{3ln} = -0.1000 - j0.1732 → p_{3bn}, p_{4bn} = -0.0457 + j0.9159, -0.543 - j 1.0891.

For p'_{2ln} = -0.2000 → p_{5bn}, p_{6bn} = -0.1000 ± j 0.9950.

EXAMPLE 9.7-8 - Continued

The normalized low-pass pole locations, p_{kln}, the bandpass normalized, low-pass pole locations, p'_{kln}, and the normalized bandpass poles, p_{kbn} are shown below. Note that the bandpass poles have very high pole-Qs if BW < ω_r.

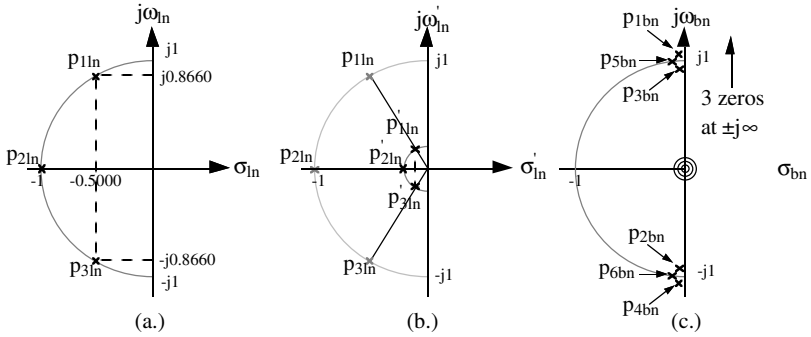


Figure 2-16 - Pole locations for Ex. 9.7-8. (a.) Normalized low-pass poles. (b.) Bandpass normalized low-pass poles. (c.) Normalized bandpass poles.

Grouping the complex conjugate bandpass poles gives the following second-order transfer functions.

$$T_1(s_{bn}) = \frac{K_1 s_{bn}}{(s+p_{1bn})(s+p_{4bn})} = \frac{K_1 s_{bn}}{(s_{bn}+0.0543+j1.0891)(s_{bn}+0.0543-j1.0891)} = \frac{\left(\frac{1.0904}{10.0410}\right)s_{bn}}{s_{bn}^2+\left(\frac{1.0904}{10.0410}\right)s_{bn}+1.0904^2} .$$

EXAMPLE 9.7-8 - Continued

$$T_2(s_{bn}) = \frac{K_2 s_{bn}}{(s+p_{2bn})(s+p_{3bn})} = \frac{K_2 s_{bn}}{(s_{bn}+0.0457+j0.9159)(s_{bn}+0.0457-j0.9159)} = \frac{\left(\frac{0.9170}{10.0333}\right)s_{bn}}{s_{bn}^2+\left(\frac{0.9170}{10.0333}\right)s_{bn}+0.9159^2} .$$

and

$$T_3(s_{bn}) = \frac{K_3 s_{bn}}{(s+p_{5bn})(s+p_{6bn})} = \frac{K_3 s_{bn}}{(s_{bn}+0.1000+j0.9950)(s_{bn}+0.1000-j0.9950)} = \frac{\left(\frac{1.0000}{5.0000}\right)s_{bn}}{s_{bn}^2+\left(\frac{1.0000}{5.0000}\right)s_{bn}+1.0000^2} .$$

Now we can begin the stage-by-stage design. Note that the Q's of the stages are $Q_1 = 10.0410$, $Q_2 = 10.0333$, and $Q_3 = 5.0000$. Therefore, use the high-Q biquad whose design equations are:

$$\alpha_1 = \frac{K_0 T_n}{\omega_{on}}, \quad \alpha_2 = |\alpha_5| = \omega_{on} T_n , \quad \alpha_3 = \frac{K_1}{\omega_{on}}, \quad \alpha_4 = \frac{1}{Q}, \text{ and } \quad \alpha_6 = K_2 .$$

For the bandpass realization $K_0 = K_2 = 0$ and $K_1 = \omega_{on}/Q$, so that the design equations simplify to

$$\alpha_1 = 0, \quad \alpha_2 = |\alpha_5| = \omega_{on}, T_n = \frac{\omega_{on}\cdot\omega_r}{f_c}, \quad \alpha_3 = \frac{K_1}{\omega_{on}} = \frac{\omega_{on}/Q}{\omega_{on}} = \frac{1}{Q}, \quad \alpha_4 = \frac{1}{Q}, \text{ and } \quad \alpha_6 = 0 .$$

<u>Stage 1</u>

$$\alpha_{11} = \alpha_{61} = 0, \ \alpha_{21} = |\alpha_{51}| = \frac{\omega_{o1}}{f_c} = \frac{1.0904\cdot 2\pi \text{x} 10^3}{10^5} = 0.06815, \ \alpha_{31} = 0.09959, \text{ and } \alpha_{41} = 0.09959$$

EXAMPLE 9.7-8 - Continued

Stage 2

$\alpha_{12} = \alpha_{62} = 0,$

$$\alpha_{22} = |\alpha_{52}| = \frac{\omega_{o2}}{f_c} = \frac{0.9159 \cdot 2\pi \text{x} 10^3}{10^5}$$

$$= 0.05755,$$

$\alpha_{32} = 0.09967$, and $\alpha_{42} = 0.09967$

Stage 3

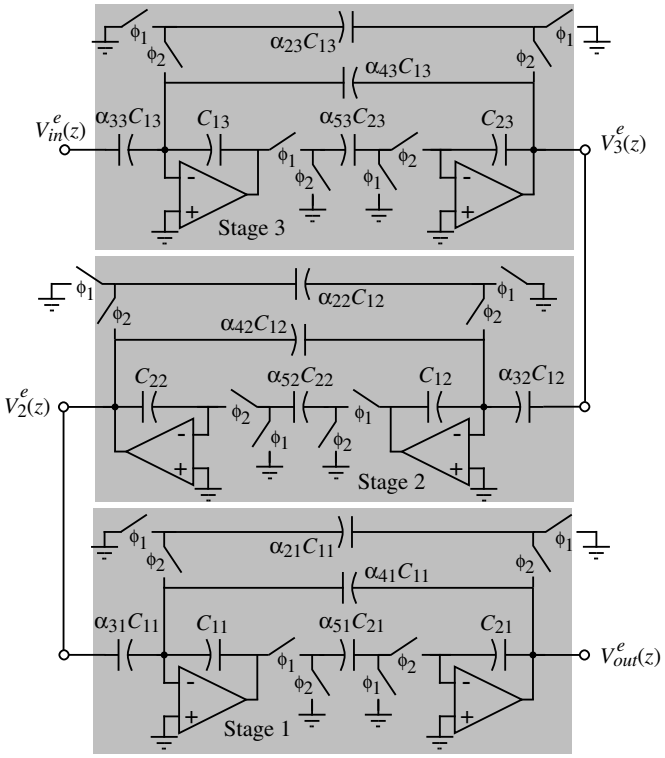
$\alpha_{13} = \alpha_{63} = 0,$

$$\alpha_{23} = |\alpha_{53}| = \frac{\omega_{o3}}{f_c} = \frac{1.0000 \cdot 2\pi \text{x} 10^3}{10^5}$$

$$= 0.06283,$$

$\alpha_{31} = 0.2000$, and $\alpha_{41} = 0.2000$

Realization →



HIGHER ORDER SWITCHED CAPACITOR FILTERS - LADDER APPROACH

The ladder approach to filter design starts from *RLC* realizations of the desired filter specification. These *RLC* realizations are called *prototype circuits*.

Advantage:

- Less sensitive to capacitor ratios.

Disadvantage:

- Design approach more complex
- Requires a prototype realization

Singly-terminated *RLC* prototype filters:

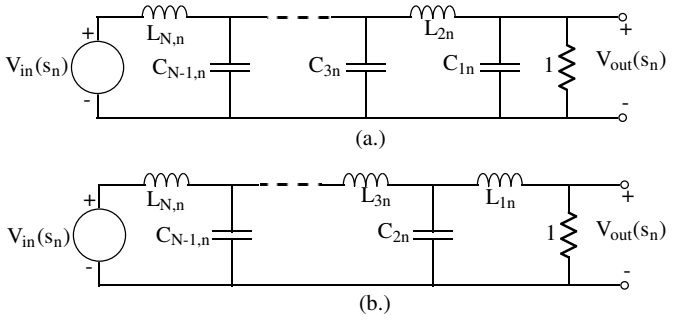


Figure 9.7-12 - Singly-terminated, *RLC* prototype filters. (a.) *N* even. (b.) *N* odd.

TABLE 9.7-3 - Normalized component values for Fig. 9.7-12 for the Butterworth and Chebyshev singly-terminated, *RLC* filter approximations.

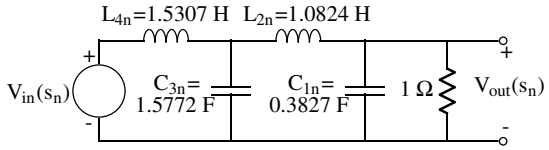
	Use these component designations for even order circuits of Fig. 9.7-12a.									
N	C_{1n}	L_{2n}	C_{3n}	L_{4n}	C_{5n}	L_{6n}	C_{7n}	L_{8n}	C_{9n}	L_{10n}
2	0.7071	1.4142								
3	0.5000	1.3333	1.5000			Butterworth (1 rps passband)				
4	0.3827	1.0824	1.5772	1.5307						
5	0.3090	0.8944	1.3820	1.6944	1.5451					
6	0.2588	0.7579	1.2016	1.5529	1.7593	1.5529				
7	0.2225	0.6560	1.0550	1.3972	1.6588	1.7988	1.5576			
8	0.1951	0.5576	0.9370	1.2588	1.5283	1.7287	1.8246	1.5607		
9	0.1736	0.5155	0.8414	1.1408	1.4037	1.6202	1.7772	1.8424	1.5628	
10	0.1564	0.4654	0.7626	1.0406	1.2921	1.5100	1.6869	1.8121	1.8552	1.5643
2	0.9110	0.9957								
3	1.0118	1.3332	1.5088		1-dB ripple Chebyshev (1 rps passband)					
4	1.0495	1.4126	1.9093	1.2817						
5	1.0674	1.4441	1.9938	1.5908	1.6652					
6	1.0773	1.4601	2.0270	1.6507	2.0491	1.3457				
7	1.0832	1.4694	2.0437	1.6736	2.1192	1.6489	1.7118			
8	1.0872	1.4751	2.0537	1.6850	2.1453	1.7021	2.0922	1.3691		
9	1.0899	1.4790	2.0601	1.6918	2.1583	1.7213	2.1574	1.6707	1.7317	
10	1.0918	1.4817	2.0645	1.6961	2.1658	1.7306	2.1803	1.7215	2.1111	1.3801
	L_{1n}	C_{2n}	L_{3n}	C_{4n}	L_{5n}	C_{6n}	L_{7n}	C_{8n}	L_{9n}	C_{10n}
	Use these component designations for odd order circuits of Fig. 9.7-12b.									

EXAMPLE 9.7-9 - Use of the Table 9.7-3 to Find a Singly-Terminated, *RLC* Low pass Filter

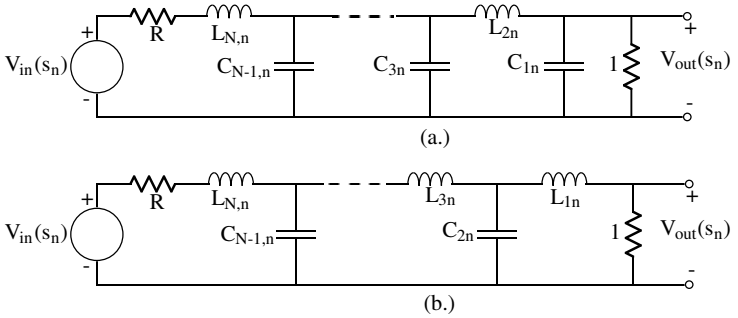
Find a singly-terminated, normalized, *RLC* filter for a 4th-order Butterworth low pass filter approximation.

Solution

Use Table 9.7-3 with the component designations at the top to get:



DOUBLY-TERMINATED *RLC* PROTOTYPE FILTERS



These structures experience a 6dB loss in the passband.

TABLE 9.7-4 - Normalized component values for Fig. 9.7-14 for the Butterworth and 1-*dB* Chebyshev doubly-terminated *RLC* approximations.

	Use these component designations for even order of Fig. 9.7-14a, R = 1Ω.									
N	C_{1n}	L_{2n}	C_{3n}	L_{4n}	C_{5n}	L_{6n}	C_{7n}	L_{8n}	C_{9n}	L_{10n}
2	1.4142	1.4142								
3	1.0000	2.0000	1.0000			Butterworth (1 rps passband)				
4	0.7654	1.8478	1.8478	0.7654						
5	0.6180	1.6180	2.0000	1.6180	0.6180					
6	0.5176	1.4142	1.9319	1.9319	1.4142	0.5176				
7	0.4450	1.2470	1.8019	2.0000	1.8019	1.2740	0.4450			
8	0.3902	1.1111	1.6629	1.9616	1.9616	1.6629	1.1111	0.3902		
9	0.3473	1.0000	1.5321	1.8794	2.0000	1.8794	1.5321	1.0000	0.3473	
10	0.3129	0.9080	1.4142	1.7820	1.9754	1.9754	1.7820	1.4142	0.9080	0.3129
3	2.0236	0.9941	2.0236		1-dB ripple Chebyshev (1 rps passband)					
5	2.1349	1.0911	3.0009	1.0911	2.1349					
7	2.1666	1.1115	3.0936	1.1735	3.0936	1.1115	2.1666			
9	2.1797	1.1192	3.1214	1.1897	3.1746	1.1897	3.1214	1.1192	2.1797	
	L_{1n}	C_{2n}	L_{3n}	C_{4n}	L_{5n}	C_{6n}	L_{7n}	C_{8n}	L_{9n}	C_{10n}
	Use these component designations for odd order of Fig. 9.7-14b, R = 1Ω.									

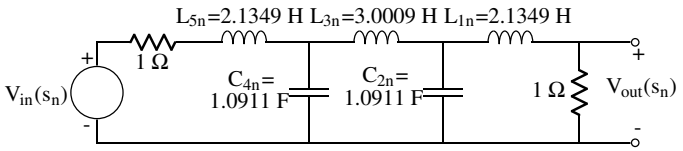
Note that no solution exists for the even-order cases of the doubly-terminated, *RLC* Chebyshev approximations for $R = 1\ \Omega$. This is a special result for $R = 1\ \Omega$ and is not true for other values of R.

EXAMPLE 9.7-10 - Use of Table 3-2 to Find a Doubly-Terminated, RLC Low-pass Filter

Find a doubly-terminated, RLC filter using minimum capacitors for a fifth-order Chebyshev filter approximation having 1 dB ripple in the passband and a source resistance of 1 Ω.

Solution

Using Table 9.7-4 and using the component designations at the top of the table gives:



FORMULATION OF THE STATE VARIABLES OF A PROTOTYPE CIRCUIT

State Variables:

The state variables of a circuit can be the current through an element or the voltage across it.

The number of state variables to solve a circuit = number of inductors and capacitors - inductor cutsets and capacitor loops.

An inductor cutset is a node where only inductors are connected.

A capacitor loop is a loop where only capacitors are in series.

The approach:

- Identify the "correct" state variables and formulate each state variable as function of itself and other state variables.
- Convert this function to a form synthesizable by switched capacitor circuits (i.e. an integrator).

A low pass example:

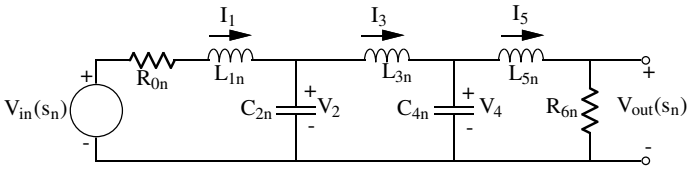


Fig. 9.7-16 - A fifth-order, low pass, normalized *RLC* ladder filter.

The state variables are I_1 , V_2, I_3, V_4, and I_5.

(The "correct" state variables will be the currents in the series elements and the voltage across the shunt elements.)

WRITING THE STATE EQUATIONS FOR A *RLC* PROTOTYPE CIRCUIT

Alternately use *KVL* and *KCL* for a loop and a node, respectively.

I_1: $V_{in}(s) - I_1(s)R_{0n} - sL_{1n}I_1(s) - V_2(s) = 0$

V_2: $I_1(s) - sC_{2n}V_2(s) - I_3(s) = 0$

I_3: $V_2(s) - sL_{3n}I_3(s) - V_4(s) = 0$

V_4: $I_3(s) - sC_{4n}V_4(s) - I_5(s) = 0$

and

I_5: $V_4(s) - sL_{5n}I_5(s) - R_{6n}I_{5n}(s) = 0$

However, we really would prefer V_{out} as a state variable instead of I_5. This is achieved using Ohm's law to get for the last two equations:

V_4: $$I_3(s) - sC_{4n}V_4(s) - \frac{V_{out}(s)}{R_{6n}} = 0$$

and

V_{out}: $$V_4(s) - \frac{sL_{5n}V_{out}(s)}{R_{6n}} - V_{out} = 0$$

VOLTAGE ANALOGS OF CURRENT

A voltage analog, V_j', of a current I_j is defined as

$$V_j' = RI_j$$

where *R'*is an arbitrary resistance (normally 1 ohm).

Rewriting the five state equations using voltage analogs for current gives:

V_1': $$V_{in}(s) - \left(\frac{V_1'(s)}{R}\right)(R_{0n} + sL_{1n}) - V_2(s) = 0$$

V_2: $$\left(\frac{V_1'(s)}{R}\right) - sC_{2n}V_2(s) - \left(\frac{V_3'(s)}{R}\right) = 0$$

V_3': $$V_2(s) - sL_{3n}\left(\frac{V_3'(s)}{R}\right) - V_4(s) = 0$$

V_4: $$\left(\frac{V_3'(s)}{R}\right) - sC_{4n}V_4(s) - \frac{V_{out}(s)}{R_{6n}} = 0$$

and

V_{out}: $$V_4(s) - \frac{sL_{5n}V_{out}(s)}{R_{6n}} - V_{out} = 0$$

THE STATE VARIABLE FUNCTIONS

Solve for each of the state variables a function of itself and other state variables.

$$V_1'(s) = \frac{R'}{sL_{1n}}\left[V_{in}(s) - V_2(s) - \left(\frac{R_{0n}}{R'}\right)V_1'(s)\right]$$

$$V_2(s) = \frac{1}{sR'C_{2n}}\ [V_1'(s) - V_3'(s)\ ]$$

$$V_3'(s) = \frac{R'}{sL_{3n}}\ [V_2(s) - V_4(s)]$$

$$V_4(s) = \frac{1}{sR'C_{4n}}\ [V_3'(s) - \left(\frac{R'}{R_{6n}}\right)\ V_{out}(s)]$$

$$V_{out}(s) = \frac{R_{6n}}{sL_{5n}}\ [V_4(s) - V_{out}(s)]$$

Note that each of these functions is the integration of voltage variables and is easily realized using the switched capacitor integrators of Sec. 9.3.

GENERAL DESIGN PROCEDURE FOR LOW PASS, SC LADDER FILTERS

1.) From T_{BP}, T_{SB}, and Ω_n (or A_{PB}, A_{SB}, and Ω_n) determine the required order of the filter approximation.

2.) From tables similar to Table 9.7-3 and 9.7-2 find the *RLC* prototype filter approximation.

3.) Write the state equations and rearrange them so each state variable is equal to the integrator of various inputs.

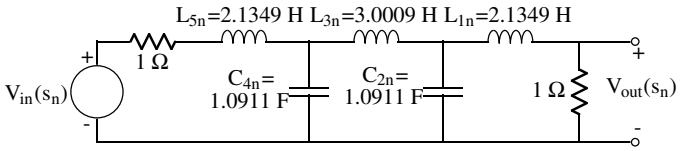
4.) Realize each of rearranged state equations by the switched capacitor integrators of Secs. 9.3.

EXAMPLE 9.7-11 - Fifth-order, Low Pass, Switched Capacitor Filter using the Ladder Approach

Design a ladder, switched capacitor realization for a Chebyshev filter approximation to the filter specifications of T_{BP} = -1*dB*, T_{SB} = -25*dB*, f_{PB} = 1kHz and f_{SB} = 1.5 kHz. Give a schematic and component value for the realization. Also simulate the realization and compare to an ideal realization. Use a clock frequency of 20 kHz. Adjust your design so that it does not suffer the -6*dB* loss in the pass band. (Note that this example should be identical with Ex. 9.7-5.)

Solution

From Ex. 9.7-5, we know that a 5th-order, Chebyshev approximation will satisfy the specification. The corresponding low pass, *RLC* prototype filter is



Next, we must find the state equations and express them in the form of an integrator. Fortunately, the above results can be directly used in this example.

Finally, use the switched-capacitor integrators of Sec. 9.3 to realize each of the five state functions and connect each of the realizations together.

EXAMPLE 9.7-11 - Continued

$$L_{1n}: \quad V_1'(s_n) = \frac{R'}{s_n L_{1n}}\left[V_{in}(s_n) - V_2(s_n) - \left(\frac{R_{0n}}{R'}\right)V_1'(s_n)\right] \qquad (1)$$

This equation can be realized by the switched capacitor integrator of Fig. 9.7-17 which has one noninverting input and two inverting inputs. Using the results of Sec. 9.3, we can write that

$$V_1'(z) = \frac{1}{z\text{-}1}\left[\alpha_{11}V_{in}(z) - \alpha_{21}zV_2(z) - \alpha_{31}zV_1'(z)\right]. \quad (2)$$

However, since $f_{PB} < f_c$, replace z by 1 and z-1 by sT.

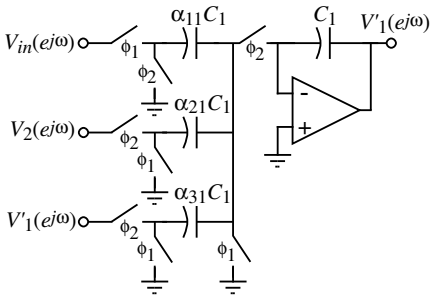


Figure 9.7-17 - Realization of V_1'.

Further, let us use the normalization defined earlier to get

$$V_1'(s_n) \approx \frac{1}{s_n T_n}\left[\alpha_{11}V_{in}(s) - \alpha_{21}V_2(s) - \alpha_{31}V_1'(s)\right]. \qquad (3)$$

Equating Eq. (1) to Eq. (3) gives the design of the capacitor ratios for the first integrator as

$$\alpha_{11} = \alpha_{21} = \frac{R'T_n}{L_{1n}} = \frac{R'\omega_{PB}}{f_c L_{1n}} = \frac{1\cdot 2000\pi}{20{,}000\cdot 2.1349} = \quad 0.1472$$

and

$$\alpha_{31} = \frac{R_{0n}T_n}{L_{1n}} = \frac{R_{0n}\omega_{PB}}{f_c L_{1n}} = \frac{1\cdot 2000\pi}{20{,}000\cdot 2.1349} = \quad 0.1472\ .$$

Assuming that $R_{0n} = R' = 1\Omega$. Also, double the value of α_{11} (α_{11} = 0.2943) in order to gain 6*dB* and remove the -6*dB* of the *RLC* prototype. The total capacitance of the first integrator is

$$\text{First integrator capacitance} = 2 + \frac{2(0.1472)}{0.1472} + \frac{1}{0.1472} = 10.79 \text{ units of capacitance.}$$

EXAMPLE 9.7-11 - Continued

C_{2n}: $$V_2(s_n) = \frac{1}{s_n R' C_{2n}} \left[V_1'(s_n) - V_3'(s_n) \right] \qquad (4)$$

This equation can be realized by the switched capacitor integrator of Fig. 9.7-18 which has one noninverting input and one inverting input. As before we write that

$$V_2(z) = \frac{1}{z-1} \left[\alpha_{12} V_1'(z) - \alpha_{22} z V_3'(z) \right]. \qquad (5)$$

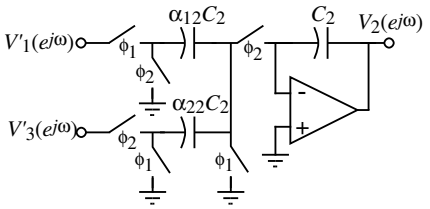


Figure 9.7-18 - Realization of V_2.

Simplifying as above gives

$$V_2(s_n) \approx \frac{1}{s_n T_n} \left[\alpha_{12} V_1'(s_n) - \alpha_{22} V_3'(s_n) \right]. \qquad (6)$$

Equating Eq. (4) to Eq. (6) yields the design of the capacitor ratios for the second integrator as

$$\alpha_{12} = \alpha_{22} = \frac{T_n}{R' C_{2n}} = \frac{\omega_{PB}}{R' f_c C_{2n}} = \frac{2000\pi}{1 \cdot 20{,}000 \cdot 1.0911} = 0.2879.$$

The second integrator has a total capacitance of

$$\text{Second integrator capacitance} = \frac{1}{0.2879} + 2 = 5.47 \text{ units of capacitance.}$$

EXAMPLE 9.7-11 - Continued

L_{3n}: $$V_3'(s_n) = \frac{R'}{s_n L_{3n}} \left[V_2(s_n) - V_4(s_n) \right] \qquad (7)$$

Eq. (7) can be realized by the switched capacitor integrator of Fig. 9.7-19 which has one noninverting input and one inverting input. For this circuit we get

$$V_3'(z) = \frac{1}{z-1} \left[\alpha_{13} V_2(z) - \alpha_{23} z V_4(z) \right]. \qquad (8)$$

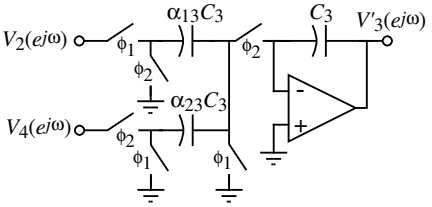


Figure 9.7-19 - Realization of V_3'.

Simplifying as above gives

$$V_3'(s_n) \approx \frac{1}{s_n T_n} \left[\alpha_{13} V_2(s_n) - \alpha_{23} V_4(s_n) \right]. \qquad (9)$$

Equating Eq. (7) to Eq. (9) yields the capacitor ratios for the third integrator as

$$\alpha_{13} = \alpha_{23} = \frac{R' T_n}{L_{3n}} = \frac{R' \omega_{PB}}{f_c L_{3n}} = \frac{1 \cdot 2000\pi}{20{,}000 \cdot 3.0009} = 0.1047.$$

The third integrator has a total capacitance of

$$\text{Third integrator capacitance} = \frac{1}{0.1047} + 2 = 11.55 \text{ units of capacitance}$$

EXAMPLE 9.7-11 - Continued

C_{4n}: $V_4(s_n) = \frac{1}{s_n R'C_{4n}} [V'_2(s_n) - \left(\frac{R'}{R_{6n}}\right) V_{out}(s_n)]$ (10)

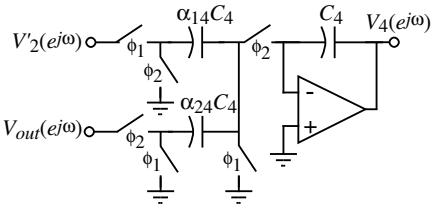


Figure 9.7-20 - Realization of V_4.

Eq. (10) can be realized by the switched capacitor integrator of Fig. 9.7-20 with one noninverting and one inverting input. As before we write that

$$V_4(z) = \frac{1}{z-1}\left[\alpha_{14}V'_3(z) - \alpha_{24}zV_{out}(z)\right]. \quad (11)$$

Assuming that $f_{PB} < f_c$ gives

$$V_4(s_n) \approx \frac{1}{s_n T_n}\left[\alpha_{14}V'_3(s_n) - \alpha_{24}V_{out}(s_n)\right]. \quad (12)$$

Equating Eq. (10) to Eq. (12) yields the design of the capacitor ratios for the fourth integrator as

$$\alpha_{14} = \alpha_{24} = \frac{T_n}{R'C_{4n}} = \frac{\omega_{PB}}{R'f_cC_{4n}} = \frac{2000\pi}{1\cdot 20{,}000\cdot 1.0911} = 0.2879.$$

if $R' = R_{0n}$. In this case, we note that fourth integrator is identical to the second integrator with the same total integrator capacitance.

EXAMPLE 9.7-11 - Continued

L_{5n}: $V_{out}(s_n) = \frac{R_{6n}}{s_n L_{5n}} [V_4(s_n) - V_{out}(s_n)]$ (13)

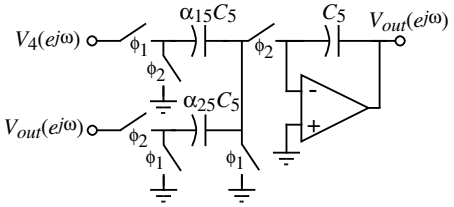


Figure 9.7-21 - Realization of V_{out}.

The last state equation, Eq. (13), can be realized by the switched capacitor integrator of Fig. 9.7-21 which has one noninverting input and one inverting input. For this circuit we get

$$V_{out}(z) = \frac{1}{z-1}[\alpha_{15}V_4(z) - \alpha_{25}zV_{out}(z)]. \quad (14)$$

Simplifying as before gives

$$V_{out}(s_n) \approx \frac{1}{s_n T_n}[\alpha_{15}V_4(s_n) - \alpha_{25}V_{out}(s_n)]. \quad (15)$$

Equating Eq. (13) to Eq. (15) yields the capacitor ratios for the fifth integrator as

$$\alpha_{15} = \alpha_{25} = \frac{R_{6n}T_n}{L_{3n}} = \frac{R_{6n}\omega_{PB}}{f_cL_{3n}} = \frac{1\cdot 2000\pi}{20{,}000\cdot 2.1349} = 0.1472$$

where $R_{6n} = 1\Omega$.

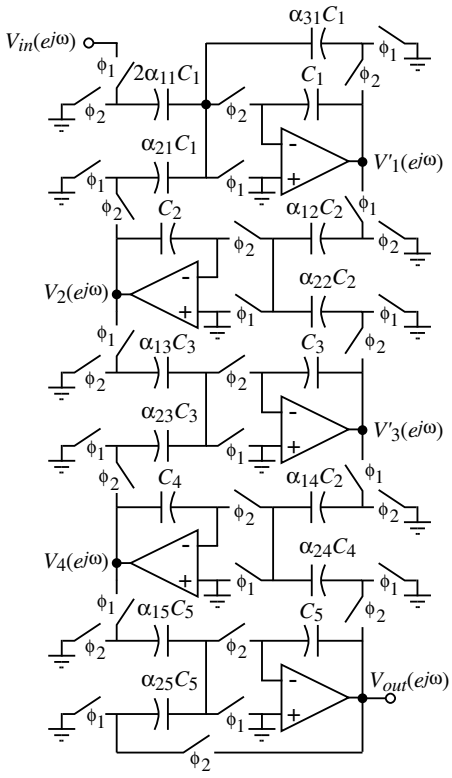
The total capacitance of the fifth integrator is

$$\text{Fifth integrator capacitance} = \frac{1}{0.1472} + 2 = 8.79 \text{ units of capacitance}$$

We see that the total capacitance of this filter is 10.79 + 5.47 + 11.53 + 5.47 + 8.79 = 42.05. We note that Ex. 9.7-5 which used the cascade approach for the same specification required 49.10 units of capacitance.

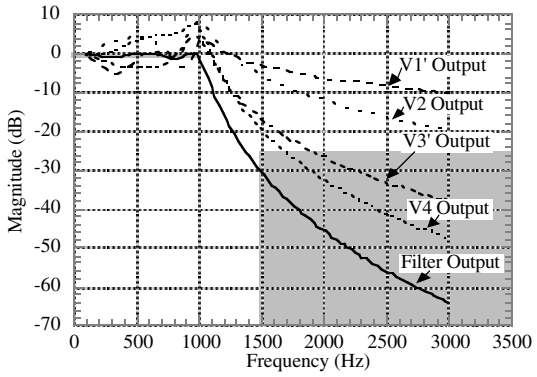
EXAMPLE 9.7-11 - Continued

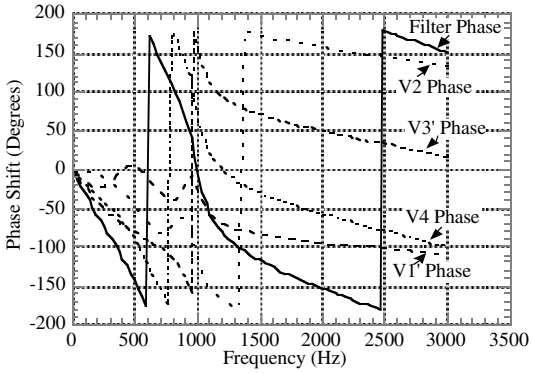
Final realization of Ex. 9.7-11.



EXAMPLE 9.7-11 - Continued

Simulated Frequency Response:





Comments:

- Both passband and stopband specifications satisfied.
- Some of the op amp outputs are exceeding 0 dB (need to voltage scale for maximum dynamic range)

EXAMPLE 9.7-11 - Continued

SPICE Input File:

```
******* 08/29/97 13:12:51 ********
******PSpice 5.2 (Jul 1992) ********

****     CIRCUIT DESCRIPTION ****

*SPICE FILE FOR EXAMPLE 9.7_5
*Example 9.7-8 : ladder filter
*Node 5 is the output at V1'
*Node 7 is the output at V2
*Node 9 is the output of V3'
*Node 11 is the output of V4
*Node 15 is the final output

VIN    1 0 DC 0 AC 1

**************************
* V1' STAGE
XNC11    1 2 3 4 NC11
XPC11    7 8 3 4 PC1
XPC12    5 6 3 4 PC1
XUSC1    5 6 3 4 USCP
XAMP1    3 4 5 6 AMP
**************************
*V2 STAGE
XNC21    5 6 19 20 NC2
XPC21    9 10 19 20 PC2
XUSC2    7 8 19 20 USCP
XAMP2    19 20 7 8 AMP
**************************
*V3' STAGE
XNC31    7 8 13 14 NC3
XPC31    11 12 13 14 PC3
XUSC3    9 10 13 14 USCP
XAMP3    13 14 9 10 AMP
**************************
*V4 STAGE
XNC41    9 10 25 26 NC2
XPC41    15 16 25 26 PC2
XUSC4    11 12 25 26 USCP
XAMP4    25 26 11 12 AMP
**************************
*VOUT STAGE
XNC51    11 12 17 18 NC1
XPC51    15 16 17 18 PC1
XUSC5    15 16 17 18 USCP
XAMP5    17 18 15 16 AMP
**************************

.SUBCKT DELAY 1 2 3
ED    4 0 1 2 1
TD    4 0 3 0 ZO=1K TD=25US
RDO    3 0 1K
.ENDS DELAY

.SUBCKT NC1 1 2 3 4
RNC1    1 0 6.7934
XNC1    1 0 10 DELAY
GNC1    1 0 10 0 .1472
XNC2    1 4 14 DELAY
GNC2    4 1 14 0 .1472
XNC3    4 0 40 DELAY
GNC3    4 0 40 0 .1472
RNC2    4 0 6.7934
.ENDS NC1
```


EXAMPLE 9.7-11 - Continued

SPICE Input File:

```
.SUBCKT NC11 1 2 3 4
RNC1    1 0 3.3978XNC1    1 0 10
DELAY
GNC1    1 0 10 0 .2943
XNC2    1 4 14 DELAY
GNC2    4 1 14 0 .2943
XNC3    4 0 40 DELAYGNC3    4 0 40 0
.2943
RNC2    4 0 3.3978
.ENDS NC11

.SUBCKT NC2 1 2 3 4
RNC1    1 0 3.4730
XNC1    1 0 10 DELAY
GNC1    1 0 10 0 .2879
XNC2    1 4 14 DELAY
GNC2    4 1 14 0 0.2879
XNC3    4 0 40 DELAY
GNC3    4 0 40 0 0.2879
RNC2    4 0 3.4730
.ENDS NC2

.SUBCKT NC3 1 2 3 4
RNC1    1 0 9.5521
XNC1    1 0 10 DELAY
GNC1    1 0 10 0 0.1047
XNC2    1 4 14 DELAY
GNC2    4 1 14 0 0.1047
XNC3    4 0 40 DELAY
GNC3    4 0 40 0 0.1047
RNC2    4 0 9.5521
.ENDS NC3

.SUBCKT NC4 1 2 3 4
RNC1    1 0 3.4730
XNC1    1 0 10 DELAY
GNC1    1 0 10 0 .2879
XNC2    1 4 14 DELAY
GNC2    4 1 14 0 .2879
XNC3    4 0 40 DELAY
GNC3    4 0 40 0 .1472
RNC2    4 0 6.7955
.ENDS NC4

.SUBCKT PC1 1 2 3 4
RPC1    2 4 6.7934
.ENDS PC1

.SUBCKT PC2 1 2 3 4
RPC1    2 4 3.4730
.ENDS PC2

.SUBCKT PC3 1 2 3 4
RPC1    2 4 9.5521
.ENDS PC3
```

EXAMPLE 9.7-11 - Continued

Switcap2 Input File (The results are exactly the same as for the SPICE simulation)

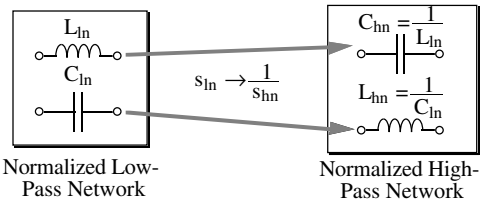
```
TITLE: EXAMPLE 9-7-11

OPTIONS;
 NOLIST;
 GRID;
 END;

TIMING;
 PERIOD 50E-6;
 CLOCK CLK 1 (0 25/50);
 END;

SUBCKT (1 4) NC (P:CAP);
 S1        (1 2)        CLK;
 S2        (2 0)        #CLK;
 S3        (3 0)        CLK;
 S4        (3 4)        #CLK;
 C11       (2 3)        CAP;
 END;

SUBCKT (1 4) PC (P:CAP1);
 S1        (1 2)        #CLK;
 S2        (2 0)        CLK;
 S3        (3 0)        CLK;
 S4        (3 4)        #CLK;
 C21       (2 3)        CAP1;
 END;

CIRCUIT

 /*****  V1' STAGE ****/
 X11   (1 2)    NC      (0.2943);
 X12   (3 2)    PC      (0.1472);
 X13   (4 2)    PC      (0.1472);
 E11   (4 0 0 2)        1E6;
 C11   (2 4)    1;

/*****  V2 STAGE ****/
 X21   (1 2)    NC      (0.2879);
 X22   (3 2)    PC      (0.2879);
 E21   (3 0 0 6)        1E6;
 C21   (6 3)    1;

/*****  V3' STAGE ****/
 X31   (3 8)    NC      (0.1047);
 X32   (7 8)    PC      (0.1047);
 E31   (5 0 0 8)        1E6;
 C31   (8 5)    1;

/*****  V4 STAGE ****/
 X41   (5 9)    NC      (0.2879);
 X42   (100 9)  PC      (0.2879);
 E41   (7 0 0 9)        1E6;
 C41   (9 7)    1;

/*****  VOUT STAGE ****/
 X51   (7 10)    NC      (0.1472);
 X52   (100 10)  PC      (0.1472);
 E51   (100 0 0 10)      1E6;
 C51   (10 100)  1;
 V1    (1 0);
 END;

ANALYZE SSS;
 INFREQQ 20 3000 LOG 80;
 SET V1 AC 1.0 0.0;
 PRINT VDB(4) VP(4) VDB(3);
 PRINT VP(3) VDB(7) VP(7);
 PRINT VDB(100) VP(100);
 PLOT VDB(100);
 END;

END;
```


HIGH PASS SWITCHED CAPACITOR FILTERS USING THE LADDER APPROACH

High pass, switched capacitor filters using the ladder approach are achieved by applying the following normalized, low pass to normalized, high pass transformation on the *RLC* prototype circuit.

$$s_{ln} = \frac{1}{s_{hn}}$$

This causes the following transformation on the inductors and capacitors of the *RLC* prototype:



Design Procedure:

1.) Identify the appropriate *RLC* prototype, low pass circuit to meet the specifications.

2.) Transform each inductor and capacitor by the normalized, low pass to high pass transformation.

3.) Choose the state variables and write the state functions.

4.) Realize the state functions using switched capacitor circuits.

The problem: The realizations are derivative circuits.

SWITCHED CAPACITOR DERIVATIVE CIRCUIT

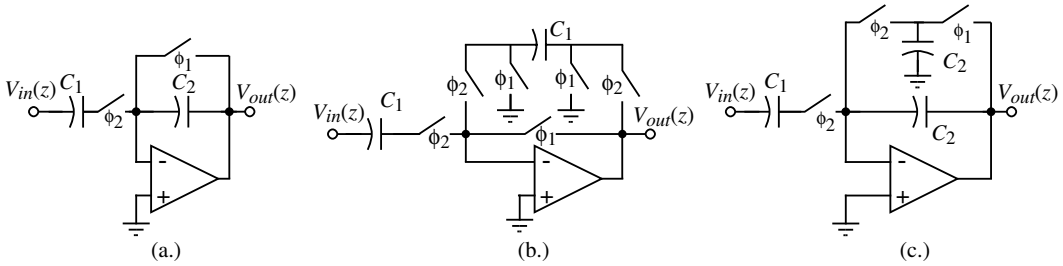
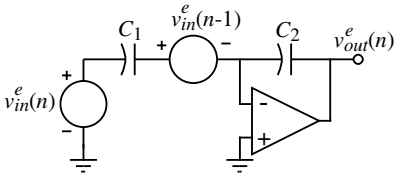


Figure 9.7-26 - (a.) Switched capacitor differentiatior circuit. (b.) Stray insensitive version of (a.). (c.) Modification to keep op amp output from being discharged to ground during ϕ_1.

Transfer function:

$\underline{\phi_1}$: $(n\text{-}1)T < t < (n\text{-}0.5)T$

$$v_{c1}^{o}(n\text{-}0.5)T = v_{in}^{e}(n\text{-}1)T \quad \text{and} \quad v_{c2}^{o}(n\text{-}0.5)T = 0$$



$\underline{\phi_2}$: $(n\text{-}0.5)T < t < (n)T$

$$v_{out}^{e}(n)T = -\frac{C_1}{C_2}v_{in}^{e}(n)T + \frac{C_1}{C_2}v_{in}^{e}(n\text{-}1)T$$

$$\therefore\ V_{out}^{e}(z) = \frac{C_1}{C_2}V_{in}^{e}(z) - z^{-1}\frac{C_1}{C_2}V_{in}^{e}(z) = -\frac{C_1}{C_2}(1\text{-}z^{-1})V_{in}^{e}(z) \quad H^{ee}(z) = \frac{V_{out}^{e}(z)}{V_{in}^{e}(z)} = -\frac{C_1}{C_2}(1\text{-}z^{-1})$$

FREQUENCY RESPONSE OF THE DERIVATIVE CIRCUIT

Replace z by $e^{j\omega T}$ to get,

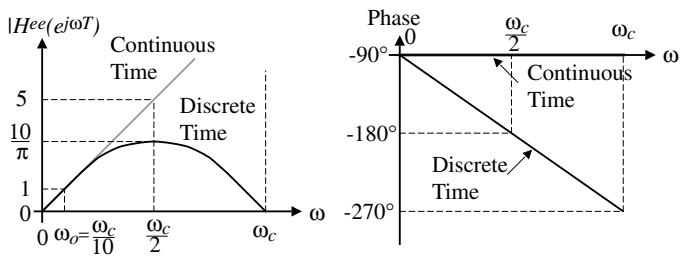
$$H^{ee}(e^{j\omega T}) = -\frac{C_1}{C_2}(1 - e^{-j\omega T}) = -\frac{C_1}{C_2}\left[\frac{e^{j\omega T/2} - e^{-j\omega T/2}}{e^{j\omega T/2}}\right] = -\frac{C_1}{C_2}(2j\omega\sin(\omega T/2))(e^{-j\omega T/2})$$

or

$$= -\frac{j\omega TC_1}{C_2}\left(\frac{\sin(\omega T/2)}{\omega T/2}\right)(\varepsilon^{-j\omega T/2}) = \left(\frac{-j\omega}{\omega_o}\right)\left(\frac{\sin(\omega T/2)}{\omega T/2}\right)(e^{-j\omega T/2}) = \text{(Ideal)x(Mag. Error)x(Phase Error)}$$

where $\omega_o = C_2/(C_1T)$.

Frequency Response for $C_2 = 0.2\pi C_1$:

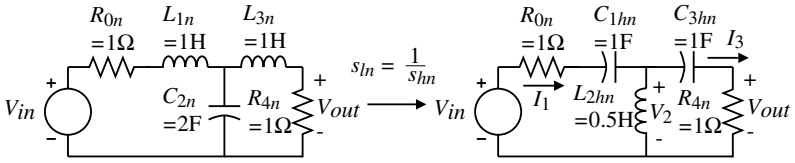


EXAMPLE 9.7-12 - High Pass, Switched Capacitor Ladder Filter

Design a high pass, switched capacitor ladder filter starting from a third-order, normalized, low pass Butterworth prototype filter. Assume the cutoff frequency is 1kHz and the clock frequency is 100kHz. Use the doubly terminated structure.

Solution

A third-order prototype filter transformed to the normalized high pass filter is shown below.



State Variable Eqs:

$$V_{in} = I_1R_{0n} + \frac{I_1}{s_nC_{1hn}} + V_2 \rightarrow I_1 = s_nC_{1hn}\,[V_{in} - I_1R_{0n} - V_2] \rightarrow \boxed{V_1' = s_nC_{1hn}R\,[V_{in} - \frac{R_{0n}}{R}V_1' - V_2]}$$

$$I_1 = \frac{V_2}{s_nL_{2hn}} + I_3 = \frac{V_2}{s_nL_{2hn}} + \frac{V_{out}}{R_{4n}} \rightarrow \quad V_2 = s_nL_{2hn}\,[I_1 - \frac{V_{out}}{R_{4n}}] \quad \rightarrow \quad \boxed{V_2 = s_nL_{2hn}[\frac{V_1'}{R} - \frac{V_{out}}{R_{4n}}]}$$

$$V_2 = \frac{I_3}{s_nC_{3hn}} + I_3R_{4n} \quad \rightarrow \quad I_3 = s_nC_{3hn}\,[V_2 - I_3R_{4n}] \quad \rightarrow \quad \boxed{V_{out} = s_nR_{4n}C_{3hn}\,[V_2 - V_{out}]}$$

Problem! Derivative circuit only has inverting inputs. Solution?

1.) Use inverters.
2.) Rearrange the equations to get integrators where possible (they will have nonintegrated inputs).
3.) Redefine the polarity of the voltages at internal nodes (180° phase reversal).

EXAMPLE 9.7-12 - Continued

Make the first equation into an integrator, reverse the sign of V_2 and V_1', and use one inverter.

Note that $V_1' = -\overline{V_1'}$ and $V_2 = -\overline{V_2}$. Therefore the rewrite the first state equation as:

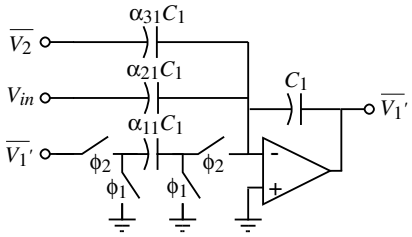
$$V_1' = s_nC_{1hn}R\,[V_{in} - \frac{R_{0n}}{R}V_1' - V_2] \rightarrow V_1' = \frac{-V_1'}{s_nC_{1hn}R_{0n}} + \frac{R}{R_{0n}}(V_{in} - V_2) \rightarrow \overline{V_1'} = \frac{-\overline{V_1'}}{s_nC_{1hn}R_{0n}} - \frac{R}{R_{0n}}(V_{in} + \overline{V_2})$$

$$V_2 = s_nL_{2hn}[\frac{V_1'}{R} - \frac{V_{out}}{R_{4n}}] \quad \rightarrow \quad \overline{V_2} = -s_nL_{2hn}[\frac{-\overline{V_1'}}{R} - \frac{V_{out}}{R_{4n}}] \rightarrow V_2 = -s_nL_{2hn}\left(\frac{\overline{V_1'}}{R} + \frac{V_{out}}{R_{4n}}\right)$$

$$V_{out} = s_nR_{4n}C_{3hn}\,[-\overline{V_2} - V_{out}]$$

C_{1hn}:

This state equation can be realized by the SC integrator shown with two inverting unswitched inputs.



We may write that:

$$\overline{V_1'}(z) = \frac{-\alpha_{11}z}{z-1}\,\overline{V_1'}(z) - \alpha_{21}V_{in}(z) - \alpha_{31}\,\overline{V_2}(z)$$

Assuming that $z - 1 \approx sT$ and $z \approx 1$, we write that

$$\overline{V_1'}(s) \approx \frac{-\alpha_{11}}{sT}\,\overline{V_1'}(s) - \alpha_{21}V_{in}(s) - \alpha_{31}\,\overline{V_2}(s)$$

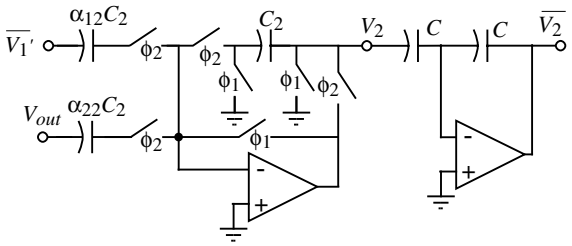
Normalizing this equation gives,

$\overline{V_1'}(s_n) \approx \frac{-\alpha_{11}}{s_n T_n}\overline{V_1'}(s_n) - \alpha_{21}V_{in}(s_n) - \alpha_{31}\overline{V_2}(s_n) \quad \rightarrow \quad \alpha_{11} = \frac{T_n}{R_{0n}C_{1hn}} = \frac{2\pi\cdot 10^3}{1\cdot 10^5} = 0.06283,\ \alpha_{21} = \alpha_{31} = 1$

EXAMPLE 9.7-12 - Continued

<u>L_{2hn}</u>:

This state eq. can be realized by the SC differentiator circuit shown with two inputs.



We may write that:

$$V_2(z) = -(1-z^{-1})[\alpha_{12}\overline{V_1'}(z) + \alpha_{22}V_{out}(z)]$$

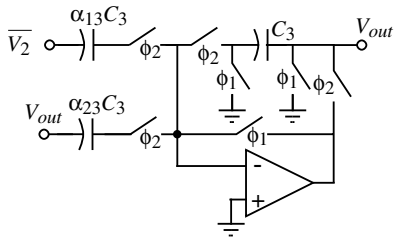
$$V_2(s) \approx -sT\,[\alpha_{12}\overline{V_1'}(s) + \alpha_{22}V_{out}(s)]$$

Normalizing T by ω_{PB} gives $V_2(s_n) = -s_n T_n [\alpha_{12}\overline{V_1'}(s_n) + \alpha_{22}V_{out}(s_n)]$

$$\therefore\ \alpha_{12} = \alpha_{22} = \frac{L_{2hn}}{T_n} = \frac{0.5\cdot 10^5}{2\pi\cdot 10^3} = 7.9577 \text{ if } R = R_{0n} = 1\Omega.$$

<u>L_{2hn}</u>:

This state equation can be realized by the SC differentiator circuit shown with two inputs.



We may write that:

$$V_{out}(z) = -(1-z^{-1})[\alpha_{13}\overline{V_2}(z) + \alpha_{23}V_{out}(z)]$$

$$V_{out}(s) \approx -sT\,[\alpha_{13}\overline{V_2}(s) + \alpha_{23}V_{out}(s)]$$

Normalizing T by ω_{PB} gives $V_{out}(s_n) = -s_n T_n [\alpha_{13}\overline{V_2}(s_n) + \alpha_{23}V_{out}(s_n)]$

$$\therefore\ \alpha_{13} = \alpha_{23} = \frac{R_{4n}C_{3hn}}{T_n} = \frac{1\cdot 10^5}{2\pi\cdot 10^3} = 15.915 \text{ if } R_{4n} = 1\Omega.$$

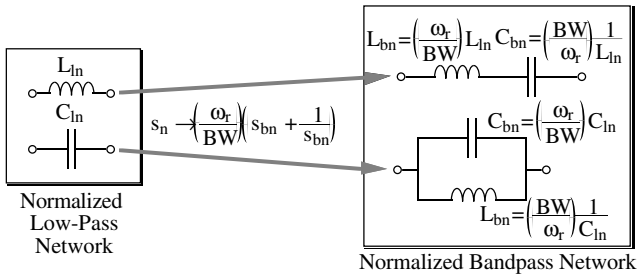
Σ capacitances = 100.49 units of capacitance

BANDPASS SWITCHED CAPACITOR FILTERS USING THE LADDER APPROACH

Bandpass switched capacitor ladder filters are obtained from low pass *RLC* prototype circuits by applying the normalized, low pass to normalized bandpass transformation given as

$$s_{ln} = \left(\frac{\omega_r}{BW}\right)\left(\frac{s_b}{\omega_r} + \frac{1}{(s_b/\omega_r)}\right) = \left(\frac{\omega_r}{BW}\right)\left(s_{bn} + \frac{1}{s_{bn}}\right)$$

This causes the following transformation on the inductors and capacitors of the *RLC* prototype:



Design Procedure:

1.) Identify the appropriate *RLC* prototype, low pass circuit to meet the specifications.

2.) Transform each inductor and capacitor by the normalized, low pass to bandpass transformation.

3.) Choose the state variables and write the state functions.

4.) Realize the state functions using switched capacitor circuits.

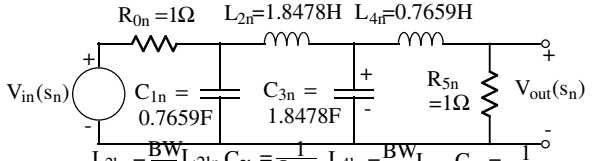
In this case, the state functions will be second-order, bandpass functions which can be realized by the second-order circuits of Sec. 9.6.

EXAMPLE 9.7-13 - Design of a Fourth-Order, Butterworth Bandpass Switched Capacitor Ladder Filter

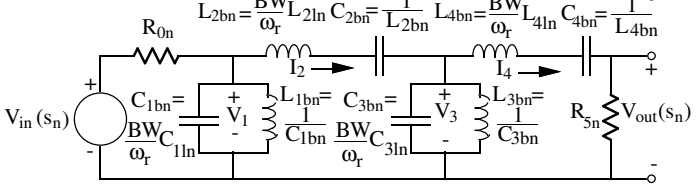
Design a fourth-order, bandpass, switched capacitor ladder filter. The filter is to have a center frequency (ω_r) of 3kHz and a bandwidth (*BW*) of 600 Hz. The clock frequency is 128kHz.

Solution

The low pass normalized prototype filter is shown (Note that this form is slightly different than the form used in Table 9.7-4)



Applying the transformation illustrated in Fig. 9.7-27 gives



The state equations for this circuit can be written as illustrated below.

$$V_{in}(s) = \left(I_2(s) + \frac{V_1(s)}{Z_{1bn}}\right)R_{0n} +$$

$$V_1(s) \rightarrow \quad V_1(s) = \frac{Z_{1bn}}{R_{0n}}[V_{in}(s) - I_2(s)R_{0n} - V_1(s)]$$

where $$Z_{1bn} = \frac{sL_{1bn}(1/sC_{1bn})}{sL_{1bn} + (1/sC_{1bn})} = \frac{s/C_{1bn}}{s^2 + (1/L_{1bn}C_{1bn})} = \frac{s/C_{1bn}}{s^2+1}$$

$$\therefore \quad V_1(s) = \frac{s/R_{0n}C_{1bn}}{s^2+1}\left[V_{in}(s) - \frac{R_{0n}}{R}V_2'(s) - V_1'(s)\right] \qquad (1)$$

EXAMPLE 9.7-13 - Continued

$$I_2(s) = Y_{2bn}[V_1(s) - V_3(s)] \qquad \rightarrow \qquad V_2'(s) = \left(\frac{sR/L_{2bn}}{s^2+1}\right)[V_1(s) - V_3(s)] \tag{2}$$

$$V_3(s) = Z_{3bn}(I_2(s)-I_4(s)) = Z_{3bn}\left(\frac{V_2'(s)}{R} - \frac{V_{out}(s)}{R_{5n}}\right) \rightarrow \; V_3(s) = \frac{s/RC_{3bn}}{s^2+1}\left[V_2'(s) - \left(\frac{R}{R_{5n}}\right)V_{out}\right] \tag{3}$$

and

$$I_4(s) = Y_{4bn}[V_3(s)-V_{out}(s)] \rightarrow \; V_{out}(s) = R_{5n}Y_{4bn}[V_3(s)-V_{out}(s)]$$

or $$V_{out}(s) = \frac{sR_{5n}/L_{4bn}}{s^2+1}[V_3(s)-V_{out}(s)] \tag{4}$$

The design of the state equations requires a re-examination of the low-Q and high-Q biquad circuits. Close examination of the above state equations and these biquads shows that the high-Q biquad can only have inverting inputs. Therefore, we shall use the low-Q biquad to realize the above state equations because it can have both inverting and noninverting inputs.

For the low-Q biquad, if we let $\alpha_1 = \alpha_3 = \alpha_6 = 0$, we get

$$H^{ee}(s) \approx \frac{-\frac{\alpha_4 s}{T}}{s^{2^\circ} + \frac{\alpha_2\alpha_5}{T^{2^\circ}}} \qquad \text{Normalizing by } \Omega_n \text{ gives} \rightarrow \qquad H^{ee}(s_n) \approx \frac{-\frac{\alpha_4 s_n}{T_n}}{s_n^{2^\circ} + \frac{\alpha_2\alpha_5}{T_n^2}}$$

We see that all α_2's and α_5's will be given as: $$\alpha_2\alpha_5 = T_n^2 = \Omega_n^2 T^2 = \frac{\omega_r^2}{f_c^2} = (2\pi)^2\left(\frac{f_r}{f_c}\right)^2$$

EXAMPLE 9.7-13 - Continued

Therefore, let $$\alpha_2 = |\alpha_5| = \frac{2\pi\cdot f_r}{f_c} = \frac{2\pi\cdot 3\text{x}10^3}{128\text{x}10^5} = 0.1473$$

Now all that is left is to design α_4 for each stage (assuming $R_{0n} = R_{5n} = R = 1\Omega$).

Also, the sum of capacitances per stage will be:

$$\Sigma \text{ capacitances/stage} = \frac{\alpha_2}{\alpha_{min}} + \frac{|\alpha_5|}{\alpha_{min}} + \frac{2}{\alpha_{min}} + \frac{\alpha_4}{\alpha_{min}} \text{x (no. of inputs)}$$

<u>Stage 1</u>

$$\frac{\alpha_{41}}{T_n} = \frac{1}{R_{0n}C_{1bn}} \quad \rightarrow \quad \alpha_{41} = \frac{T_n}{R_{0n}C_{1bn}} = \frac{\omega_r\cdot BW}{f_c\cdot\omega_r\cdot C_{1ln}} = \frac{2\pi\cdot 600}{128\text{x}10^3\cdot 0.7658} = 0.03848$$

There will be one noninverting input (V_{in}) and two inverting inputs (V_2' and V_1).

$$\Sigma \text{ capacitances} = \frac{2(0.1437)}{0.03848} + \frac{2}{0.03848} + 3 = 62.44 \text{ units of capacitance}$$

<u>Stage 2</u>

$$\frac{\alpha_{42}}{T_n} = \frac{R}{L_{2bn}} \quad \rightarrow \quad \alpha_{42} = \frac{T_n\cdot BW}{\omega_r L_{2ln}} = \frac{\omega_r\cdot BW}{f_c\cdot\omega_r\cdot L_{2ln}} = \frac{2\pi\cdot 600}{128\text{x}10^3\cdot 1.8478} = 0.01594$$

There will be one noninverting input (V_1) and one inverting input (V_3).

$$\Sigma \text{ capacitances} = \frac{2(0.1437)}{0.01594} + \frac{2}{0.01594} + 2 = 145.50 = \text{units of capacitance}$$

<u>Stage 3</u>

Same as stage 2. $\alpha_{43} = 0.01594$

There will be one noninverting input (V_2') and one inverting input (V_{out}).

Σ capacitances = 145.50 units of capacitance

EXAMPLE 9.7-13 - Continued

Stage 4

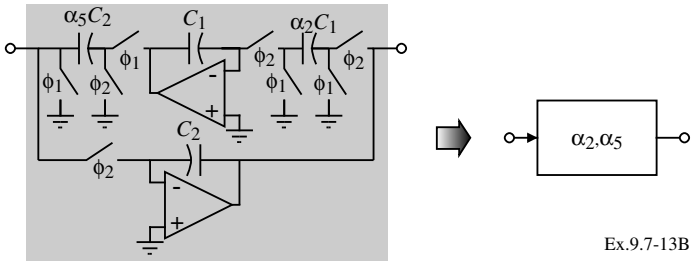
Same as stage 1. $\alpha_{44} = 0.03848$.

There will be one noninverting input (V_3) and one inverting input (V_{out}).

Σ capacitances = 61.44 units of capacitance.

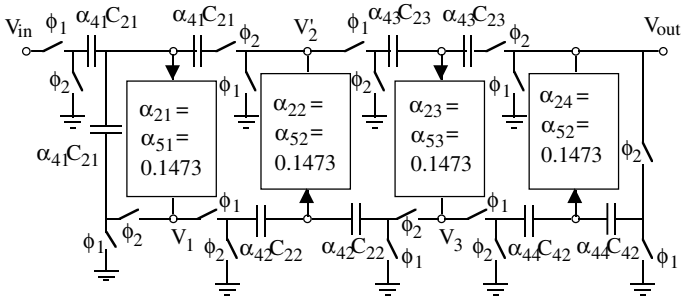
Total capacitance of this example is 414.88 units of capacitance.

Realization:

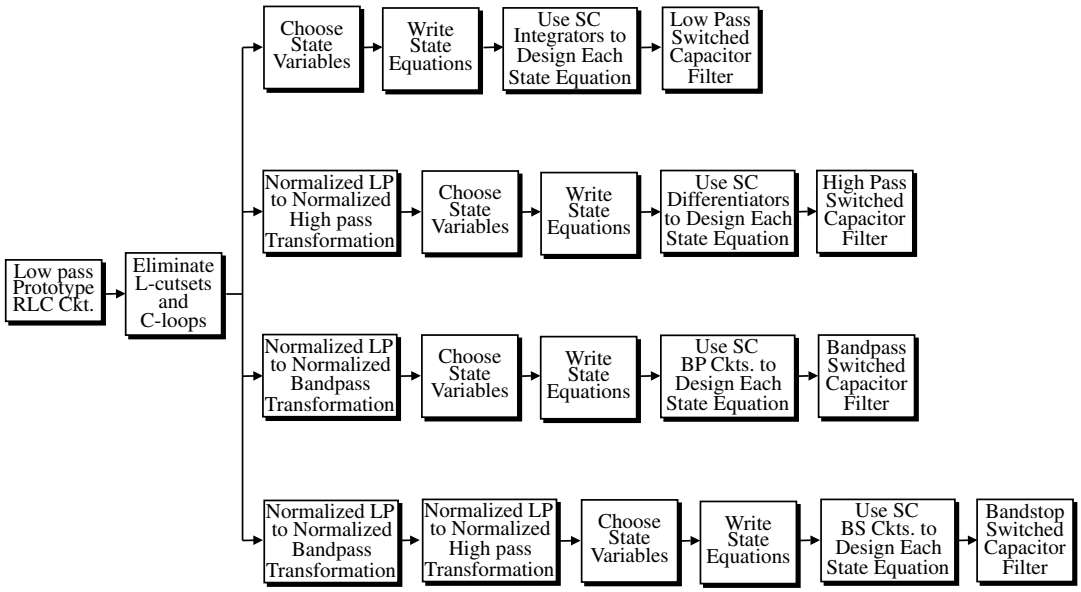


Ex.9.7-13B

Using this simplification gives:



GENERAL APPROACH TO DESIGNING SWITCHED CAPACITOR LADDER FILTERS



ANTI-ALIASING IN SWITCHED CAPACITOR FILTERS

A characteristic of circuits that sample the signal (switched capacitor circuits) is that the signal passbands occur at each harmonic of the clock frequency including the fundamental.

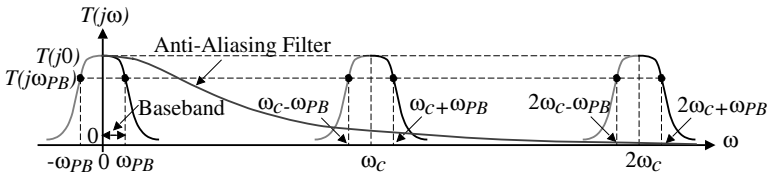


Figure 9.7-28 - Spectrum of a discrete-time filter and a continuous-time anti-aliasing filter.

The primary problem of aliasing is that there are undesired passbands that contribute to the noise in the desired baseband.

NOISE ALIASING IN SWITCHED CAPACITOR CIRCUITS

In all switched capacitor circuits, a noise aliasing occurs from the passbands that occur at the clock frequency and each harmonic of the clock frequency.

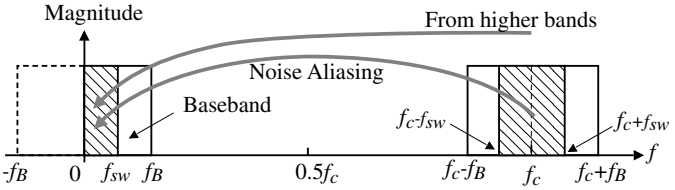


Figure 9.7-31 - Illustration of noise aliasing in switched capacitor circuits.

It can be shown that the aliasing enhances the baseband noise voltage spectral density by a factor of $2f_{sw}/f_c$. Therefore, the baseband noise voltage spectral density is

$$\overline{e_{BN}^2} = \left(\frac{kT/C}{f_{sw}}\right)\text{x}\left(\frac{2f_{sw}}{f_c}\right) = \frac{2kT}{f_cC}\ \text{volts}^2/\text{Hz}$$

Multiplying this equation by $2f_B$ gives the baseband noise voltage in volts(rms)^2. Therefore, the baseband noise voltage is

$$v_{BN}^2 = \left(\frac{2kT}{f_cC}\right)(2f_B) = \frac{2kT}{C}\left(\frac{2f_B}{f_c}\right) = \frac{2kT/C}{OSR}\ \text{volts(rms)}^2$$

where *OSR* is the oversampling ratio.

SIMULATION OF NOISE IN SWITCHED CAPACITOR FILTERS

The noise of switched capacitor filters can be simulated using the above concepts.

1.) Convert the switched capacitor filter to a continuous time equivalent filter by replacing each switched capacitor with a resistor whose value is $1/(f_c C)$.

2.) Multiply the noise of this resistance by $2f_B/f_c$, to make the resulting noise to approximate that of the switched capacitor filter.

Unfortunately, simulators like SPICE do not permit the multiplication of the thermal noise. Another approach is to assume that the resistors are noise-free and build a noise generator that represents the effect of the noise of v_{BN}^2.

1.) Put a zero dc current through a resistor identical to the one being modeled.

2.) A voltage source that is dependent on the voltage across this resistor can be placed at the input of an op amp to implement v_{BN}^2. The gain of the voltage dependent source should be $2f_B/f_c$.

3.) Model all resistors that represent switched capacitors in the same manner.

The resulting noise source model along with the normal noise sources of the op amp will serve as a reasonable approximation to the noise in a switched capacitor filter.

CONTINUOUS TIME ANTI-ALIASING FILTERS

Sallen and Key, Unity Gain, Low Pass Filter:

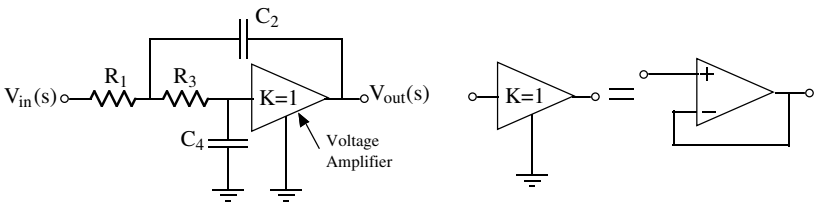


Fig. 9.7-29 - (a.) A second-order, low pass active filter using positive feedback. (b.) The realization of the voltage amplifier K by the noninverting op amp configuration.

Transfer function:

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{\frac{K}{R_1R_3C_2C_4}}{s^2 + s\left(\frac{1}{R_3C_4} + \frac{1}{R_1C_2} + \frac{1}{R_3C_2} - \frac{K}{R_3C_4}\right) + \frac{1}{R_1R_3C_2C_4}} = \frac{T_{LP}(0)\,\omega_o^2}{s^2 + \left(\frac{\omega_o}{Q}\right)s + \omega_o^2}$$

We desire $K = 1$ in order to not influence the passband gain of the SCF. Therefore, with $K = 1$,

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{\frac{1}{R_1R_3C_2C_4}}{s^2 + s\left(\frac{1}{R_1C_2} + \frac{1}{R_3C_2}\right) + \frac{1}{R_1R_3C_2C_4}} = \frac{1/mn(RC)^2}{s^2 + (1/RC)[(n+1)/n]s + 1/mn(RC)^2}$$

where $R_3 = nR_1 = nR$ and $C_4 = mC_2 = mC$.

DESIGN EQS. FOR THE UNITY GAIN, SALLEN AND KEY LOW PASS FILTER

Equating $V_{out}(s)/V_{in}(s)$ to the standard second-order low pass transfer function, we get two design equations which are

$$\omega_o = \frac{1}{\sqrt{mn}RC}$$

$$\frac{1}{Q} = (n+1)\sqrt{\frac{m}{n}}$$

The approach to designing the components of Fig. 9.7-29a is to select a value of m compatible with standard capacitor values such that

$$m \leq \frac{1}{4Q^2} \ .$$

Then, n, can be calculated from

$$n = \left(\frac{1}{2mQ^2} - 1\right) \pm \frac{1}{2mQ^2}\sqrt{1-4mQ^2} \ .$$

This equation provides two values of n for any given Q and m. It can be shown that these values are reciprocal. Thus, the use of either one produces the same element spread.

EXAMPLE 9.7-9 - Application of the Sallen-Key Anti-Aliasing Filter

Use the above design approach to design a second-order, low-pass filter using Fig. 9.7-7a if Q = 0.707 and f_o = 1 kHz

Solution

We see that m should be less than 0.5 for this example. Let us choose m = 0.5.

$$m = 0.5 \ \rightarrow \ n = 1.$$

These choices guarantee that Q = 0.707.

Now, use $\omega_o = \frac{1}{\sqrt{mn}RC}$ to find the RC product $\rightarrow$ $RC = 0.225\text{x}10^{-3}$.

At this point, one has to try different values to see what is best for the given situation (typically the area required).

Let us choose $C = C_2$ = 500pF.

This gives $R = R_1$ = 450kΩ. Thus, C_4 = 250pF and R_3 = 450kΩ.

It is readily apparent that the anti-aliasing filter will require considerable area to implement.

A NEGATIVE FEEDBACK, SECOND-ORDER, LOW PASS ANTI-ALIASING FILTER

Another continuous-time filter suitable for anti-aliasing filtering is shown in Fig. 9.7-30. This filter uses frequency-dependent negative feedback to achieve complex conjugate poles.

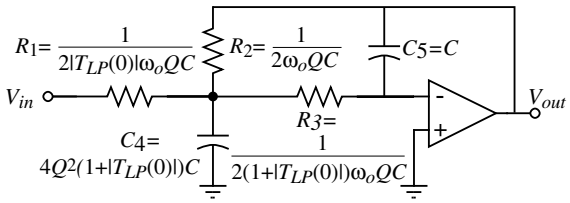


Figure 9.7-30 - A negative feedback realization of a second-order, low pass filter.

This gain of this circuit in the passband is determined by the ratio of R_2/R_1.

EXAMPLE 9.7-10 - Design of A Negative Feedback, Second-Order, Low-Pass Active Filter

Use the negative feedback, second-order, low-pass active filter of Fig. 9.7-30 to design a low-pass filter having a dc gain of -1, Q = $1/\sqrt{2}$, and f_o = 10kHz.

Solution

Let us use the design equations given on Fig. 9.7-30. Assume that $C_5 = C = 100pF$. Therefore, we get $C_4 = (8)(0.5)C = 400pF$. The resistors are

$$R_1 = \frac{\sqrt{2}}{(2)(1)(6.2832)(10^{-6})} = 112.54\ k\Omega\ .$$

$$R_2 = \frac{\sqrt{2}}{(2)(6.2832)(10^{-6})} = 112.54\ k\Omega\ .$$

and

$$R_3 = \frac{\sqrt{2}}{(2)(6.2832)(2)(10^{-6})} = 56.27\ k\Omega\ .$$

Unfortunately we see that because of the passive element sizes that anti-aliasing filters will occupy a large portion of the chip.

SUMMARY

- Switched capacitor circuits have reached maturity in CMOS technology.
- The switched capacitor circuit concept was a pivotal step in the implementation of analog signal processing circuits in CMOS technology.
- The accuracy of the signal processing is proportional to capacitor ratios.
- Switched capacitor circuits have been developed for:

  Amplification

  Integration

  Differentiation

  Summation

  Filtering

  Comparing

  Analog-digital conversion
- Approaches to switched capacitor circuit design:

  Oversampled approach - clock frequency is much greater than the signal frequency

  z-domain approach - specifications converted to the z-domain and directly realized, can operate to within half of the clock frequency
- Switched capacitor circuits can be simulated in the frequency domain by SPICE or SWITCAP
- Clock feedthrough and *kT/C* noise represent the lower limit of the dynamic range of switched capacitor circuits.