EE247
Lecture 8

- Continuous-time filters continued
  - Various Gm-C filter implementations
  - Comparison of continuous-time filter topologies
- Switched-Capacitor Filters
  - “Analog” sampled-data filters:
    - Continuous amplitude
    - Quantized time
  - Applications:
    - First commercial product: Intel 2912 voice-band CODEC chip, 1979
    - Oversampled A/D and D/A converters
    - Stand-alone filters
      E.g. National Semiconductor LMF100 (x2 biquads)

Summary Last Lecture

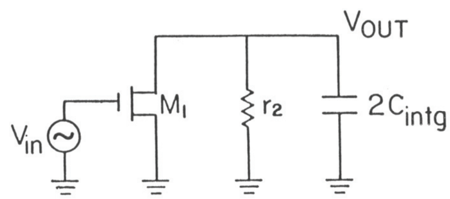
- Automatic on-chip filter tuning (continued from previous lecture)
  - Continuous tuning
    - Reference integrator locked to a reference frequency
    - DC tuning of resistive timing element
  - Periodic digitally assisted tuning
    - Systems where filter is followed by ADC & DSP, existing hardware can be used to periodically update filter freq. response
- Continuous-time filters
  - Highpass filters- 1st order→ integrator in the feedback path
  - Bandpass filters
    - Cascade of LP and HP for $Q_{filter}<5$
    - Direct implementation for narrow-band filter via LP to BP transformation

Simplest Form of CMOS Gm-Cell Nonidealities

- DC gain (integrator Q)

$$a = \frac{g_m^{M1,2}}{g_0^{M1,2} + g_{load}}$$

$$a = \frac{2L}{\theta \left(V_{gs} - V_{th}\right)_{M1,2}}$$



Small Signal Differential Mode Half-Circuit

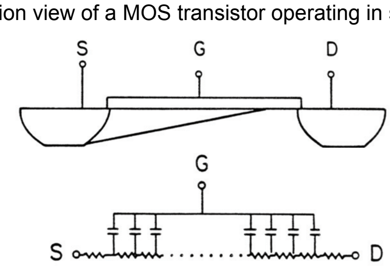
- Where a denotes DC gain & θ is related to channel length modulation by:

$$\lambda = \frac{\theta}{L}$$

- Seems no extra poles!

CMOS Gm-Cell High-Frequency Poles

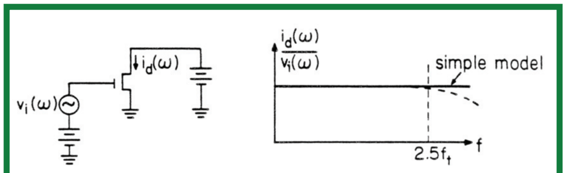
Cross section view of a MOS transistor operating in saturation



Distributed channel resistance & gate capacitance

- Distributed nature of gate capacitance & channel resistance results in infinite no. of high-frequency poles

CMOS Gm-Cell High-Frequency Poles



High frequency behavior of an MOS transistor operating in saturation region

$$P_2^{effective} \approx \frac{1}{\sum_{i=2}^{\infty} \frac{1}{P_i}}$$

$$P_2^{effective} \approx 2.5\omega_t^{M1,2}$$

$$\omega_t^{M1,2} = \frac{g_m^{M1,2}}{2/3C_{ox}WL} = \frac{3}{2}\frac{\mu\left(V_{gs}-V_{th}\right)_{M1,2}}{L^2}$$

- Distributed nature of gate capacitance & channel resistance results in an effective pole at 2.5 times input device cut-off frequency

Simple Gm-Cell Quality Factor

$$a = \frac{2L}{\theta\left(V_{gs}-V_{th}\right)_{M1,2}}$$

$$P_2^{effective} = \frac{15}{4}\frac{\mu\left(V_{gs}-V_{th}\right)_{M1,2}}{L^2}$$

$$Q_{real}^{intg.} \approx \frac{1}{\frac{1}{a} - \omega_o \sum_{i=2}^{\infty} \frac{1}{p_i}}$$

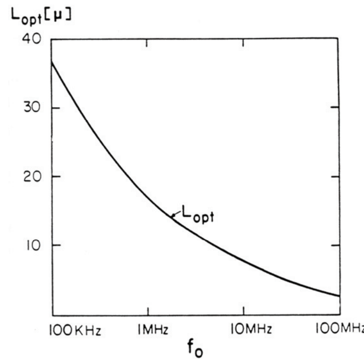
$$\frac{1}{Q^{intg.}} \approx \frac{\theta\left(V_{gs}-V_{th}\right)_{M1,2}}{2L} - \frac{4}{15}\frac{\omega_o L^2}{\mu\left(V_{gs}-V_{th}\right)_{M1,2}}$$

- Note that phase lead associated with DC gain is inversely prop. to L
- Phase lag due to high-freq. poles directly prop. to L

→ For a given ω_o there exists an optimum *L* which cancel the lead/lag phase error resulting in high integrator *Q*

Simple Gm-Cell Channel Length for Optimum Integrator Quality Factor

$$L_{opt.} \approx \left[\frac{15}{4} \frac{\theta\mu\left(V_{gs} - V_{th}\right)^2_{M1,2}}{\omega_o} \right]^{1/3}$$

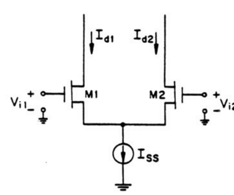


- Optimum channel length computed based on process parameters (could vary from process to process)

Source-Coupled Pair CMOS Gm-Cell Transconductance

For a source-coupled pair the differential output current (ΔI_d) as a function of the input voltage(Δv_i):

$$\Delta I_d = I_{ss}\left[\frac{\Delta v_i}{\left(V_{gs} - V_{th}\right)_{M1,2}}\right]\left\{1 - \frac{1}{4}\left[\frac{\Delta v_i}{\left(V_{gs} - V_{th}\right)_{M1,2}}\right]^2\right\}^{1/2}$$



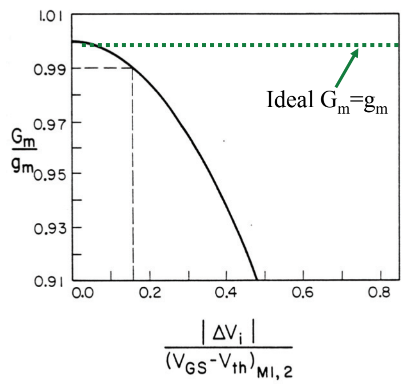
$$Note: For\ small \left[\frac{\Delta v_i}{\left(V_{gs} - V_{th}\right)_{M1,2}}\right] \rightarrow \frac{\Delta I_d}{\Delta v_i} = g_m^{M1,M2}$$

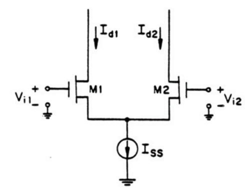
Note: As Δv_i *increases* $\frac{\Delta I_d}{\Delta v_i}$ *or the effective transconductance decreases*

$$\Delta v_i = V_{i1} - V_{i2}$$

$$\Delta I_d = I_{d1} - I_{d2}$$

Source-Coupled Pair CMOS Gm-Cell Linearity

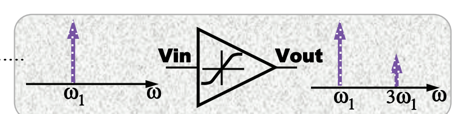




- Large signal G_m drops as input voltage increases
  → Gives rise to nonlinearity

Measure of Linearity

$$Vout = \alpha_1 Vin + \alpha_2 Vin^2 + \alpha_3 Vin^3 + ...$$

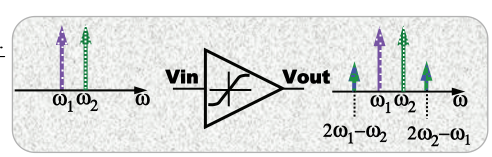


$$HD3 = \frac{amplitude\ 3rd\ harmonic\ dist.\ comp.}{amplitude\ fundamental}$$

$$= \frac{1}{4}\frac{\alpha_3}{\alpha_1} Vin^2 + ...$$

$$IM_3 = \frac{amplitude\ 3rd\ order\ IM\ comp.}{amplitude\ fundamental}$$

$$= \frac{3}{4}\frac{\alpha_3}{\alpha_1} Vin^2 + \frac{25}{8}\frac{\alpha_5}{\alpha_1} Vin^4 + ...$$



Source-Coupled Pair Gm-Cell Linearity

$$\Delta I_d = I_{ss}\left[\frac{\Delta v_i}{\left(V_{gs}-V_{th}\right)_{M1,2}}\right]\left\{1-\frac{1}{4}\left[\frac{\Delta v_i}{\left(V_{gs}-V_{th}\right)_{M1,2}}\right]^2\right\}^{1/2} \qquad (1)$$

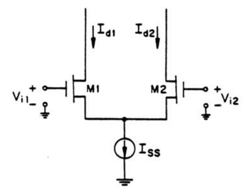
$$\Delta I_d = a_1\times\Delta v_i + a_2\times\Delta v_i^2 + a_3\times\Delta v_i^3 + \ldots\ldots\ldots\ldots$$

Series expansion used in (1)

$$a_1 = \frac{I_{ss}}{\left(V_{gs}-V_{th}\right)_{M1,2}} \qquad \& \qquad a_2 = 0$$

$$a_3 = -\frac{I_{ss}}{8\left(V_{gs}-V_{th}\right)^3_{M1,2}} \qquad \& \qquad a_4 = 0$$

$$a_5 = -\frac{I_{ss}}{128\left(V_{gs}-V_{th}\right)^5_{M1,2}} \qquad \& \qquad a_6 = 0$$

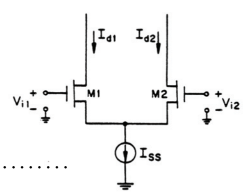


Linearity of the Source-Coupled Pair CMOS Gm-Cell

$$IM3 \approx \frac{3a_3}{4a_1}\hat{v}_i^2 + \frac{25a_5}{8a_1}\hat{v}_i^4 \ldots\ldots\ldots\ldots$$

Substituting for $a_1, a_3, \ldots.$

$$IM3 \approx \frac{3}{32}\left(\frac{\hat{v}_i}{(V_{GS}-V_{th})}\right)^2 + \frac{25}{1024}\left(\frac{\hat{v}_i}{(V_{GS}-V_{th})}\right)^4 \ldots\ldots\ldots\ldots$$



$$\hat{v}_{i\,max} \approx 4(V_{GS}-V_{th})\times\sqrt{\frac{2}{3}\times IM3}$$

$$IM_3 = 1\% \;\&\; (V_{GS}-V_{th}) = 1V \;\Rightarrow \hat{V}_{in}^{rms} \approx 230mV$$

- Key point: Max. signal handling capability function of gate-overdrive voltage

Simplest Form of CMOS Gm Cell Disadvantages

•Max. signal handling capability function of gate-overdrive

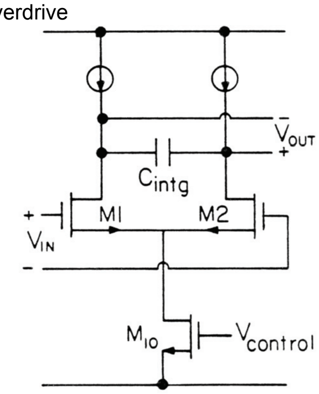
$$IM_3 \propto \left(V_{GS} - V_{th}\right)^{-2}$$

•Critical freq. is also a function of gate-overdrive

$$\omega_o = \frac{g_m^{M1,2}}{2 \times C_{intg}}$$

since $g_m = \mu C_{ox} \frac{W}{L}\left(V_{gs} - V_{th}\right)$

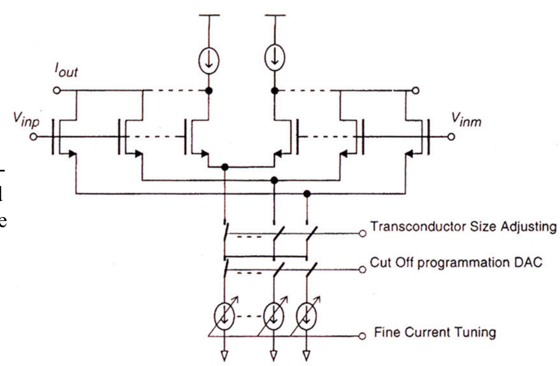
then $\omega_o \propto \left(V_{gs} - V_{th}\right)$



→ Filter tuning affects max. signal handling capability!

Simplest Form of CMOS Gm Cell Removing Dependence of Maximum Signal Handling Capability on Tuning

- Can overcome problem of max. signal handling capability being a function of tuning by providing tuning through :
  - Coarse tuning via switching in/out binary-weighted cross-coupled pairs→ Try to keep gate overdrive voltage constant
  - Fine tuning through varying current sources



→ Dynamic range dependence on tuning removed (to 1st order)

Ref: R.Castello ,I.Bietti, F. Svelto , "High-Frequency Analog Filters in Deep Submicron Technology , "*International Solid State Circuits Conference*, pp 74-75, 1999.

Dynamic Range for Source-Coupled Pair Based Filter

$$IM_3 = 1\% \;\; \& \;\; \left(V_{GS} - V_{th}\right) = 1V \quad \Rightarrow V_{in}^{rms} \approx 230mV$$

- Minimum detectable signal determined by total noise voltage
- It can be shown for the 6th order Butterworth bandpass filter fundamental noise contribution is given by:

$$\sqrt{\overline{v_o^2}} \approx \sqrt{3\,Q\frac{k\,T}{C_{intg}}}$$

$$Assuming \quad Q = 10 \quad C_{intg} = 5pF$$

$$v_{noise}^{rms} \approx 160\mu V$$

$$since \;\; v_{max}^{rms} = 230mV$$

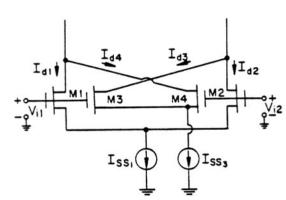
$$Dynamic\,Range = 20log\frac{230x10^{-3}}{160x10^{-6}} \approx 63dB$$

Improving the Max. Signal Handling Capability of the Source-Coupled Pair Gm-Cell

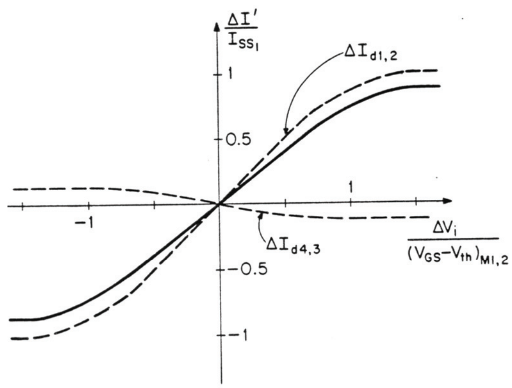
- 2nd source-coupled pair added to subtract current proportional to nonlinear component associated with the main SCP

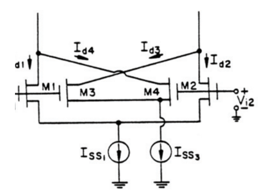
$$\frac{I_{ss1}}{I_{ss3}} = b \quad \& \quad \frac{\left(V_{gs} - V_{th}\right)_{M1,2}}{\left(V_{gs} - V_{th}\right)_{M3,4}} = a \quad and\ thus$$

$$\frac{\left(\frac{W}{L}\right)_{M1,2}}{\left(\frac{W}{L}\right)_{M3,4}} = \frac{b}{a^2}$$



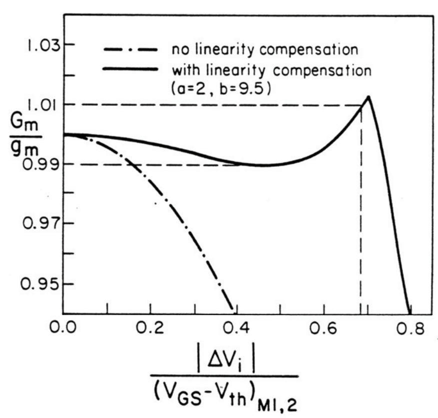
Improving the Max. Signal Handling Capability of the Source-Coupled Pair Gm





Ref: H. Khorramabadi, "High-Frequency CMOS Continuous-Time Filters," U. C. Berkeley, Department of Electrical Engineering, Ph.D. Thesis, February 1985 (ERL Memorandom No. UCB/ERL M85/19).

Improving the Max. Signal Handling Capability of the Source-Coupled Pair Gm

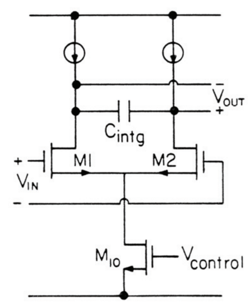


- Improves maximum signal handling capability by about 12dB

  → Dynamic range theoretically improved to 63+12=75dB

Simplest Form of CMOS Gm-Cell

- Pros
  - Capable of very high frequency performance (highest?)
  - Simple design
- Cons
  - Tuning affects power dissipation
  - Tuning affects max. signal handling capability (can overcome)
  - Limited linearity (possible to improve)



Ref: H. Khorramabadi and P.R. Gray, "High Frequency CMOS continuous-time filters," *IEEE Journal of Solid-State Circuits,* Vol.-SC-19, No. 6, pp.939-948, Dec. 1984.

Gm-Cell
Source-Coupled Pair with Degeneration

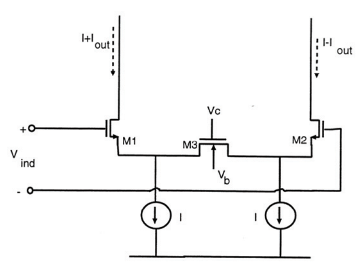
$$I_d = \frac{\mu C_{ox}}{2}\frac{W}{L}\left[2\left(V_{gs}-V_{th}\right)V_{ds}-V_{ds}^2\right]$$

$$g_{ds} = \frac{\partial I_d}{\partial V_{ds}} \approx \mu C_{ox}\frac{W}{L}\left(V_{gs}-V_{th}\right)\Big|_{V_{ds}\ small}$$

$$g_{eff} = \frac{1}{\frac{1}{g_{ds}^{M3}}+\frac{2}{g_m^{M1,2}}}$$

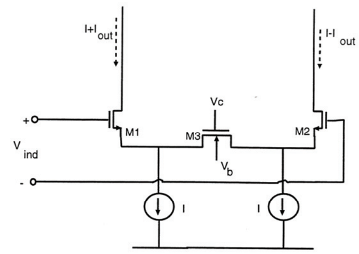
$$for\ g_m^{M1,2} >> g_{ds}^{M3}$$

$$g_{eff} \approx g_{ds}^{M3}$$



M3 operating in triode mode → source degeneration→ determines overall gm
Provides tuning through varing Vc

Gm-Cell
Source-Coupled Pair with Degeneration



- Pros
  - Moderate linearity
  - Continuous tuning provided by Vc
  - Tuning does not affect power dissipation
- Cons
  - Extra poles associated with the source of M1,2,3 → Low frequency applications only

Ref: Y. Tsividis, Z. Czarnul and S.C. Fang, "MOS transconductors and integrators with high linearity," *Electronics Letters,* vol. 22, pp. 245-246, Feb. 27, 1986

BiCMOS Gm-Cell Example

- MOSFET in triode mode:

$$I_d = \frac{\mu C_{ox}}{2}\frac{W}{L}\left[2\left(V_{gs} - V_{th}\right)V_{ds} - V_{ds}^2\right]$$

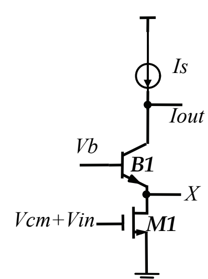
- Note that if Vds is kept constant:

$$g_m^{M1} = \frac{\partial I_d}{\partial V_{gs}} = \mu C_{ox}\frac{W}{L}V_{ds}$$

- Linearity performance → keep *gm* constant→ function of how constant *Vds* can be held
  - Need to minimize Gain @ Node X

$$A_x = g_m^{M1} / g_m^{B1}$$

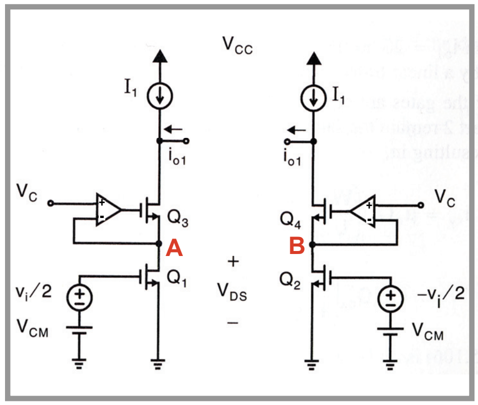
- Since for a given current, *gm* of BJT is larger compared to MOS- preferable to use BJT
- Extra pole at node X



gm can be varied by changing *Vb* and thus *Vds*

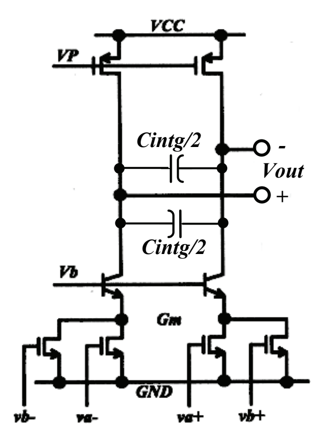
Alternative Fully CMOS Gm-Cell Example

- BJT replaced by a MOS transistor with boosted gm
- Lower frequency of operation compared to the BiCMOS version due to more parasitic capacitance at nodes A & B

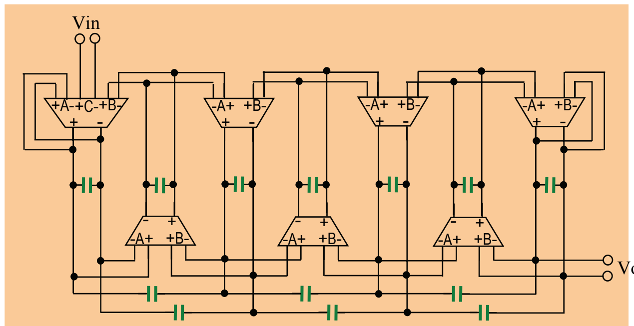


BiCMOS Gm-C Integrator

- Differential- needs common-mode feedback ckt
- Freq.tuned by varying Vb
- Design tradeoffs:
  - Extra poles at the input device drain junctions
  - Input devices have to be small to minimize parasitic poles
  - Results in high input-referred offset voltage → could drive ckt into non-linear region
  - Small devices → high 1/f noise



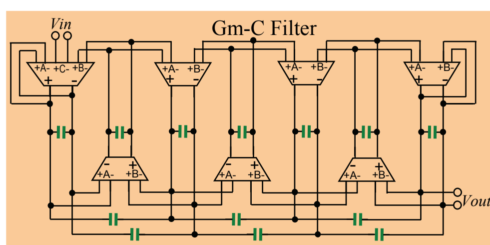
7th Order Elliptic Gm-C LPF For CDMA RX Baseband Application

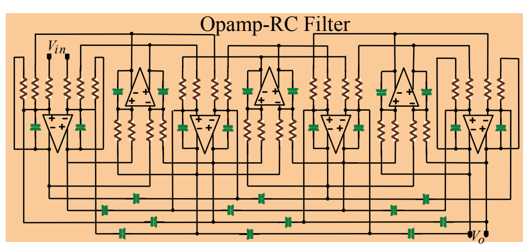


- Gm-Cell in previous page used to build a 7th order elliptic filter for CDMA baseband applications (650kHz corner frequency)
- In-band dynamic range of <50dB achieved

Comparison of 7th Order Gm-C versus Opamp-RC LPF

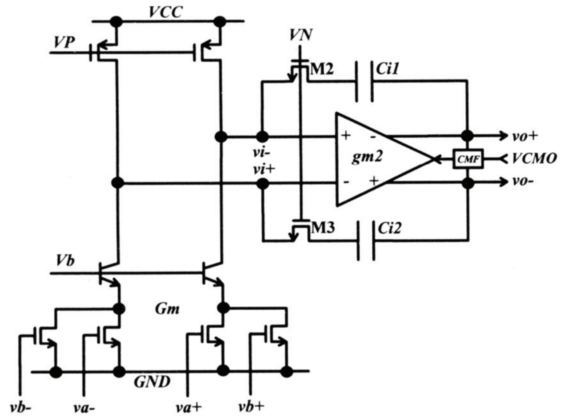
- Gm-C filter requires 4 times less intg. cap. area compared to Opamp-RC
  →For low-noise applications where filter area is dominated by Cs, could make a significant difference in the total area
- Opamp-RC linearity superior compared to Gm-C
- Power dissipation tends to be lower for Gm-C since OTA load is C and thus no need for buffering





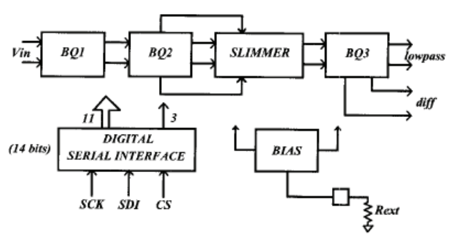
BiCMOS Gm-OTA-C Integrator

- Used to build filter for disk-drive applications
- Since high frequency of operation, time-constant sensitivity to parasitic caps significant.
  → Opamp used
- M2 & M3 added to compensate for phase lag (provides phase lead)



Ref: C. Laber and P.Gray, "A 20MHz 6th Order BiCMOS Parasitic Insensitive Continuous-time Filter & Second Order Equalizer Optimized for Disk Drive Read Channels," *IEEE Journal of Solid State Circuits,* Vol. 28, pp. 462-470, April 1993.

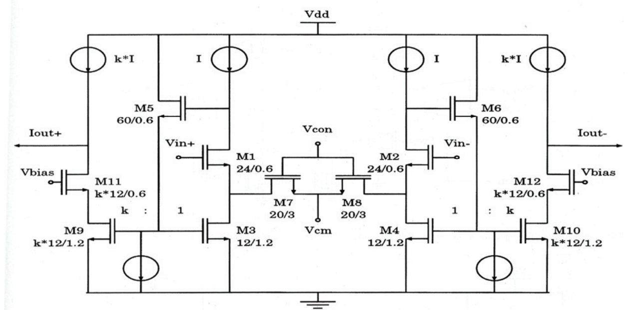
6th Order BiCMOS Continuous-time Filter & Second Order Equalizer for Disk Drive Read Channels



- Gm-C-opamp of the previous page used to build a 6th order filter for Disk Drive
- Filter consists of 3 Biquad with max. Q of 2 each
- Performance in the order of 40dB SNDR achieved for up to 20MHz corner frequency

Ref: C. Laber and P.Gray, "A 20MHz 6th Order BiCMOS Parasitic Insensitive Continuous-time Filter & Second Order Equalizer Optimized for Disk Drive Read Channels," *IEEE Journal of Solid State Circuits,* Vol. 28, pp. 462-470, April 1993.

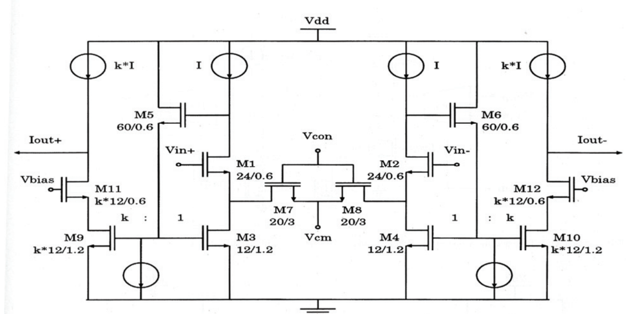
Gm-Cell
Source-Coupled Pair with Degeneration



– Gm-cell intended for low Q disk drive filter

Ref: I.Mehr and D.R.Welland, "A CMOS Continuous-Time Gm-C Filter for PRML Read Channel Applications at 150 Mb/s and Beyond", IEEE Journal of Solid-State Circuits, April 1997, Vol.32, No.4, pp. 499-513.

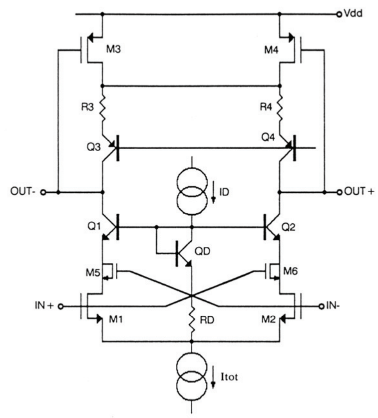
Gm-Cell
Source-Coupled Pair with Degeneration



– M7,8 operating in triode mode determine the overall gm of the cell
– Feedback provided by M5,6 maintains the gate-source voltage of M1,2 constant by forcing their current to be constant→ helps linearize *rds* of M7,8
– Current mirrored to the output via M9,10 with a factor of k
– Performance level of about 50dB SNDR at fcorner of 25MHz achieved

BiCMOS Gm-C Integrator

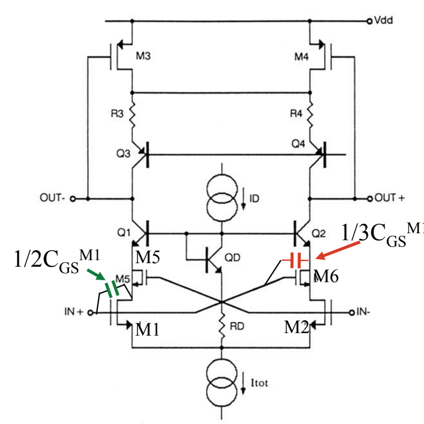
- Needs higher supply voltage compared to the previous design since quite a few devices are stacked vertically
- M1,2 → triode mode
- Q1,2 → hold V_{ds} of M1,2 constant
- Current ID used to tune filter critical frequency by varying V_{ds} of M1,2 and thus controlling *gm* of M1,2
- M3, M4 operate in triode mode and added to provide common-mode feedback



Ref: R. Alini, A. Baschirotto, and R. Castello, "Tunable BiCMOS Continuous-Time Filter for High-Frequency Applications," *IEEE Journal of Solid State Circuits,* Vol. 27, No. 12, pp. 1905-1915, Dec. 1992.

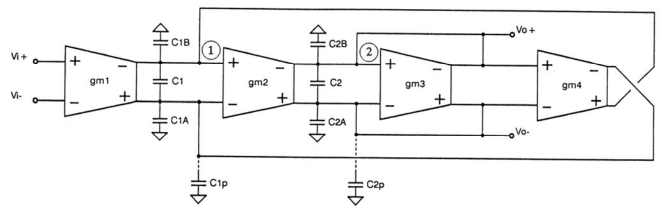
BiCMOS Gm-C Integrator

- M5 & M6 configured as capacitors- added to compensate for RHP zero due to Cgd of M1,2 (moves it to LHP) size of M5,6 → 1/3 of M1,2



Ref: R. Alini, A. Baschirotto, and R. Castello, "Tunable BiCMOS Continuous-Time Filter for High-Frequency Applications," *IEEE Journal of Solid State Circuits,* Vol. 27, No. 12, pp. 1905-1915, Dec. 1992.

BiCMOS Gm-C Filter For Disk-Drive Application



- Using the integrators shown in the previous page
- Biquad filter for disk drives
- *gm1=gm2=gm4=2gm3*
- *Q=2*
- Tunable from 8MHz to 32MHz

Ref: R. Alini, A. Baschirotto, and R. Castello, "Tunable BiCMOS Continuous-Time Filter for High-Frequency Applications," *IEEE Journal of Solid State Circuits,* Vol. 27, No. 12, pp. 1905-1915, Dec. 1992.

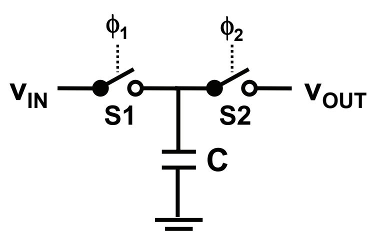
Summary
Continuous-Time Filters

- Opamp RC filters
  - Good linearity → High dynamic range (60-90dB)
  - Only discrete tuning possible
  - Medium usable signal bandwidth (<10MHz)
- Opamp MOSFET-C
  - Linearity compromised (typical dynamic range 40-60dB)
  - Continuous tuning possible
  - Low usable signal bandwidth (<5MHz)
- Opamp MOSFET-RC
  - Improved linearity compared to Opamp MOSFET-C (D.R. 50-90dB)
  - Continuous tuning possible
  - Low usable signal bandwidth (<5MHz)
- Gm-C
  - Highest frequency performance (at least an order of magnitude higher compared to the rest <100MHz)
  - Dynamic range not as high as Opamp RC but better than Opamp MOSFET-C (40-70dB)

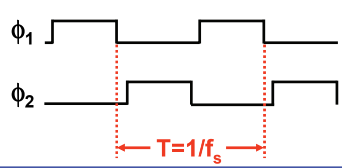
Switched-Capacitor Filters Today

- Emulating resistor via switched-capacitor network
- 1st order switched-capacitor filter
- Switch-capacitor filter considerations:
  - Issue of aliasing and how to avoid it
  - Tradeoffs in choosing sampling rate
  - Effect of sample and hold
  - Switched-capacitor filter electronic noise

Switched-Capacitor Resistor



- Capacitor C is the "switched capacitor"
- Non-overlapping clocks ϕ_1 and ϕ_2 control switches S1 and S2, respectively
- v_{IN} is sampled at the falling edge of ϕ_1
  - Sampling frequency f_S
- Next, ϕ_2 rises and the voltage across C is transferred to v_{OUT}
- Why does this behave as a resistor?



Switched-Capacitor Resistors

- Charge transferred from v_{IN} to v_{OUT} during each clock cycle is:

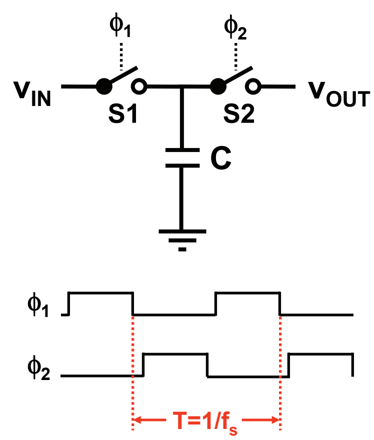
$$Q = C(v_{IN} - v_{OUT})$$

- Average current flowing from v_{IN} to v_{OUT} is:

$$i = Q/t = Q \cdot f_s$$

Substituting for Q:

$$i = f_S C(v_{IN} - v_{OUT})$$



Switched-Capacitor Resistors

$$i = f_S C(v_{IN} - v_{OUT})$$

With the current through the switched-capacitor resistor proportional to the voltage across it, the equivalent "switched capacitor resistance" is:

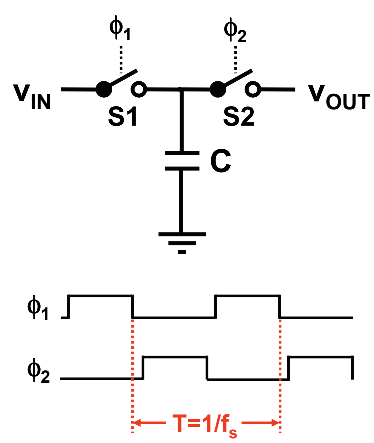
$$R_{eq} = \frac{V_{IN} - V_{OUT}}{i} = \frac{1}{f_S C}$$

Example:

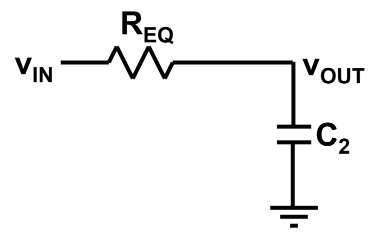
$f_S = 100KHz, C = 0.1pF$

$\rightarrow R_{eq} = 100Mega\Omega$

Note: Can build large time-constant in small area



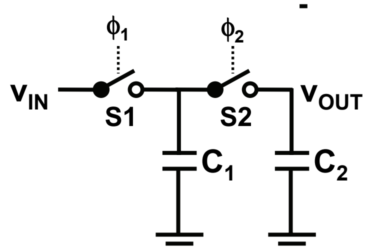
Switched-Capacitor Filter



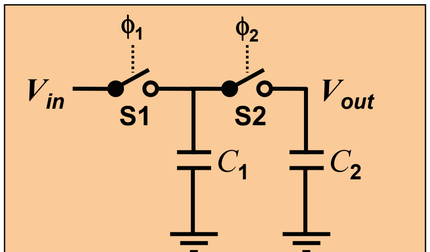
- Let's build a "switched- capacitor " filter …
- Start with a simple RC LPF
- Replace the physical resistor by an equivalent switched-capacitor resistor
- 3-dB bandwidth:

$$\omega_{-3dB} = \frac{1}{R_{eq}C_2} = f_s \times \frac{C_1}{C_2}$$

$$f_{-3dB} = \frac{1}{2\pi} f_s \times \frac{C_1}{C_2}$$

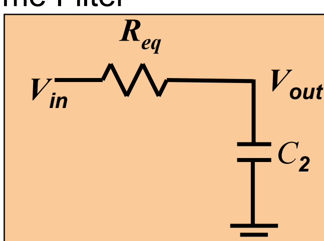


Switched-Capacitor Filter Advantage versus Continuous-Time Filter



$$f_{-3dB} = \frac{1}{2\pi} f_s \times \frac{C_1}{C_2}$$

- Corner freq. proportional to:
  System clock (accurate to few ppm)
  C ratio accurate → < 0.1%



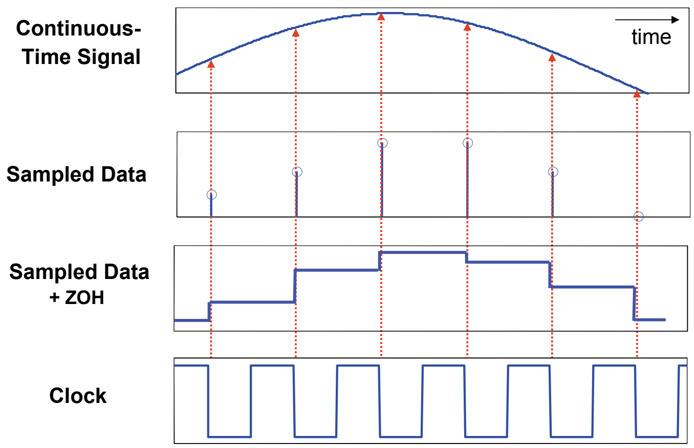
$$f_{-3dB} = \frac{1}{2\pi} \times \frac{1}{R_{eq}C_2}$$

- Corner freq. proportional to:
  Absolute value of Rs & Cs
  Poor accuracy → 20 to 50%

Main advantage of SC filters → inherent corner frequency accuracy

Typical Sampling Process

Continuous-Time(CT) ⇒ Sampled Data (SD)

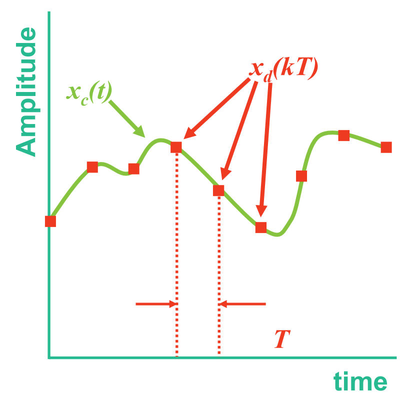


Uniform Sampling

Nomenclature:

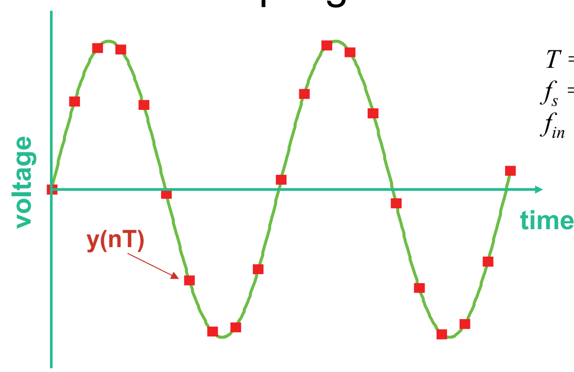
Continuous time signal $x_c(t)$
Sampling interval T
Sampling frequency $f_s = 1/T$
Sampled signal $x_d(kT) = x(k)$

- Problem: Multiple continuous time signals can yield exactly the same discrete time signal
- Let's look at samples taken at 1µs intervals of several sinusoidal waveforms …



Note: Samples are the waveform values at kT instances and undefined in between

Sampling Sine Waves



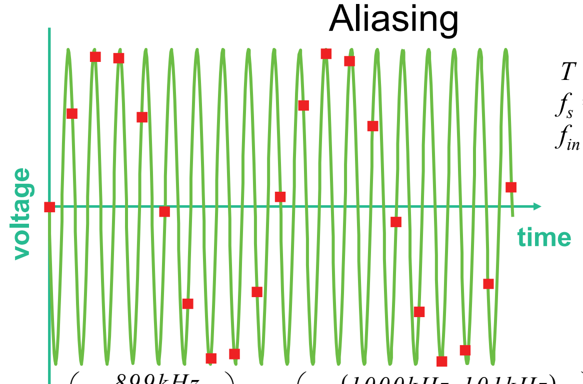
$T = 1\mu s$
$f_s = 1/T = 1MHz$
$f_{in} = 101kHz$

$v(t) = cos\ (2\pi.f_{in}.t)$

Sampled-data domian $\rightarrow t \rightarrow n.T$ or $t \rightarrow n/f_s$

$$v(n) = cos\left(2\pi.\frac{f_{in}}{f_s}.n\right) = cos\left(2\pi.\frac{101kHz}{1MHz}.n\right)$$

Sampling Sine Waves
Aliasing

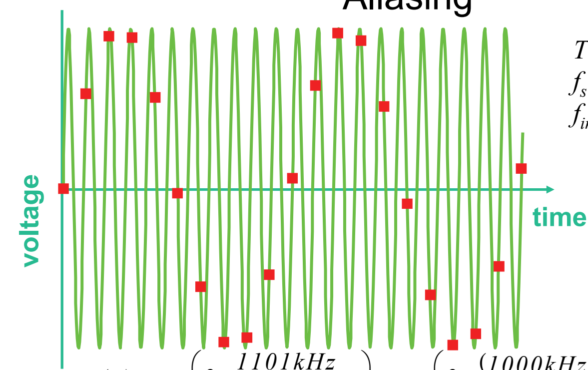


$T = 1\mu s$
$f_s = 1/T = 1MHz$
$f_{in} = 899kHz$

$$v(n) = cos\left(2\pi.\frac{899kHz}{1MHz}.n\right) = cos\left(2\pi.\frac{(1000kHz\text{-}101kHz)}{1MHz}.n\right) = cos\left(2\pi - \frac{101kHz}{1MHz}.n\right)$$

$$= cos\left(2\pi.\frac{101kHz}{1MHz}.n\right)$$

Sampling Sine Waves
Aliasing



$T = 1\mu s$
$f_s = 1/T = 1MHz$
$f_{in} = 1101kHz$

$$v(n) = cos\left(2\pi.\frac{1101kHz}{1MHz}.n\right) = cos\left(2\pi.\frac{(1000kHz+101kHz)}{1MHz}.n\right)$$

$$= cos\left(2\pi.\frac{101kHz}{1MHz}.n\right)$$

Sampling Sine Waves

<u>Problem:</u>

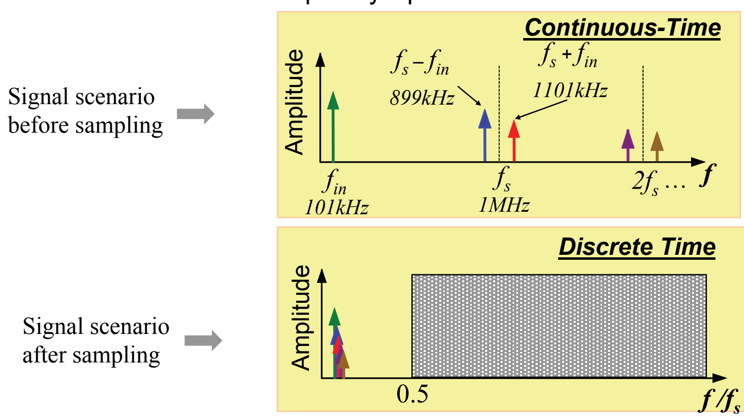
Identical samples for:

$$v(t) = cos\ [2\pi f_{in} t\ ]$$
$$v(t) = cos\ [2\pi (f_{in} + n.f_s) t\ ]$$
$$v(t) = cos\ [2\pi (f_{in} - n.f_s) t\ ]$$

* (n-integer)

→Multiple continuous time signals can yield exactly the same discrete time signal

Sampling Sine Waves
Frequency Spectrum



Key point: Signals @ $nf_S \pm f_{max\_signal}$ fold back into band of interest→Aliasing

Aliasing

- Multiple continuous time signals can produce identical series of samples
- The folding back of signals from $nf_s \pm f_{sig}$ (n integer) down to f_{fin} is called <u>aliasing</u>
  - Sampling theorem: $f_s > 2f_{max\_Signal}$
- If aliasing occurs, no signal processing operation downstream of the sampling process can recover the original continuous time signal

How to Avoid Aliasing?

- Must obey sampling theorem:

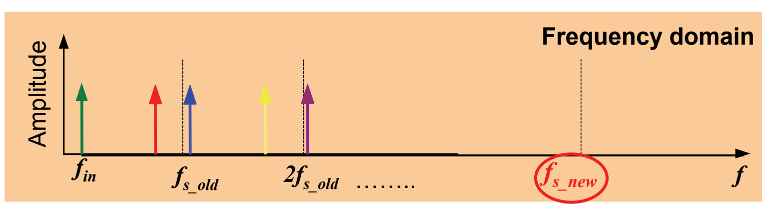
$$f_{max\text{-}Signal} < f_s/2$$

*Note:

Minimum sampling rate of $f_s = 2x f_{max\text{-}Signal}$ is called Nyquist rate

- Two possibilities:
  1. Sample fast enough to cover all spectral components, including "parasitic" ones outside band of interest
  2. Limit f_{max_Signal} through filtering → attenuate out-of-band components prior to sampling

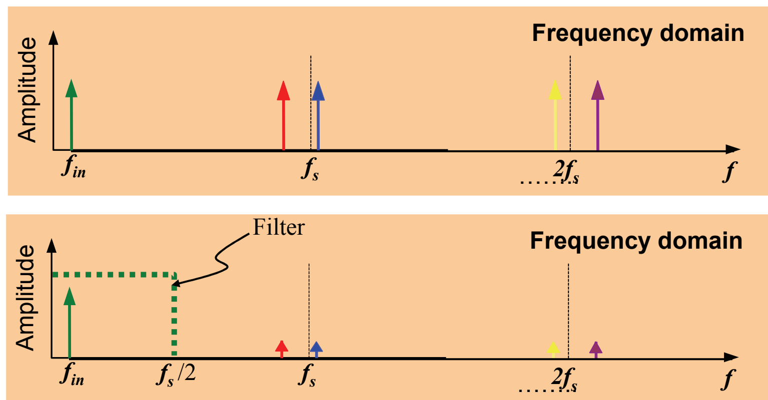
How to Avoid Aliasing?
1-Sample Fast



Push sampling frequency to *x2* of the highest frequency signal to cover all unwanted signals as well as wanted signals

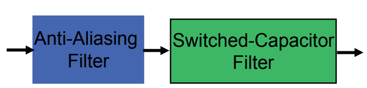
→ In vast majority of cases <u>not practical</u>

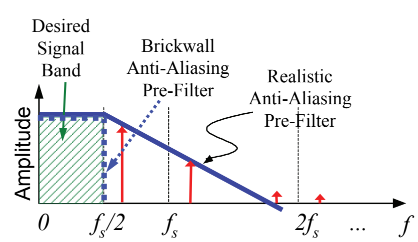
How to Avoid Aliasing?
2-Filter Out-of-Band Signal Prior to Sampling



Pre-filter signal to eliminate/attenuate signals above $f_s/2$- then sample

Anti-Aliasing Filter Considerations

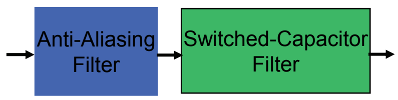


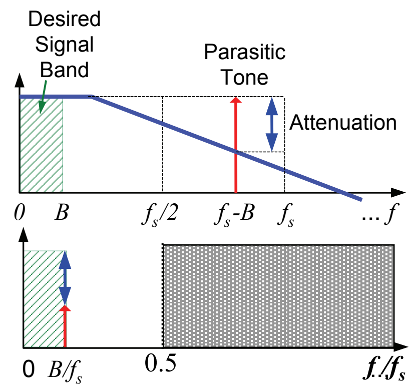


Case1- $B = f_{sig}^{max} = f_s/2$

- Non-practical since an extremely high order anti-aliasing filter (close to an ideal brickwall filter) is required
- Practical anti-aliasing filter →Non-zero filter "transition band"
- In order to make this work, we need to sample much faster than 2x the signal bandwidth
  →"Oversampling"

Practical Anti-Aliasing Filter



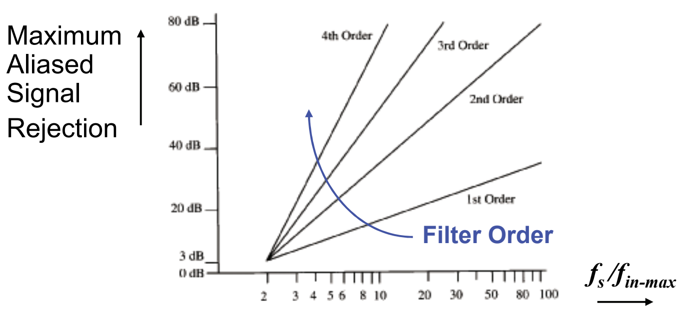


Case2 - $B = f_{max\_Signal} << f_s/2$

- More practical anti-aliasing filter
- Preferable to have an anti-aliasing filter with:
  - →The lowest order possible
  - →No frequency tuning required (if frequency tuning is required then why use switched-capacitor filter, just use the prefilter!?)

Tradeoff

Oversampling Ratio versus Anti-Aliasing Filter Order

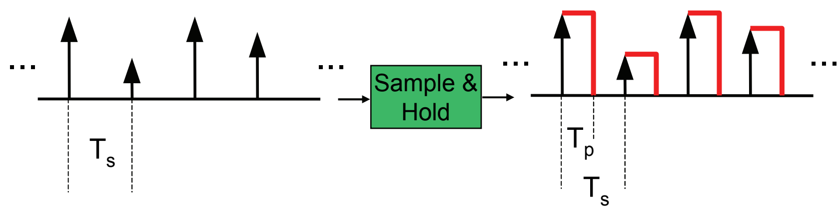


* *Assumption→ anti-aliasing filter is Butterworth type (not a necessary requirement)*

→Tradeoff: Sampling speed versus anti-aliasing filter order

Ref: R. v. d. Plassche, *CMOS Integrated Analog-to-Digital and Digital-to-Analog Converters*, 2nd ed., Kluwer publishing, 2003, p.41]

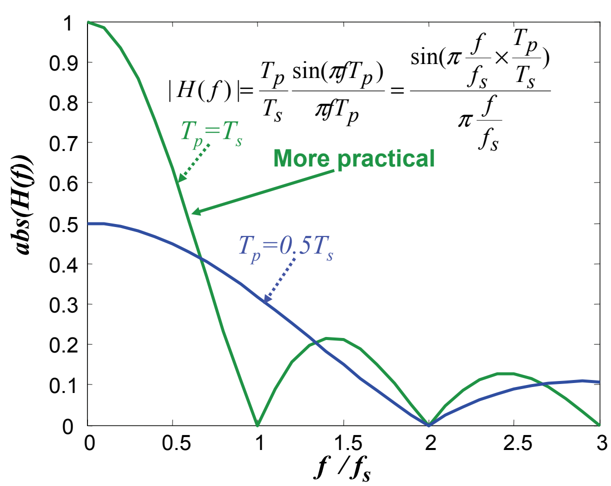
Effect of Sample & Hold



•Using the Fourier transform of a rectangular impulse:

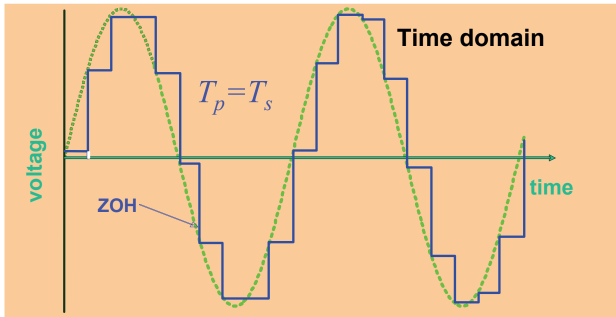
$$|H(f)| = \frac{T_p}{T_s}\frac{\sin(\pi f T_p)}{\pi f T_p}$$

Effect of Sample & Hold on Frequency Response

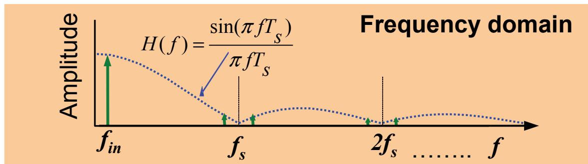


Sample & Hold Effect
(Reconstruction of Analog Signals)

$T_p = T_s$



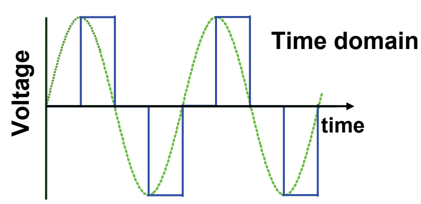
Magnitude droop due to *sinx/x* effect



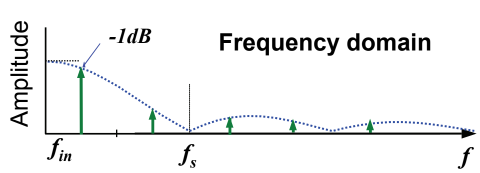
Sample & Hold Effect
(Reconstruction of Analog Signals)

Magnitude droop due to *sinx/x* effect:

Case 1) $f_{sig} = f_s/4$



Droop= *-1dB*

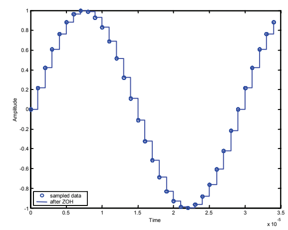


Sample & Hold Effect
(Reconstruction of Analog Signals)

Magnitude droop due to ***sinx/x*** effect:

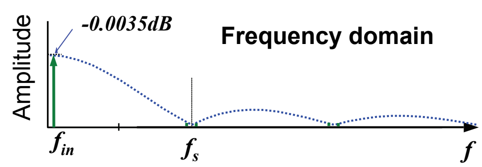
Case 2)
$f_{sig}=f_s/32$

Time domain



Droop= *-0.0035dB*

→ High oversampling ratio desirable



Sampling Process Including S/H