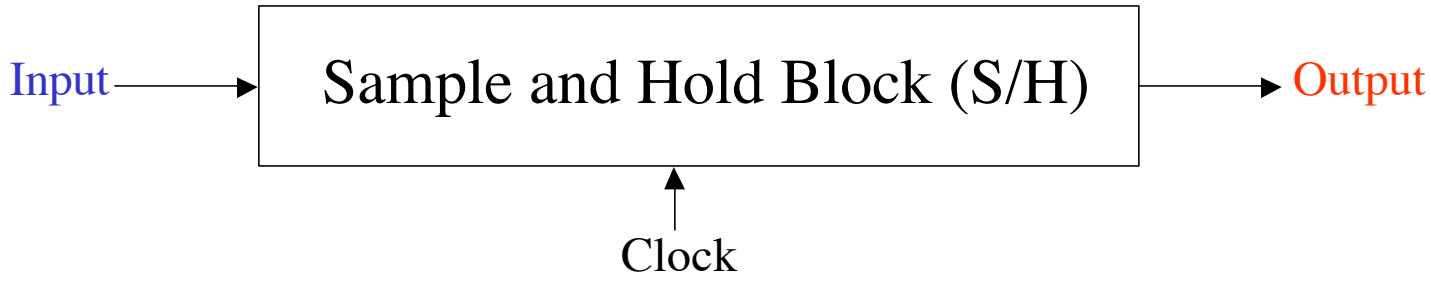
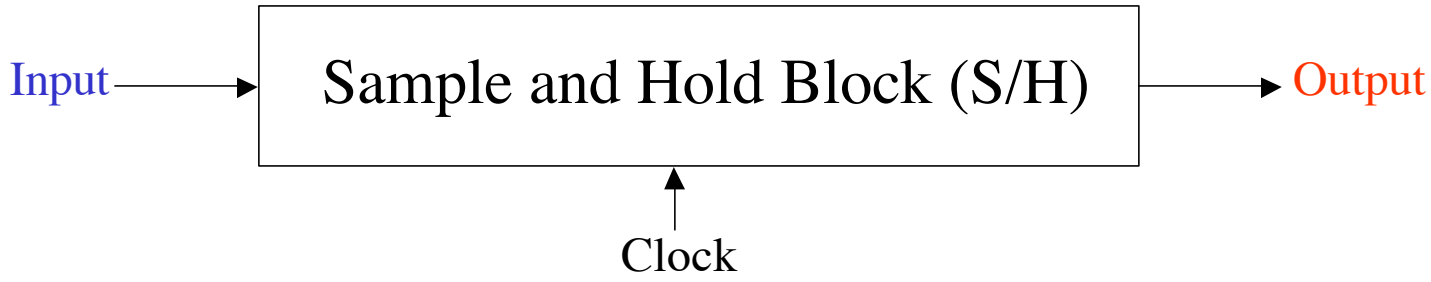
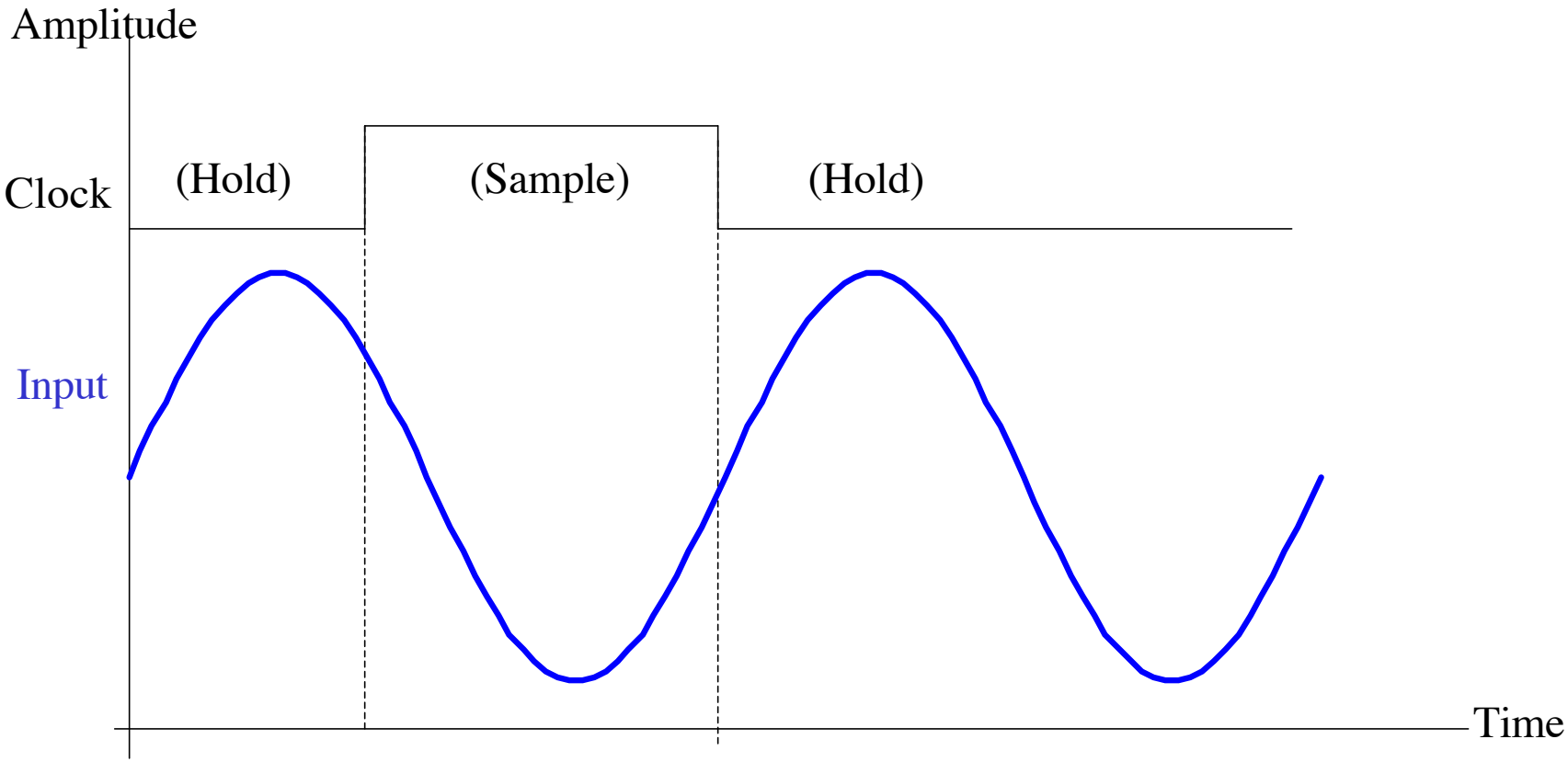
Sample and Hold Elements

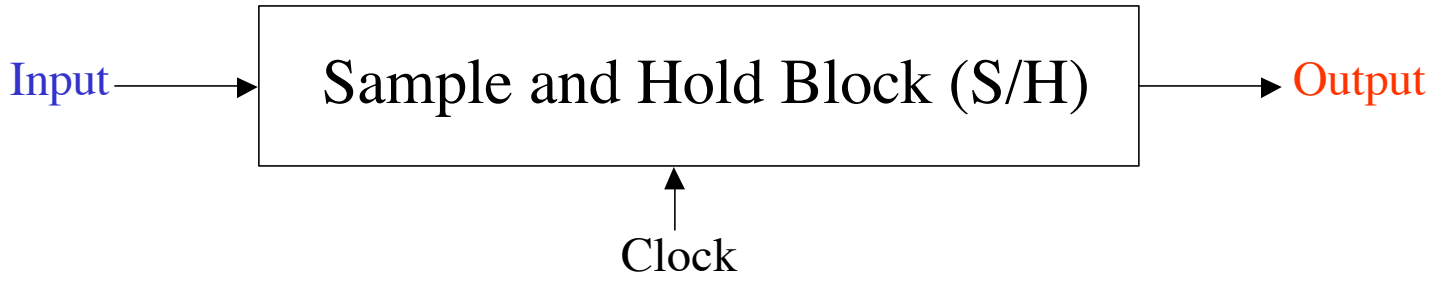


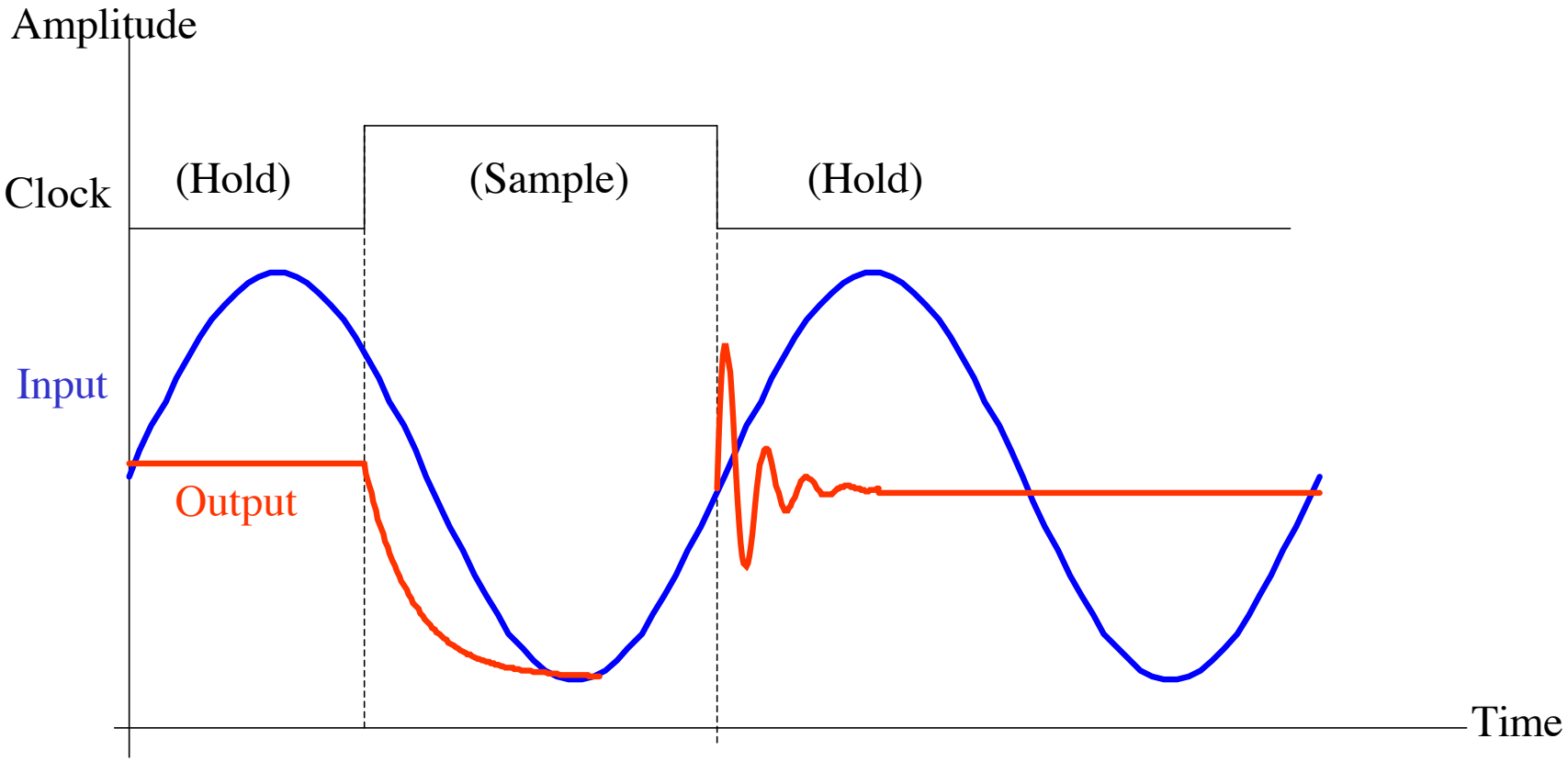
Sample and Hold Elements



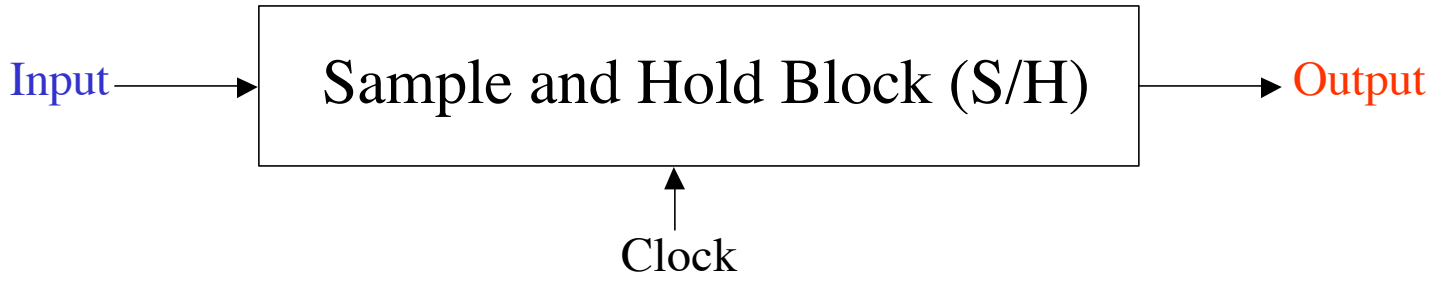


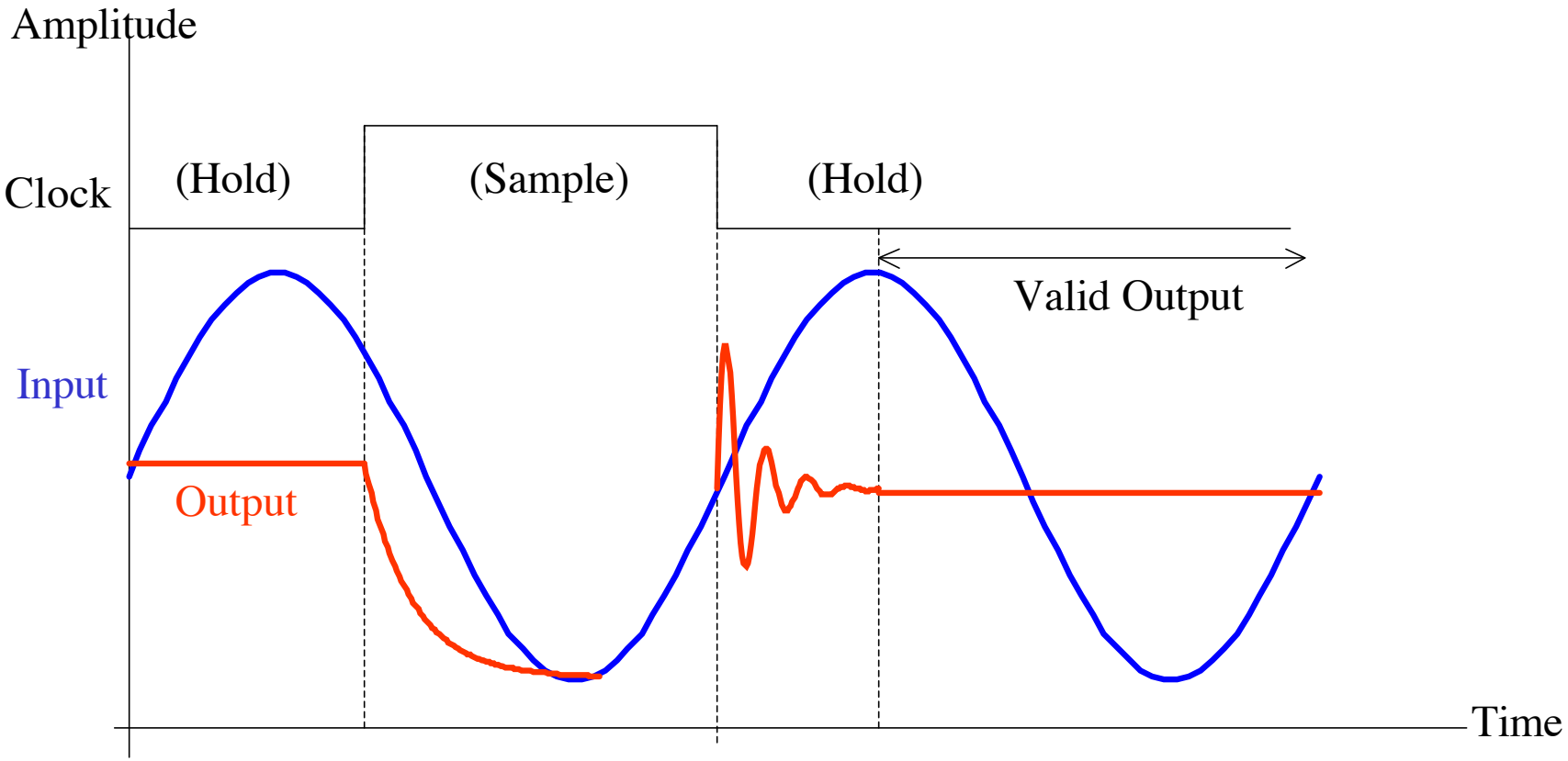
Sample and Hold Elements



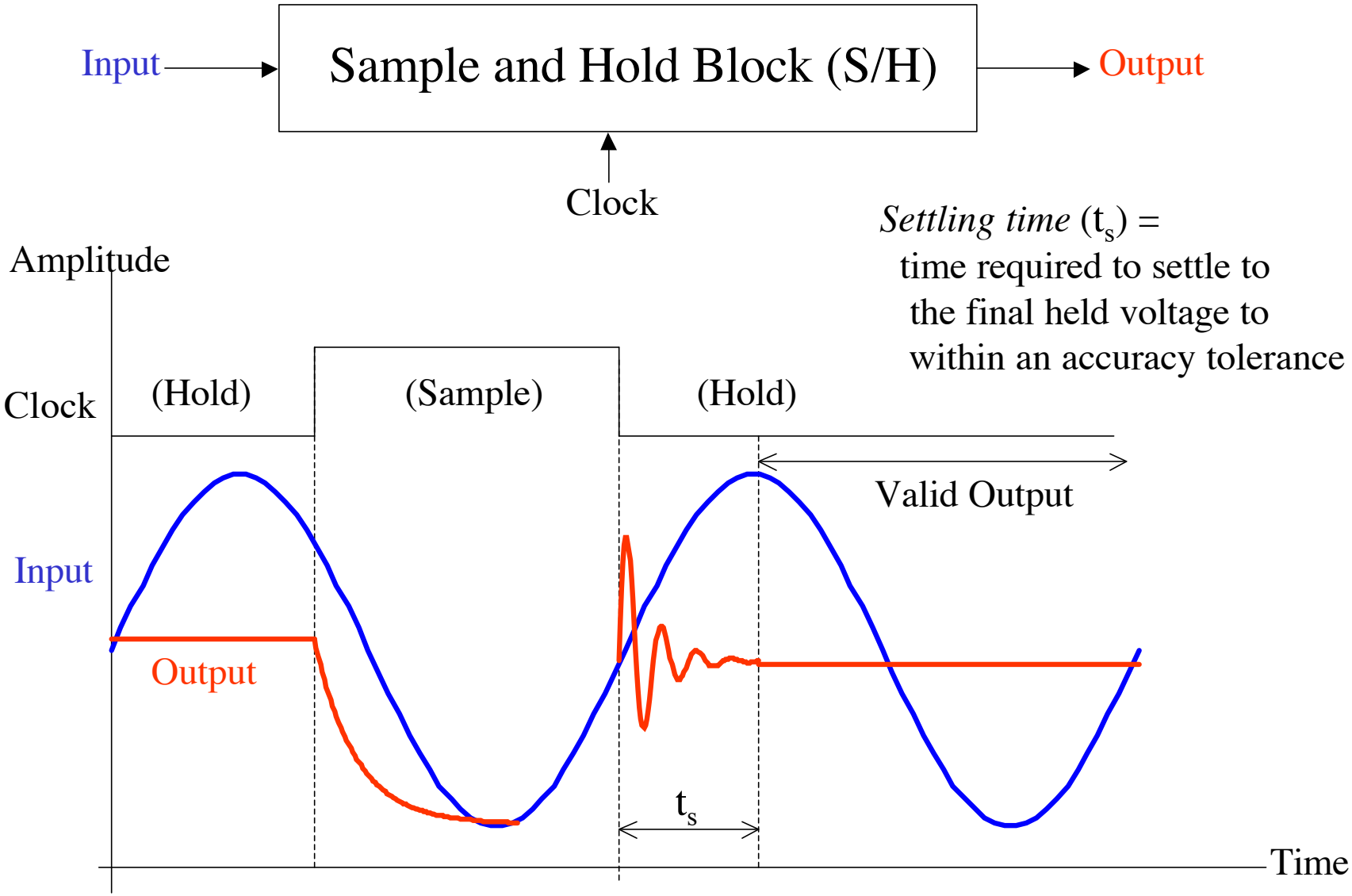


Sample and Hold Elements

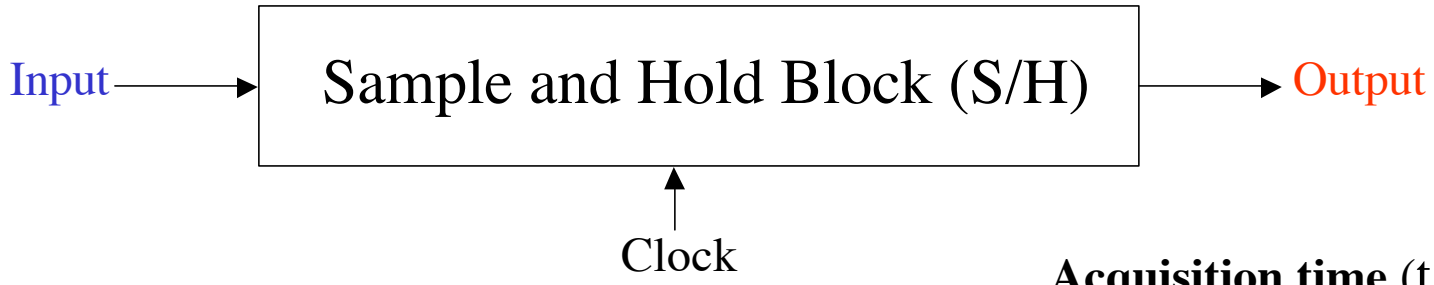




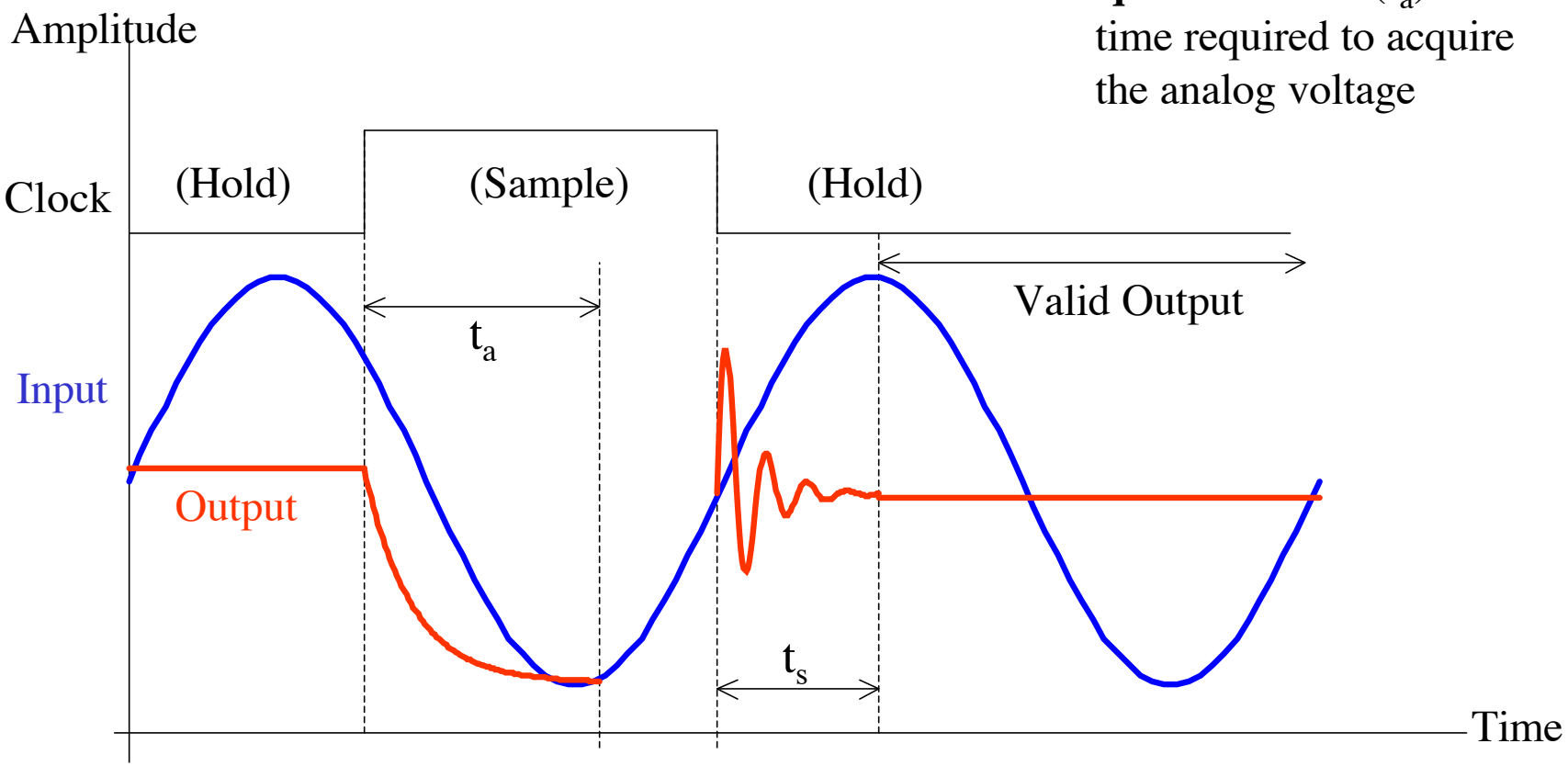
Sample and Hold Elements



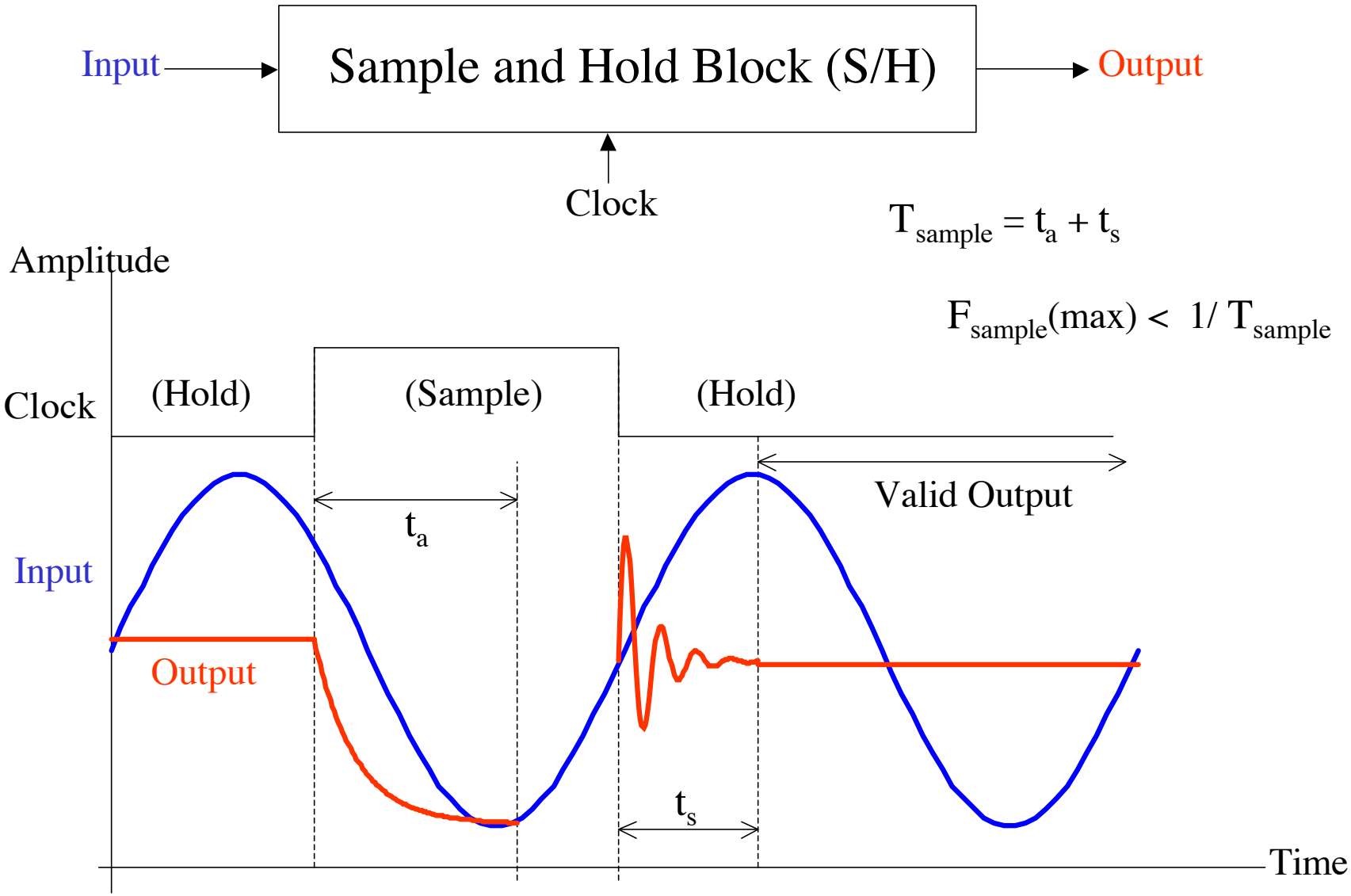
Sample and Hold Elements



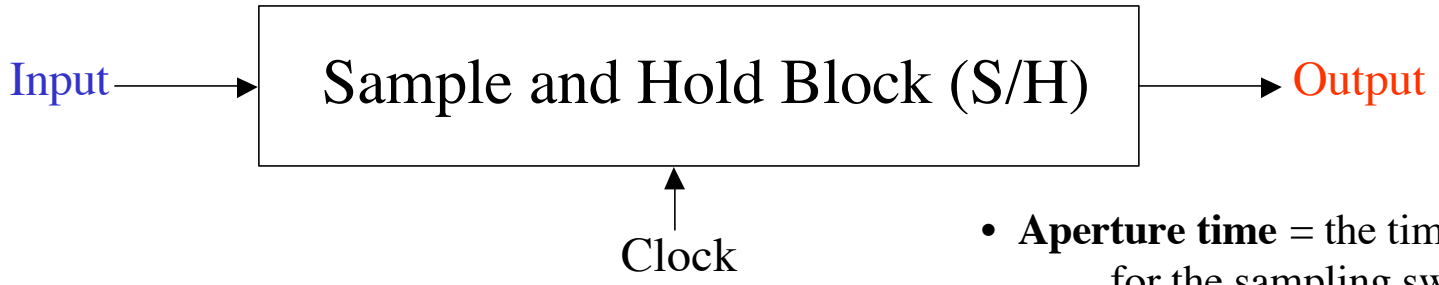
Acquisition time (t_a) = time required to acquire the analog voltage



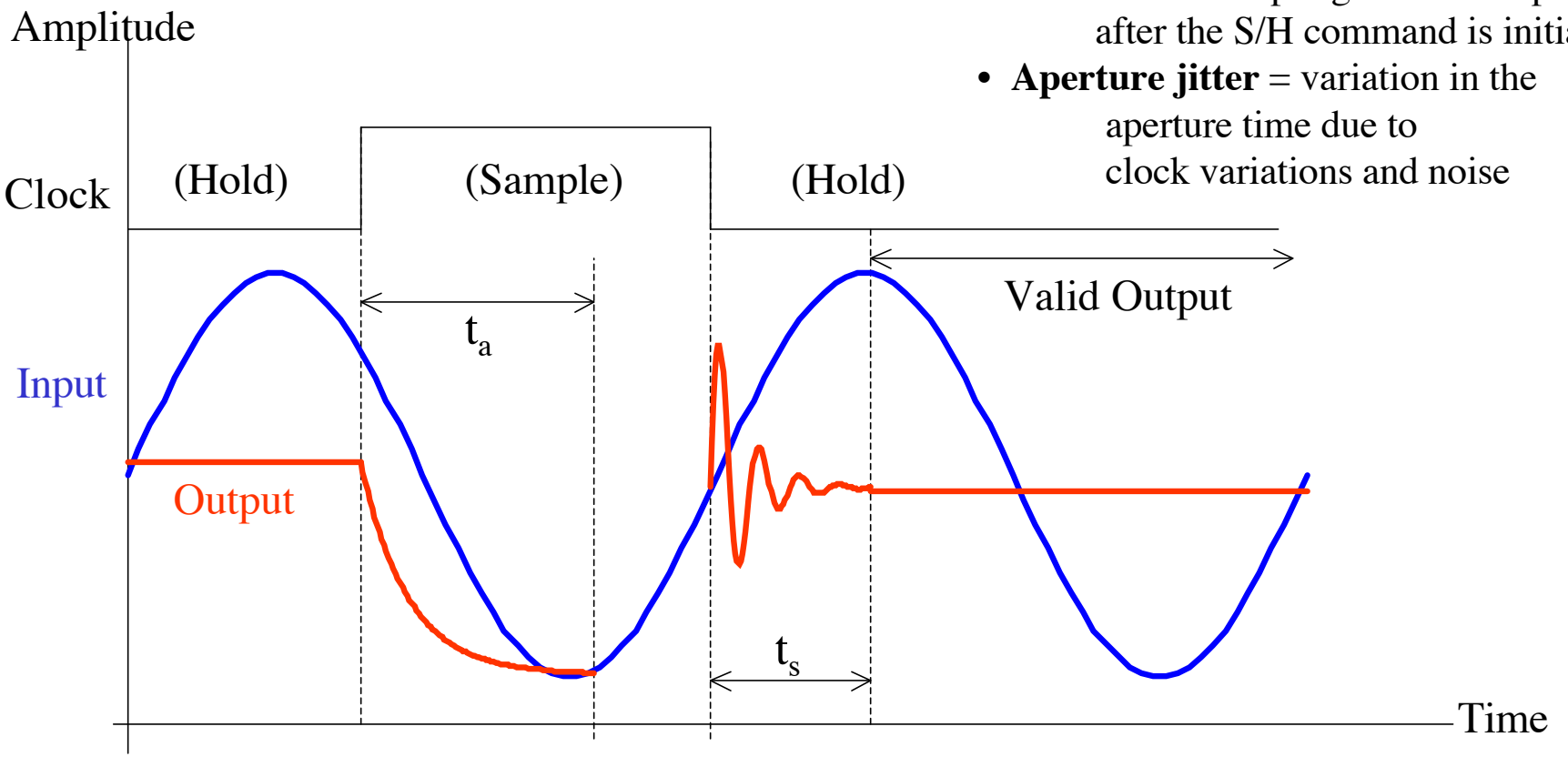
Sample and Hold Elements



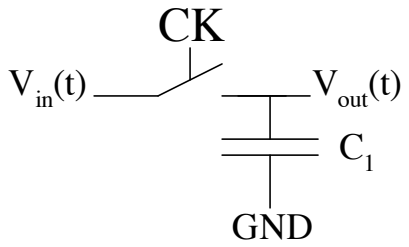
Sample and Hold Elements



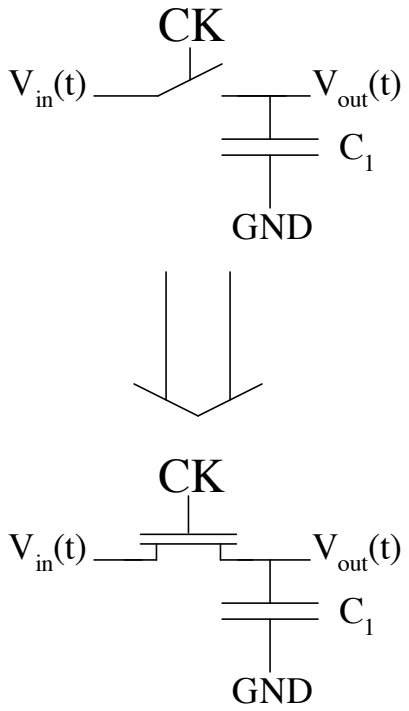
- **Aperture time** = the time required for the sampling switch to open after the S/H command is initiated
- **Aperture jitter** = variation in the aperture time due to clock variations and noise



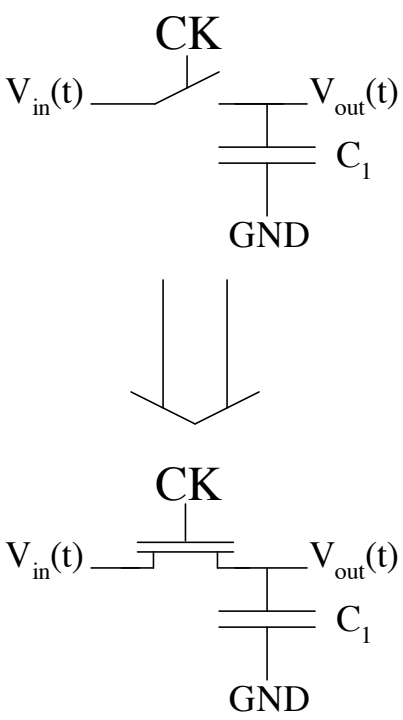
Basic Sample and Hold Element



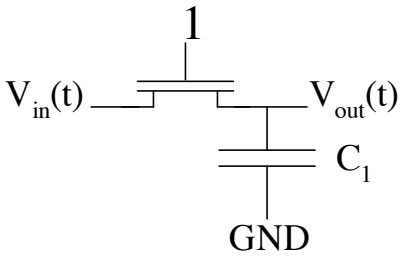
Basic Sample and Hold Element



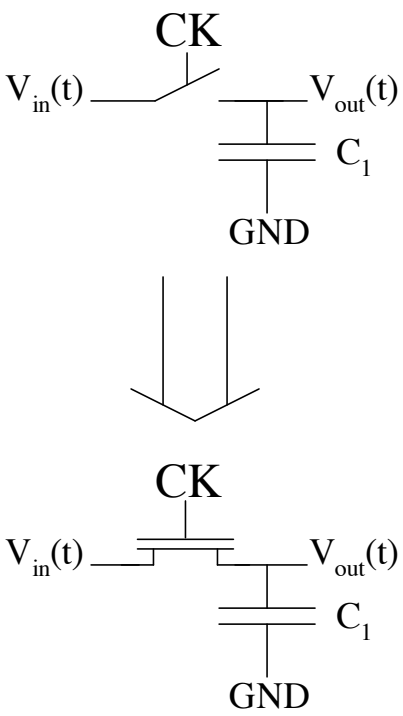
Basic Sample and Hold Element



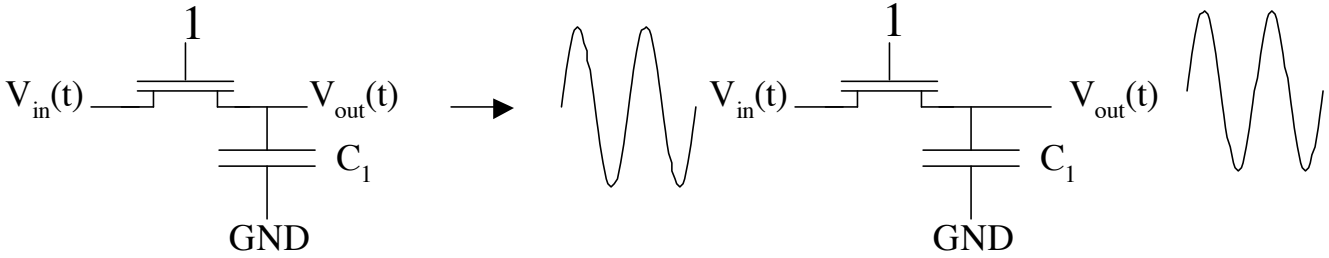
CK = 1 (Vdd)



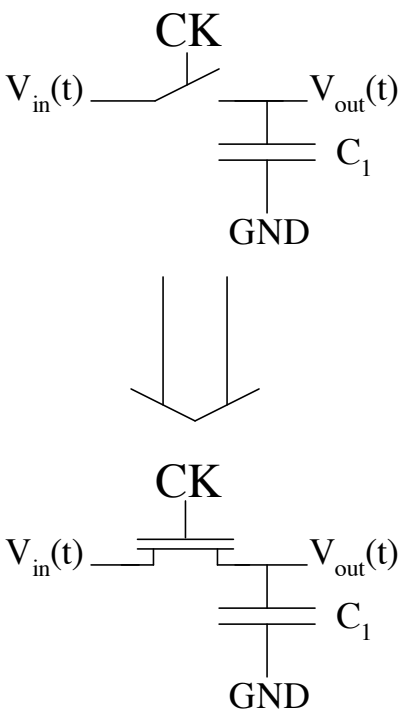
Basic Sample and Hold Element



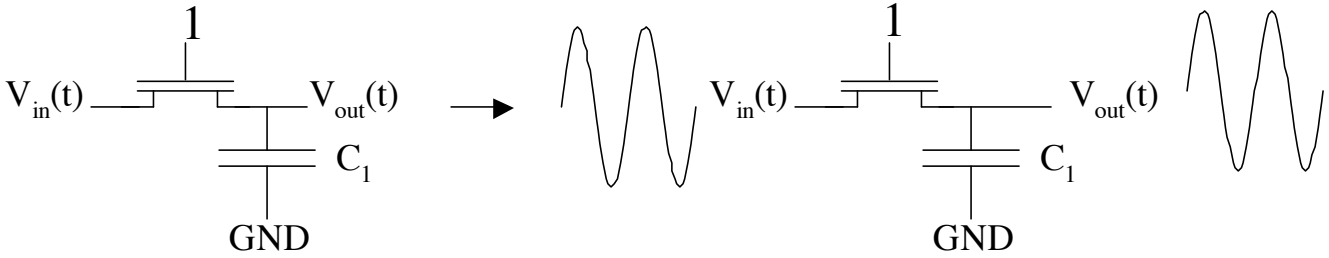
CK = 1 (Vdd)



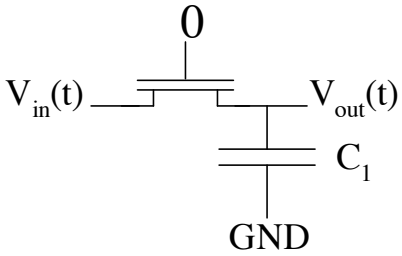
Basic Sample and Hold Element



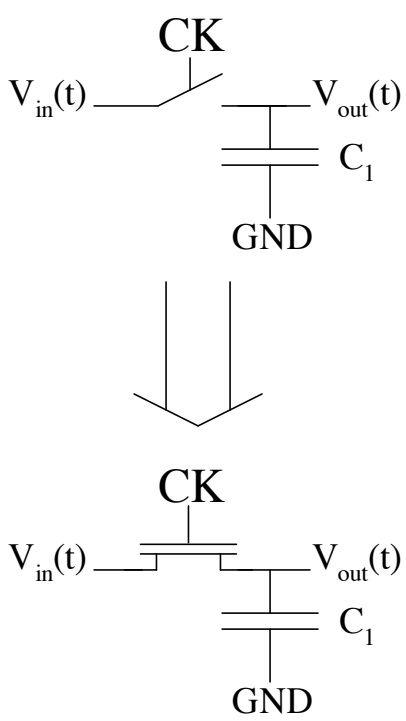
CK = 1 (Vdd)



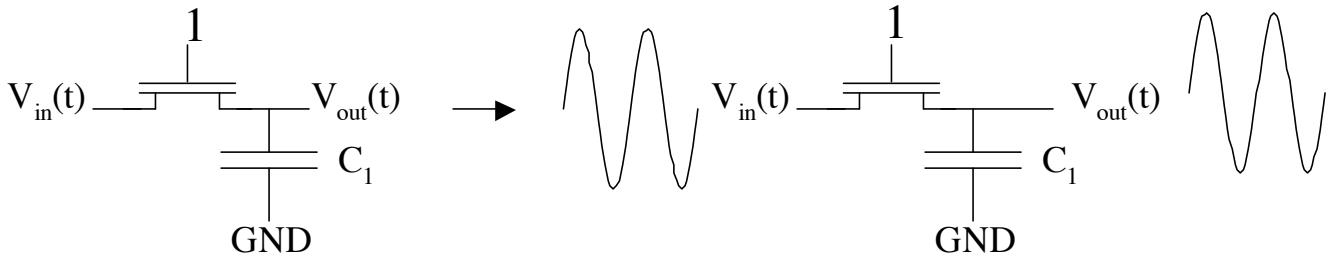
CK = 0 (Vdd)



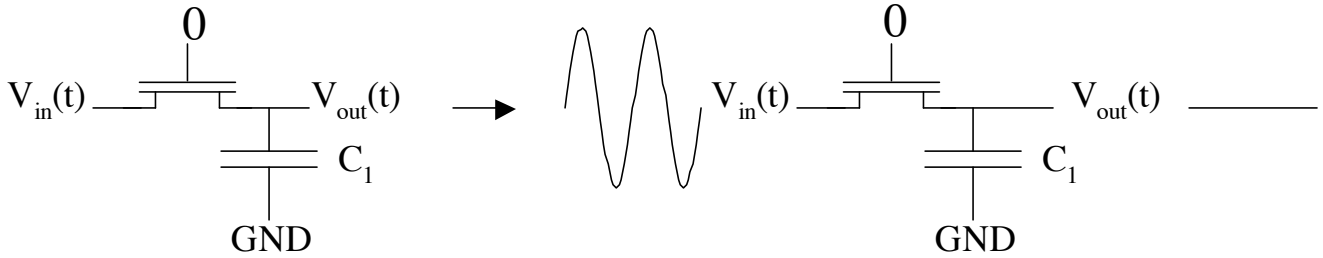
Basic Sample and Hold Element



CK = 1 (Vdd)

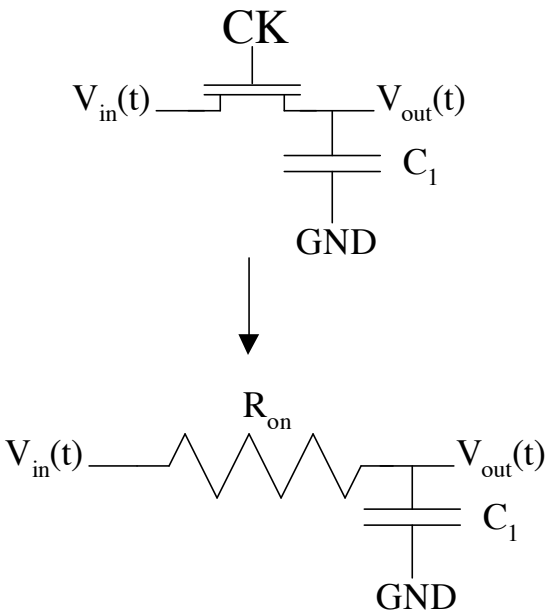


CK = 0 (Vdd)



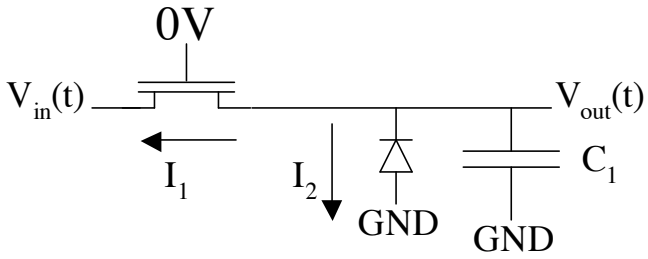
Acquisition and Hold Time

Acquisition Time



but R_{on} is not a constant….

Hold Time

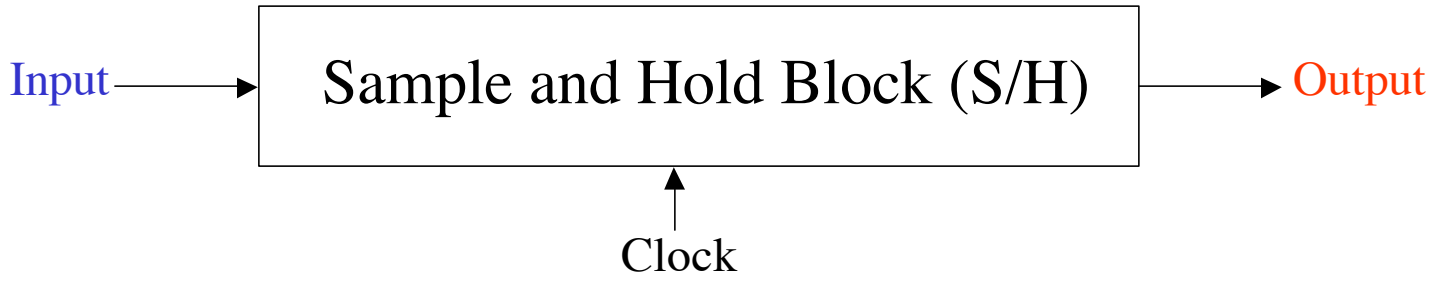


$I_2(t)$: Leakage through the reversed-biased pn junction
Typically 1fA to 100fA (dark)

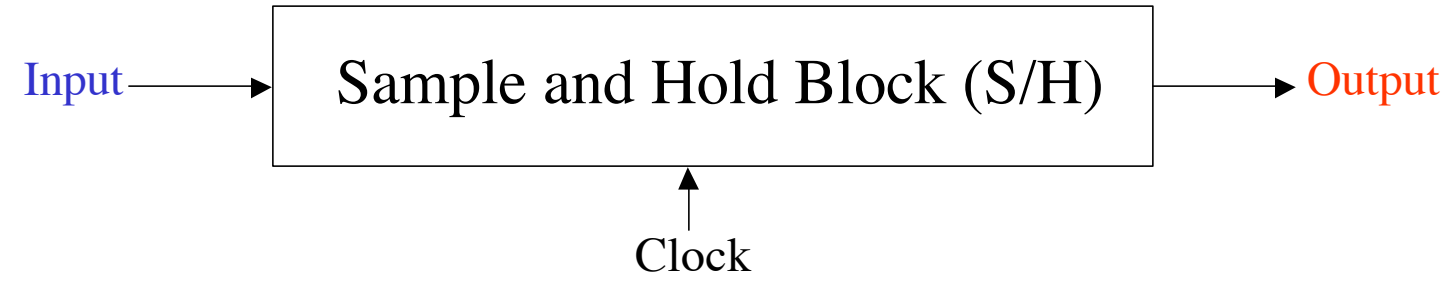
$I_1(t)$: Leakage through the MOS transistor
Can be negligable with correct biasing

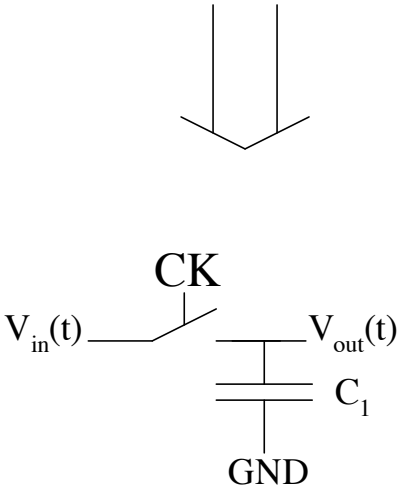
C_1	Hold time (1mV drop) with $I_1(t)$ = 10fA
10pF	1s
1pF	100ms
100fF	10ms
10fF	1ms

Basic S/H elements

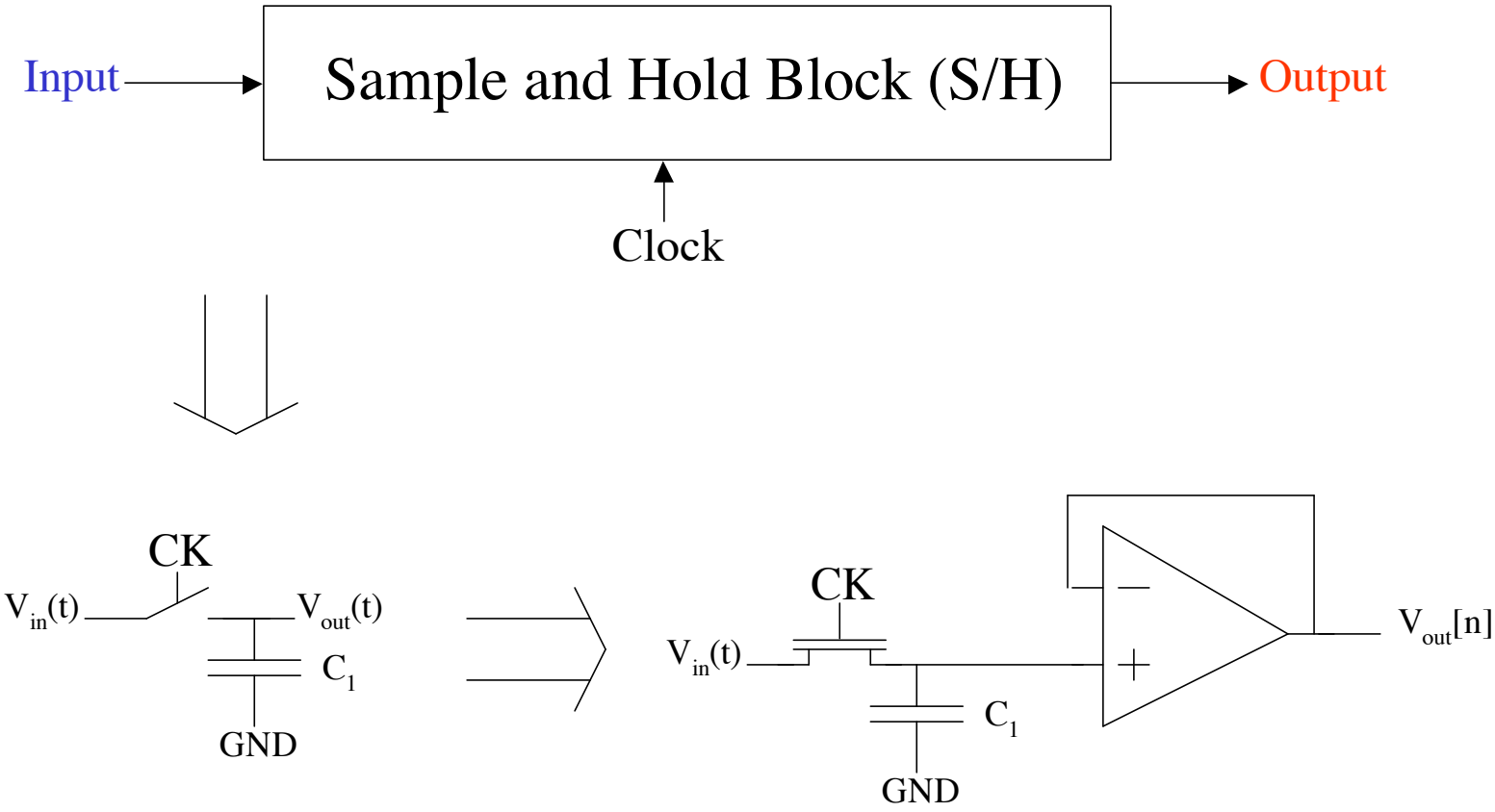


Basic S/H elements



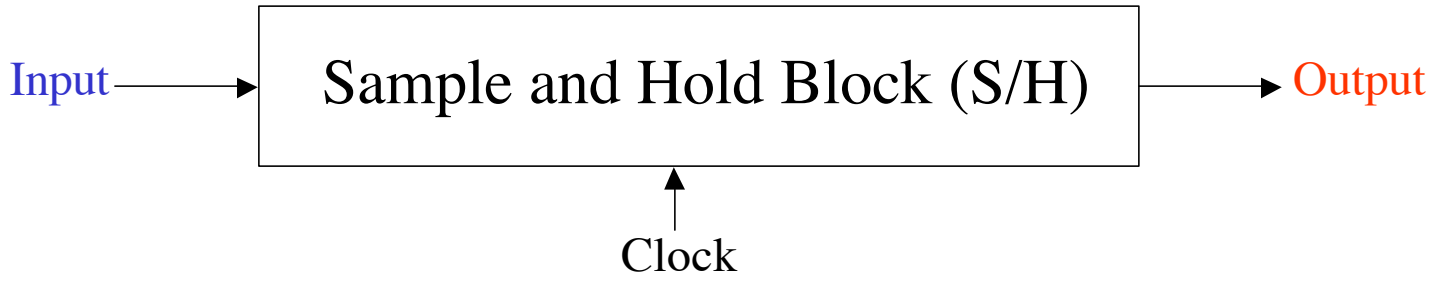


Basic S/H elements

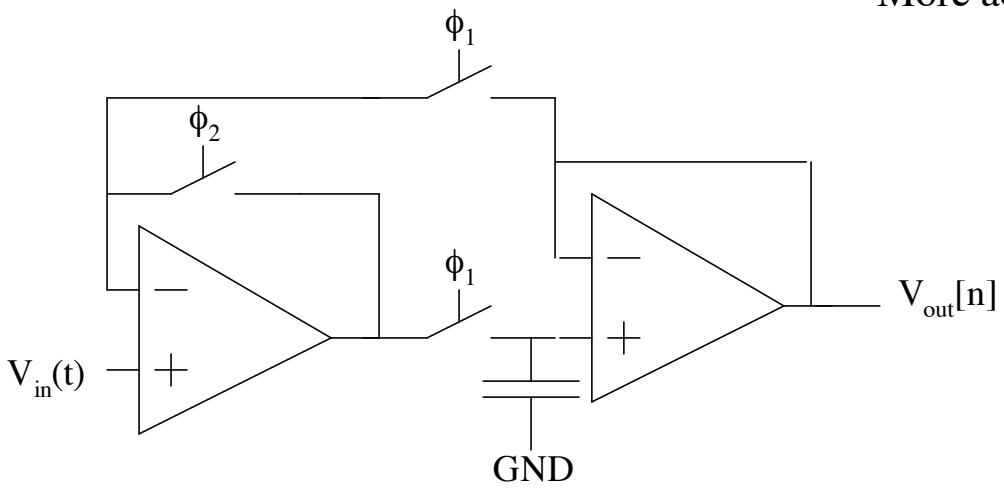


Would use a buffer to drive loads
that are not purely capacitive

S/H elements



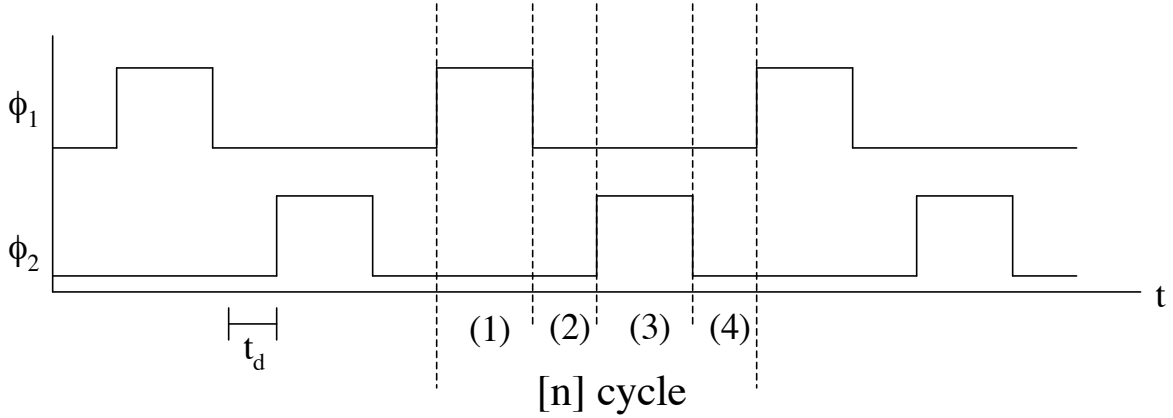
More accurate, but slower



ϕ_1 and ϕ_2 are non-overlapping clocks

Non-Overlapping Clocks

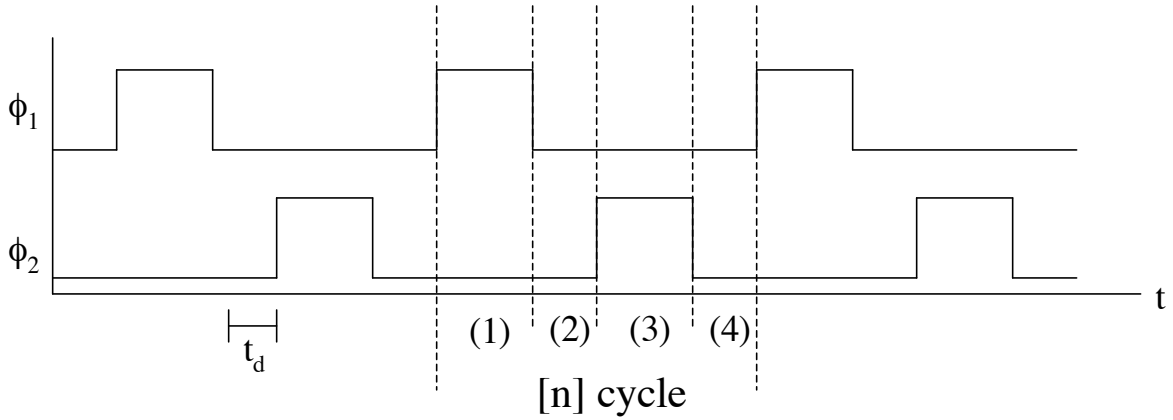
We will always be using non-overlapping clocks; therefore, we want a waveform like



We effectively have four phases.

Non-Overlapping Clocks

We will always be using non-overlapping clocks; therefore, we want a waveform like



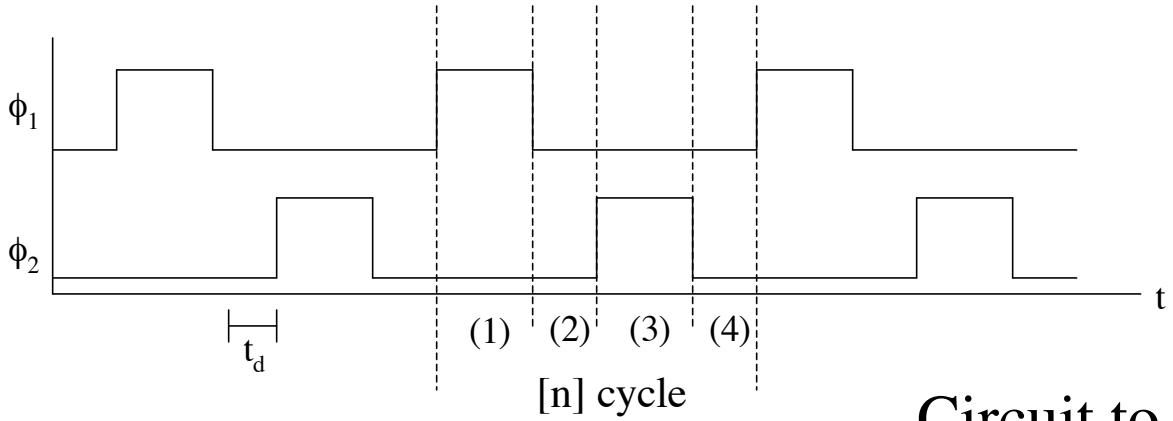
We effectively have four phases.

Would want t_d as small as possible for proper operation

We will also assume that the input is held constant through the entire $[n]^{th}$ cycle

Non-Overlapping Clocks

We will always be using non-overlapping clocks; therefore, we want a waveform like

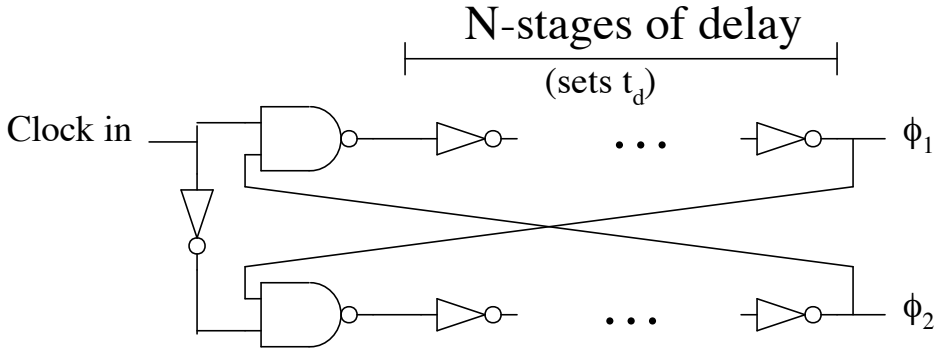


We effectively have four phases.

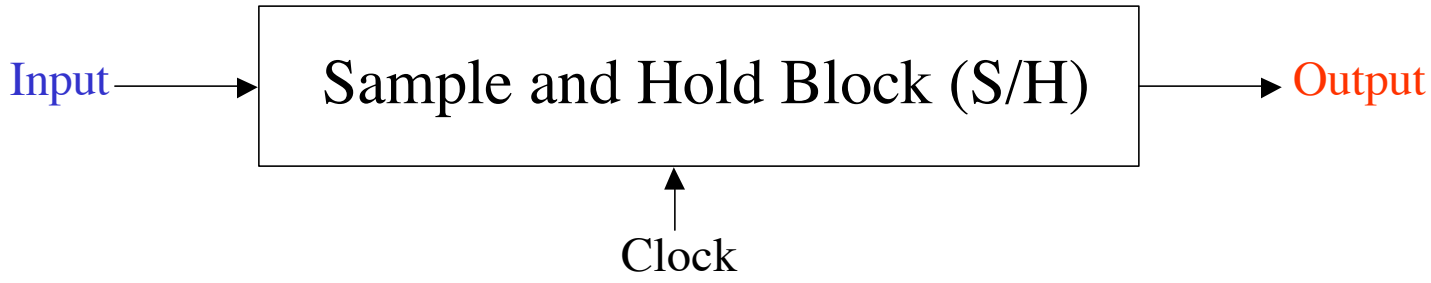
Would want t_d as small as possible for proper operation

We will also assume that the input is held constant through the entire [n]th cycle

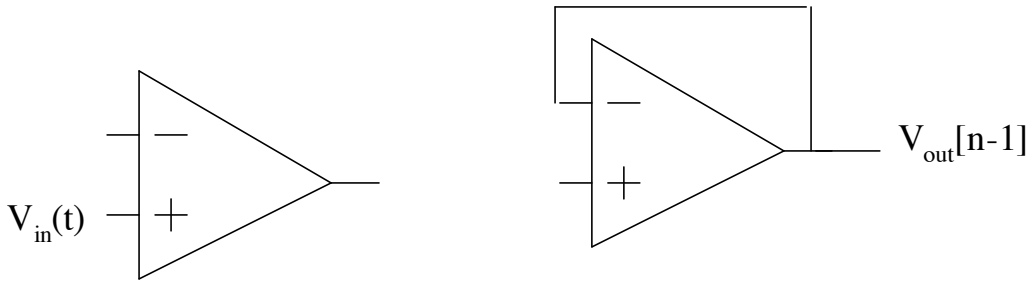
Circuit to generate waveform



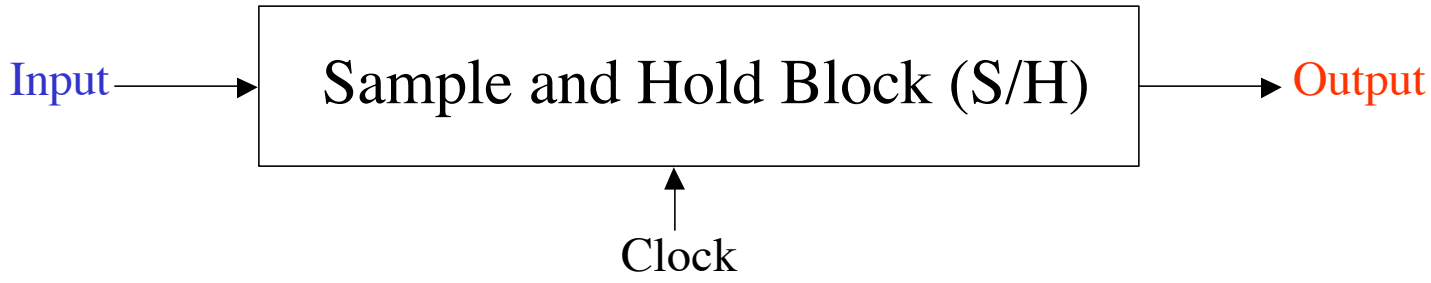
S/H elements



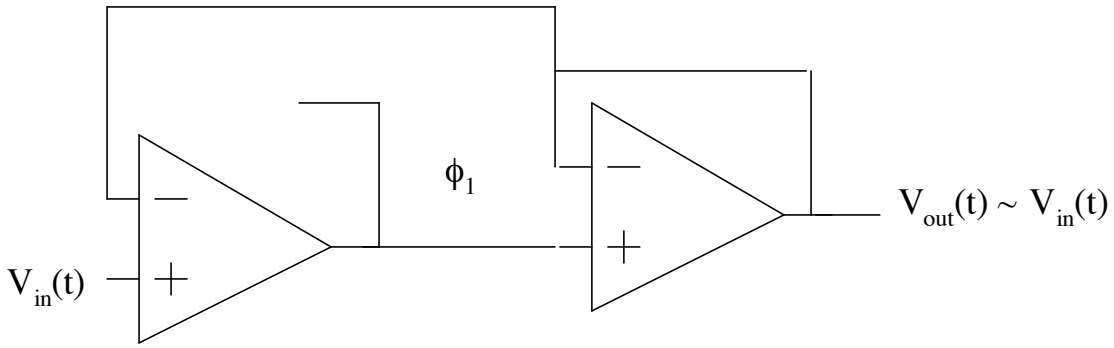
Initial Phase ($\phi_1, \phi_2 = 0$)



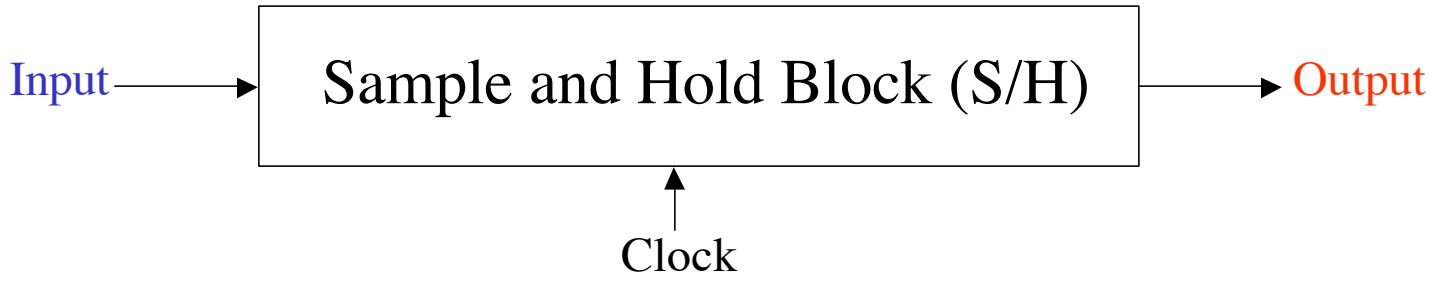
S/H elements



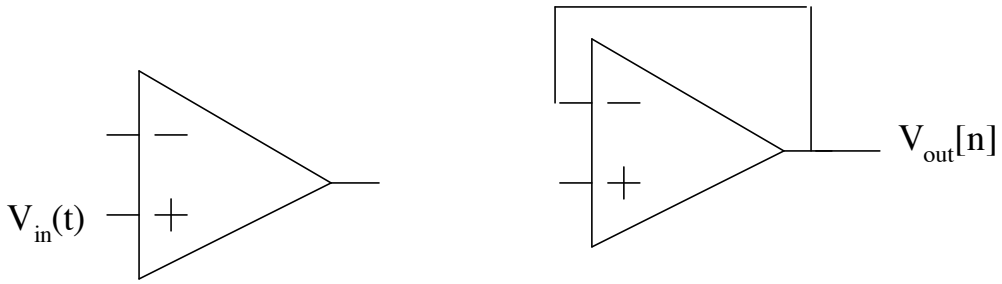
Phase I ($\phi_1 = 1, \phi_2 = 0$)



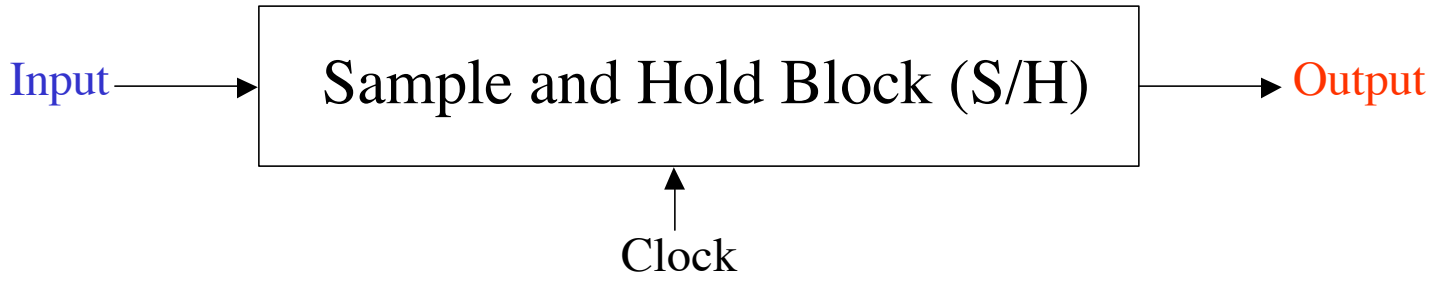
S/H elements

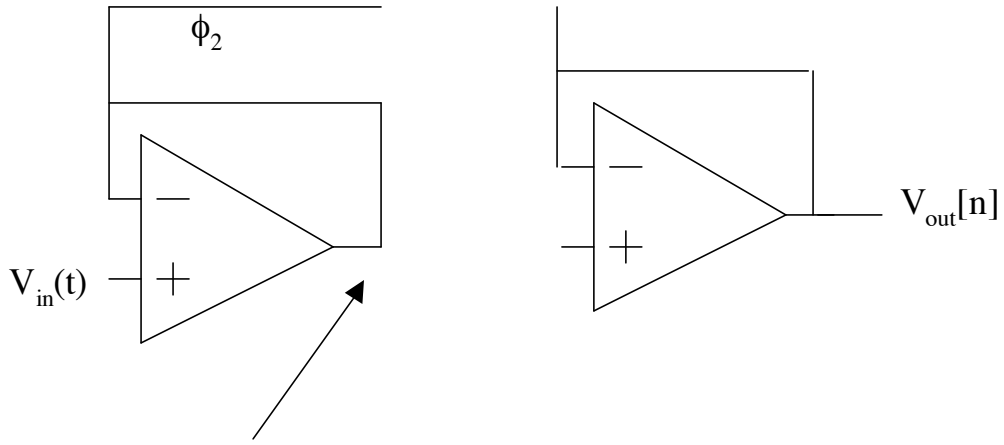


Phase II ($\phi_1, \phi_2 = 0$)



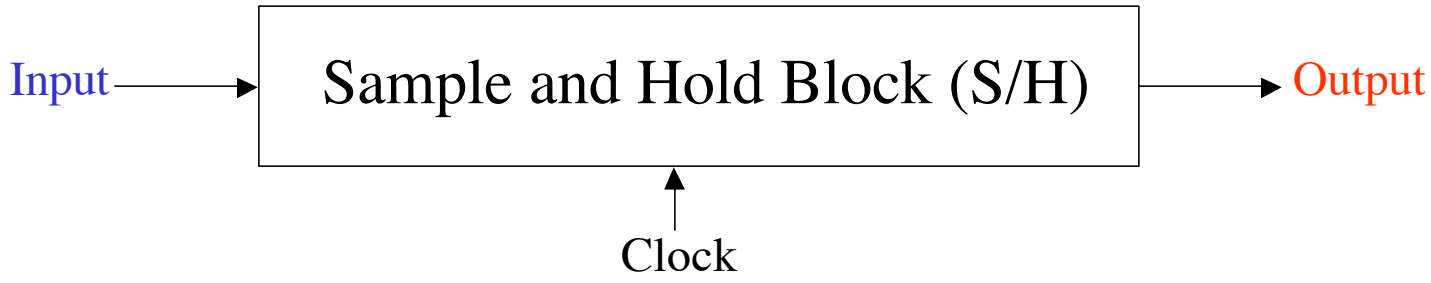
S/H elements

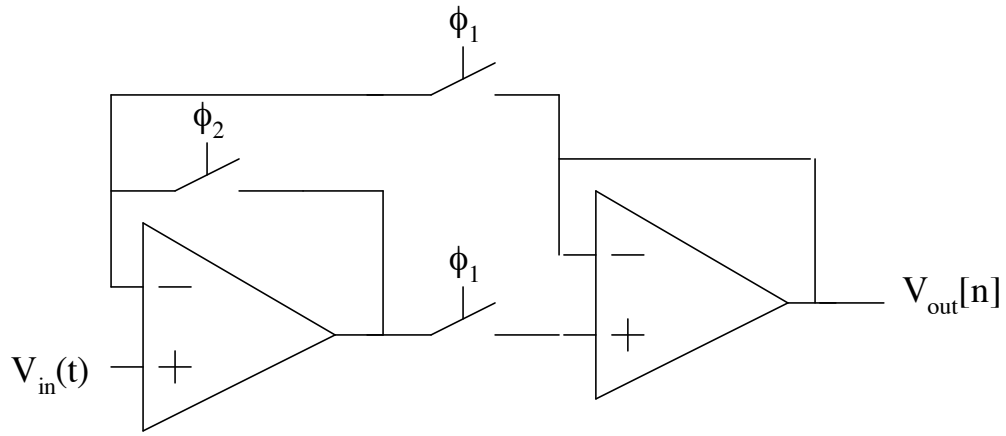




are ~ $V_{in}(t)$; therefore ready for the next phase

S/H elements





ϕ_1 and ϕ_2 are non-overlapping clocks