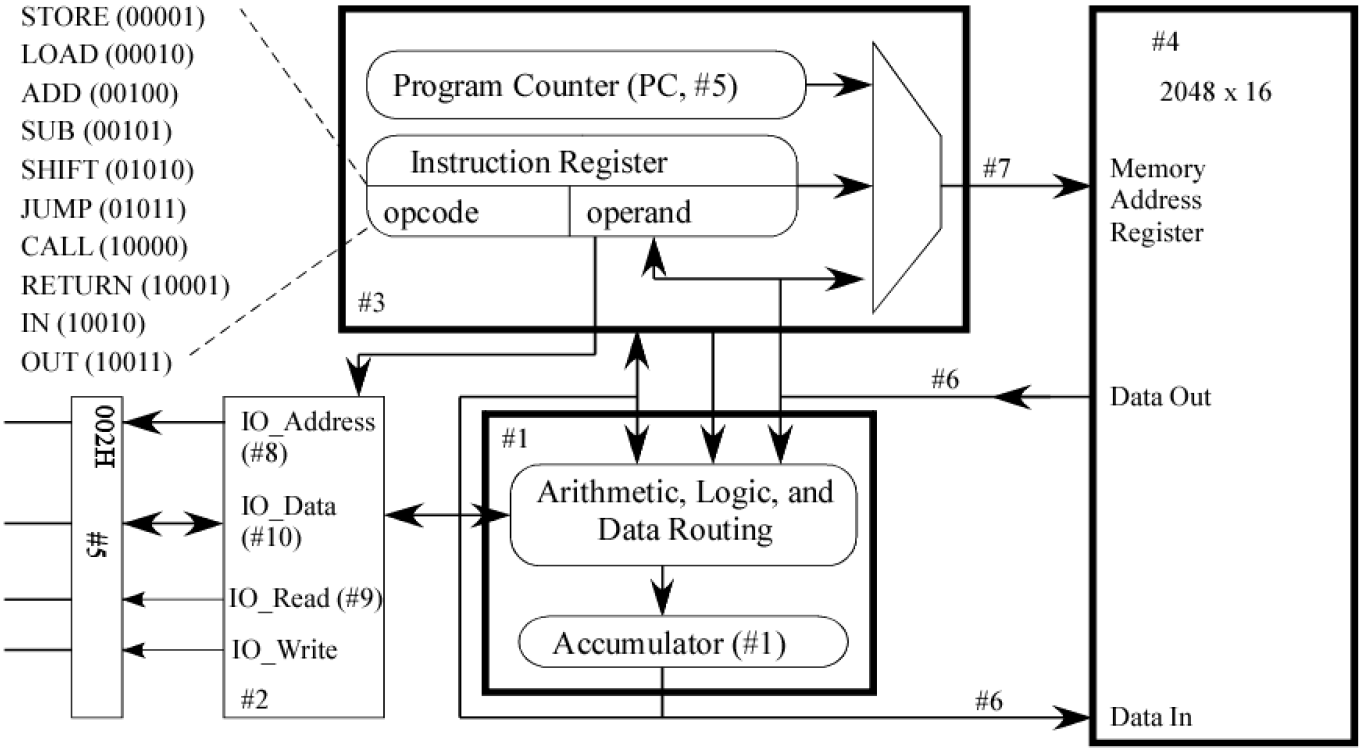
The following questions refer to the SCOMP processor we have been using in our projects



Question #1-#4 are matching with the following components

a. Memory
b. Interrupt
c. ALU
d. Timer
e. Peripheral
f. Cache
g. Control
h. LED display

_____ 1.

_____ 2.

_____ 3.

_____ 4.

_____ 5.

Question #6-10 are digital bus sizes (widths)

a. 1
b. 2
c. 4
d. 5
e. 11
f. 12
g. 15
h. 16

_____ 6.

_____ 7.

_____ 8.

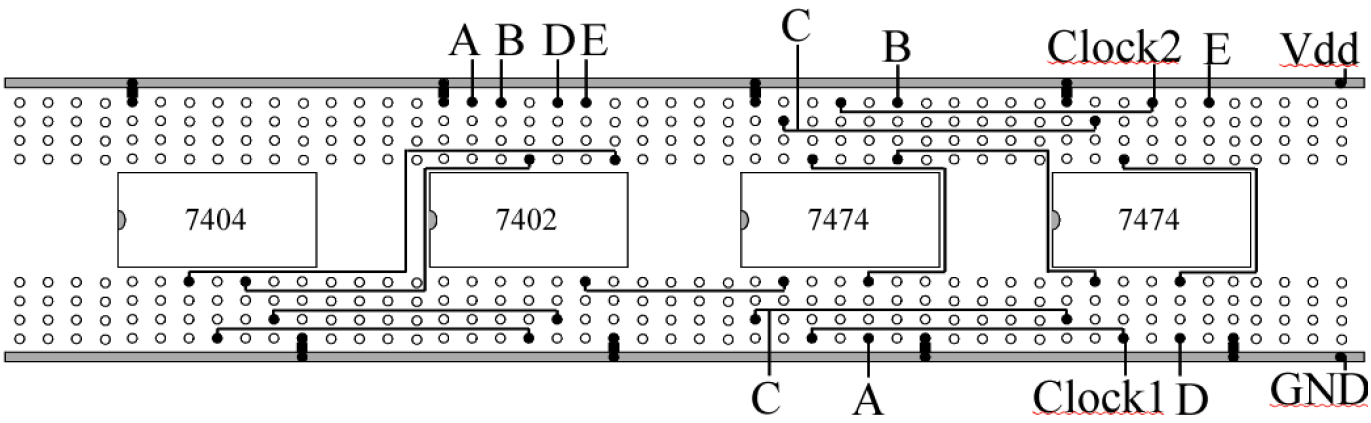
_____ 9.

_____ 10.

_____ 11. What instruction would you use to multiply a number in the accumulator by 4 in a single instruction? a. ADD b. SUB c. JUMP d. SHIFT e. LOAD	_____ 12. What command is used to send the accumulator to an IO port? a. JUMP b. IN c. SHIFT d. OUT e. LOAD	_____ 13. What command is used to execute a subroutine? a. RETURN b. IN c. CALL d. OUT e. JMP

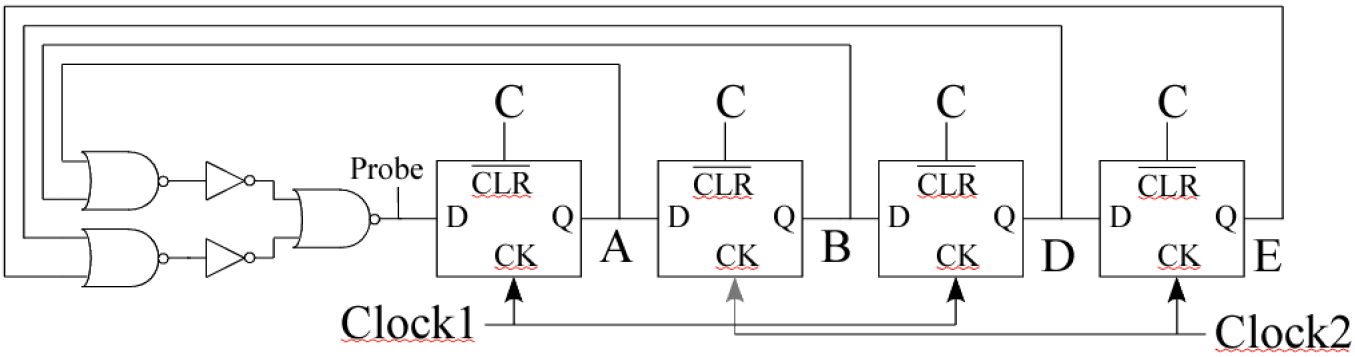
Your company has a critical component used in a larger system that was made from discrete parts that you want to have implemented as part of an FPGA. The problem has been assigned to you to take this component, analyze it, and make an FPGA implementation. The diagram from a breadboard, like the solderless breadboards you use in class is below. The design uses familiar 7402, 7404, and 7474 chips that you have used in lab where one should assume roughly 10ns delay for a gate through this breadboard.

The board has five signals, A, B, C, D, & E and two non-overlapping clock signals, Clock1 & Clock2.



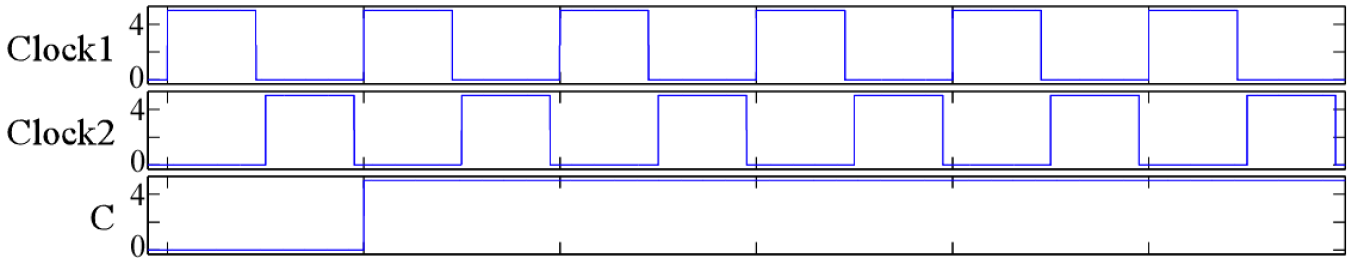
Draw the gate level diagram for this circuit.

For this problem, continue the problem assuming the following solution (from first objective part), where we still have a gate delay of 10ns in the protoboard. Clock1, Clock2 are the clock inputs, and C is also an input into the circuit.



What is the logic function between A, B, D, and E and the Probe output? What is the propagation delay?

Complete the timing diagram for the remaining signals and the probe signal. Why are the clocks non-overlapping and alternating for the four shift registers? Describe the output you would see if C = 0? What does the C signal do?



What is the VHDL code for your implementation that performs the same function as this circuit?