ECE 2031 Exam 1
Summer 2025

Name _____

General Instructions instructions:

- Exam is closed book / closed notes other than the one-page of handwritten notes.
- Choose the best possible answer available in all cases.
- Blank scratch paper is allowed

The first part (Objective Questions) of the exam is to be completed and submitted first. When you have submitted the first part of the exam, you will be handed the second part (Open Response Question) part of the exam.

_____/52_ Part I: Objective Questions

_____/48_ Part II: Open Response Question

____/100_ Final Score

ECE 2031 Exam 3 (Final Exam) Part I Answer Sheet
Summer 2025

Name _____

General Instructions:

- Exam is closed book / closed notes other than the allowed handwritten notes.
- Choose the best possible answer available in all cases.
- The only graded answers are those placed on the lines below, and would be the identified element (e.g. a, b, c, d, e, f, requested short answer, True / False, etc). You may keep the following pages as they will not be used in grading
- Blank scratch paper is allowed

The first part (Objective Questions) of the exam is to be completed and submitted first. When you have submitted the first part of the exam, you will be handed the second part (Open Response Question) part of the exam. Each question has equal weight (4 points each).

_____ Question 1

_____ Question 2

_____ Question 3

_____ Question 4

_____ Question 5

_____ Question 6

_____ Question 7

_____ Question 8

_____ Question 9

_____ Question 10

_____ Question 11

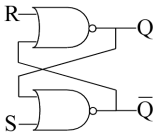
_____ Question 12

_____ Question 13

Part I: Objective Questions

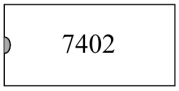
These questions have straight-forward answers. Make sure to put your answer in the line required as that is the part that will be graded for the answer given. Only the final answers, as indicated by the question, will be considered correct for each question. Each question is worth 4 points (total of 80 points)

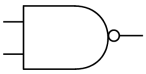
Matching (Choose the best answer):

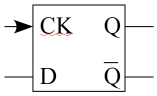
_____ 1. 

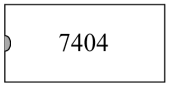
_____ 2. 

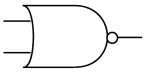
_____ 3. 

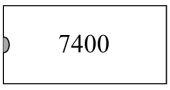
_____ 4. 

_____ 5. 

_____ 6. 

_____ 7. 

_____ 8. 

_____ 9. 

a. Multiple NAND Gates

b. Multiple Inverters

c. D Flip Flop

d. A NOR Gate

e. A NAND Gate

f. Multiple NOR Gates

g. SR Latch

h. CMOS Inverter

i. Multiple Flip Flops

Implement the following logic expression for a given output (OUT) given the input signals (A, B, C) entirely in 2-input NAND gates

_____ 10. A + B C

_____ 11. (A + C) B

_____ 12. AB + AC + BC

_____ 13. (True/False) An FPGA uses a number of physical lookup tables to target logic gates on the FPGA.

ECE 2031 Exam 1 Part II Open Response Question
Summer 2025

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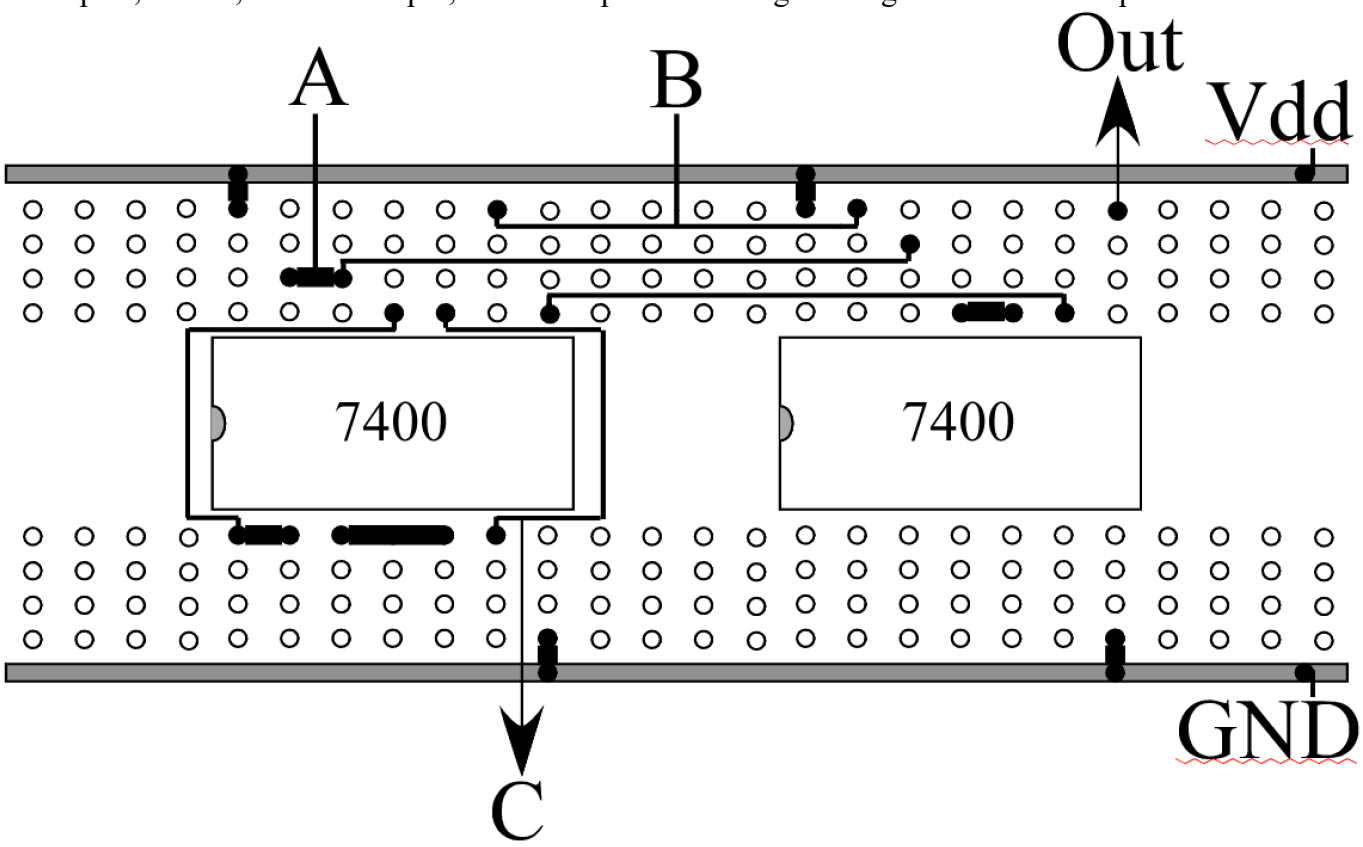
_____/48_ Part II: Open Response Question

Your company has a critical component used in a larger system that was made from discrete parts that you want to have implemented as part of an FPGA. The problem has been assigned to you to take this component, analyze it, and make an FPGA implementation. The diagram from a breadboard, like the solderless breadboards you use in class is below. The design uses familiar 7400 chips that you have used in lab where one should assume roughly 10ns delay for a gate through this breadboard. The board has two inputs, A & B, and one Output, Out. This problem will go through a number of steps.



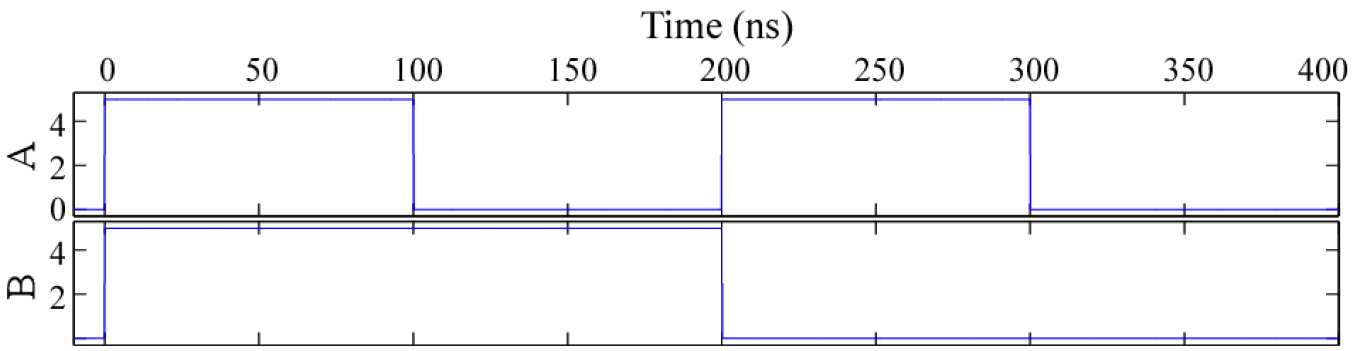
1. Draw the gate level diagram for this circuit.

2. Write the logic expression assuming the two inputs, A and B, as well as the intermediate output C. You will also want to identify the function to get C.

3. Describe the output you would see if B = 0 for any input signal of A?

4. What is the output you would see if B = 1 for step up and step down changes in A?

5. Draw a timing diagram given the starting signals for A and B. You will want to include C, other intermediate signals, as well as the Out signal.



6. What is the VHDL code for your implementation that performs the same function as this circuit?