

# Reconfigurable Analog PDE computation for Baseband and RF Computation

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**Abstract:** This discussion focuses on ODE / PDE analog computation in large-scale Field Programmable Analog Arrays (FPAA). In particular, we focus on the capability of first and second-order ladder topologies as the basis for second-order waveguiding PDEs. One-dimensional ladder topologies enable linear delays, linear-phase analog filters, as well as analog beamforming, potentially at RF frequencies. Two-dimensional ladder topologies enable solutions of PDE problems, such as E&M modeling based on Maxwell's equations.

**Keywords:** Physical Computing, FPAAs, PDEs

Large-scale Field Programmable Analog Arrays (FPAA) enables analog computing from low frequencies (e.g. 1-100Hz) to potentially RF frequencies. SoC FPAA enable both analog and digital signal processing and computation [1], while retaining the x1000 improvement (as predicted by [2]) in computational energy efficiency compared to custom digital solutions (e.g. Vector-Matrix Multiplication (VMM) [3]). Digital systems utilize relatively inexpensive high resolution (16, 32, or 64bit) with noisy numerics; analog systems utilize lower starting resolution (8 to 12bit typically) but with far less noisy numerical calculations [4]. Floating-Gate (FG) analog memory and computation in FPAA designs enable considerable parameter (and computational) density; memory and computation capability are closely linked in analog computation. These configurable devices compare favorably against custom designs; unlike FPGA designs, FPAA architectures are open to the academic community.

Figure 1 shows the typical system test for our SoC FPAA system. The FPAA can communicate entirely through digital interfaces; the present structure can communicate through serial or SPI to a USB port to be controlled through a laptop or tablet. The interface allows direct and standard connection to most platforms. The communication between the FPAA and the host typically requires a majority of the power, as opposed to the IC or resulting infrastructure. In a typical high performance computing system, one might expect many FPAA devices implemented on a single board, multiplying up the resulting system performance.

This discussion focuses on ODE / PDE analog computation available in SoC FPAA structures. One such computation is a ladder filter (Fig. 2), a transconductance-capacitor

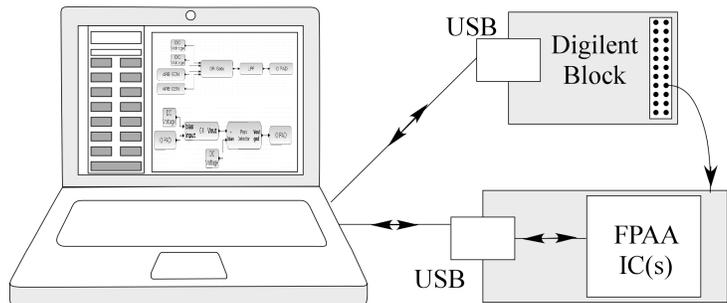


Figure 1: A typical measurement setup for SoC FPAA devices. The interface is a USB port to communicate and power the resulting board. Additional resources (like a Diligent function generator + scope) can be easily used for further characterization.

implementation of LC networks (2<sup>nd</sup> order waveguiding PDEs) [4].

Even though analog PDE solutions require discretizing in space, the continuous-time PDE solutions provide significant numerical advantages, as well as expected energy-efficiency improvements. The algorithm tradeoff between analog and digital computation directly leads to the tradeoff between high precision with poor numerics of digital computation versus the good numerics with lower precision of analog computation [5]. ODE / PDE computations are the framework for analog numerics, similar to LU decomposition and Matrix inversion are the framework for digital numerics [5]. One would not want to simply emulate the matrix solution operations for

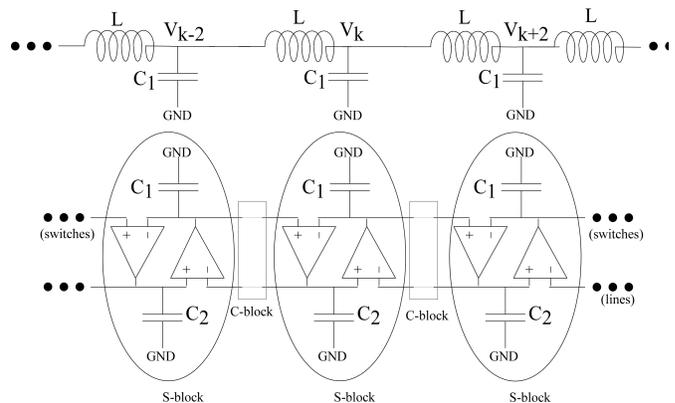


Figure 2: Implementation of a one-dimensional ladder filter for computing inductor (L) and capacitor (C) lines. These components can be implemented in CABs or as part of routing.

analog computing. Analog summation by charge or current (change of charge with time) is ideal due to KCL, or the physical summation of carriers. Analog integration is also effectively ideal, typically performed as a current (or sum of currents) on a capacitor.

Analog naturally has infinitesimal timesteps, and therefore no issue of errors due to these timesteps or accuracy questions due to the order of numerical integration approximation. This capability is precisely the framework why analog computation is ideally suited towards solutions of ODEs. These features extend to benefit hyperbolic PDE in a similar fashion. For example, stability issues related to temporal discretization are trivially satisfied. Classical digital PDE error accumulation (e.g. phase accumulation) is primarily due to sampling of time [6] is completely eliminated by this analog technique. Continuous-time computation eliminates constraining sample sizes in space and time [6]. One solves the physical system, so any nonlinearities are effectively part of the problem (and the solution, like the analytic solution), as opposed to error accumulating in the form seen in digital time varying solutions. Analog systems (properly designed) allow systems to run to

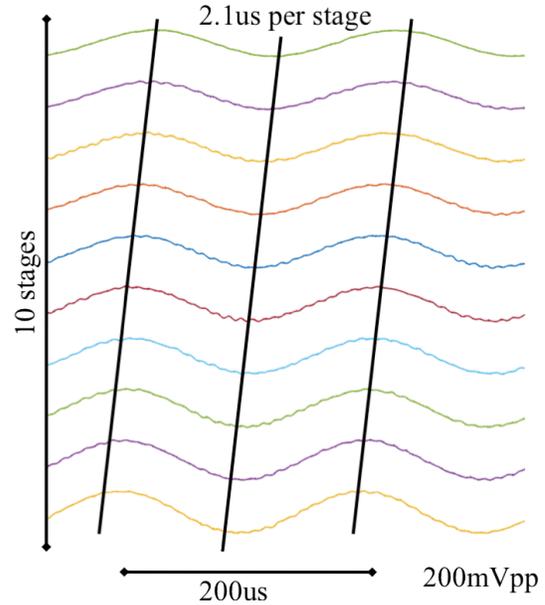


Figure 4: Measured data for a sine-wave input (5kHz) to a 10-tap ladder filter implemented on the SoC FPAA (350nm IC).

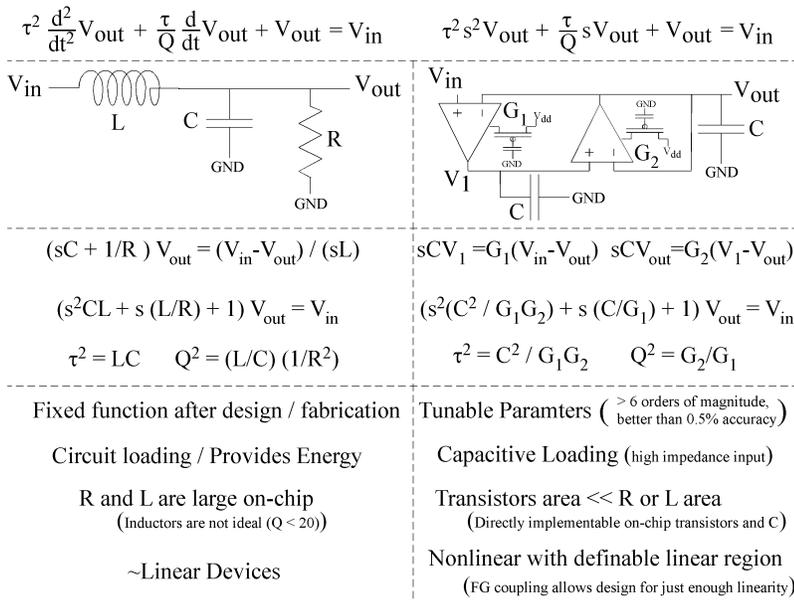


Figure 3: Illustration and comparison of simulating ODEs using FG programmable OTAs versus passive devices. Passive device comparison will be similar to passives using Op-amp devices; switched capacitor approaches will be less ideal except for linearity, as well as this technique loses all continuous-time advantages. Both approaches can implement the desired second order equation (expressed as an ODE and in Laplace form in this case). OTA approaches are known for efficient, low-noise IC circuit design, as well as not appreciably loading driving circuits. OTA conductances are programmable through their current source, implemented through an FG transistor. Capacitors to GND show up everywhere on a CMOS IC, making this approach amiable to dense CMOS implementation. Passive implementation potentially only wins on linearity, a metric potentially tunable to its sufficient ranges using FG devices.

arbitrary time lengths. The spatial sampling results in a particular error due to spatial grids; programmable devices allow for programmable nonlinear grids. Alternative solution methods could utilize sets of spatial basis functions, still solved in continuous time.

Figure 3 shows a comparison of using passive components and FG OTAs to implement a linear, second-order differential equation. Figure 2 shows the basic transformation between an inductor-capacitor line and an OTA-capacitor line. Both approaches can implement the desired second order equation (expressed as an ODE and in Laplace form in this case). One will get a similar comparison between an RC network and OTA-C circuit. A (small) resistor and an OTA require similar size in an FPAA implementation. Inductor IC implementation is difficult at best, where the inductor size is huge and the inductor Q is rarely over 10. Although an inductor-capacitor would have no noise, introducing a resistive element (or finite Q) creates a similar thermal noise component. The transconductance amplifiers utilize current sources programmable over six orders of magnitude in current (and therefore time constant) [7].

Figure 4 shows the one-dimensional measurement for a compiled (measured on an

FPAA) 10-stage delay-line ladder-filter implementation. These continuous-time approaches, while discretized in time, eliminate many computational issues. Figure 4 shows the wavepropagating, linear delay behavior for an input sinewave measured from the SoC FPAA [1]. These SoC FPAA compiled linear-phase analog filters would be the front-end block used for analog beamforming. Beamforming would require a Vector-Matrix Multiplication (VMM) to generate the final beams.

These results extend to potentially scaling of FPAA devices. FG and FPAA devices can scale from 350nm CMOS (e.g. SoC FPAA) to smaller linewidths, including 130nm and 40nm CMOS, resulting in quadratically higher

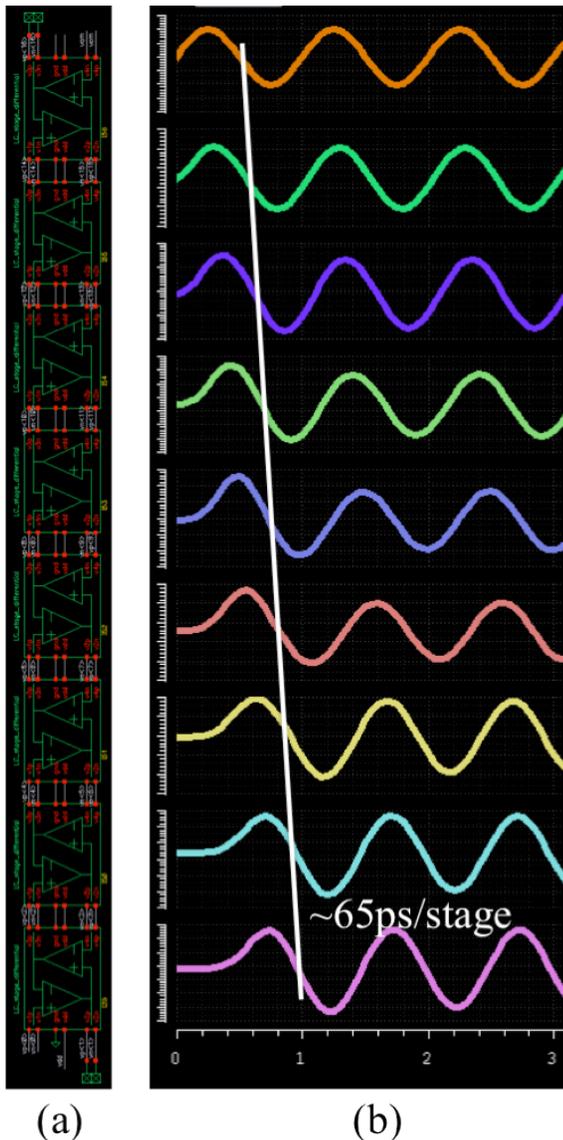


Figure 5: 40nm Ladder Filter design. (a) Cadence schematic of 40nm fabricated design. (b) Post Simulation of 8-tap Delay-line application of the ladder filter (4GHz input). The filter was tuned (using FG devices) to a nearly constant 65ps delay; other delays are also programmable.

bandwidths through the FPAA fabric [8,9]. Figure 5 shows spatio-temporal beamforming simulation at 4GHz bandwidths based on measured 40nm measurements.

FG-enabled Operational Transconductance Amplifiers (OTA) are one (of multiple) key CAB components available on the SoC FPAA. Other elements are available, and utilized, including FG and non-FG transistors, switches, multipliers, and current mirrors. The OTA element illustrates one important example device for numerical computation, particularly second-order hyperbolic and parabolic equations. Figure 6 illustrates the three key advantages of the FG OTA approach. OTA devices are known as a transistor efficient, power efficient, and lowest-noise implementation available for analog filters. Op-amp based designs are never be as efficient, resulting from building an excellent amplifier constrained by feedback. Switched capacitor designs achieve high linearity by oversampling with a resulting high-energy cost [10]. Switched-capacitor circuits do not use continuous-time operation (eliminating many of the resulting ODE advantages). FG OTAs completes an analog computational capability. FG for bias current allows OTA to be programmed over 6-8 orders of magnitude in current with better than 0.5% accuracy throughout (e.g. one example in [7]). FG OTA allows for wide linear range where needed (upto power supplies). This technique opens up just amount of linear range needed. Without FG, one has to deal with nonlinearities / linearity of the OTA device. On SoC FPAA, we have only required three input ranges, sufficient for applications for the last 7 years.

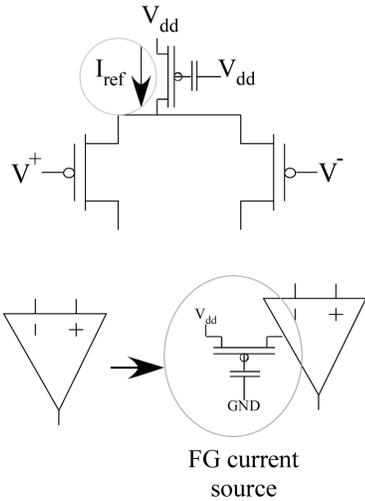
Expanding the ladder filter to two dimensions opens up computational capabilities beyond filtering and beamforming. A second-order ladder structure computes a two-dimensional wave equation. Figure 7 shows a two-dimensional ladder filter for computing electric field in a 2-D space. Maxwell's equations for electric field (multidimensional) can be formulated as

$$\nabla^2 \vec{E} - \mu\epsilon \frac{\partial^2 \vec{E}}{\partial t^2} = \mu \frac{\partial \vec{J}}{\partial t} + \nabla(\rho/\epsilon)$$

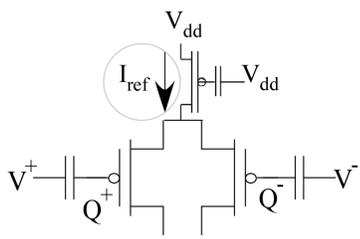
where we have one equation for each electric field component (in this case, two for two dimensions),  $\mu$  and  $\epsilon$  are fundamental E&M constants,  $\rho$  is the charge density, and  $\vec{J}$  is the vector current density. This PDE can be coupled with other ODEs or PDEs for more complex simulations.

This two-dimensional wave equation can be implemented on the SoC FPAA family. The PDE solutions on analog systems potentially could conservatively show x10,000 improvement over digital approaches, and potentially show x1,000,000 improvement over digital approaches. Computational energy efficiency allows for trading off computational speed and power. For example, x1,000,000 improvement could enable x1000 in speed, and x1000

Programmable FG Bias Current

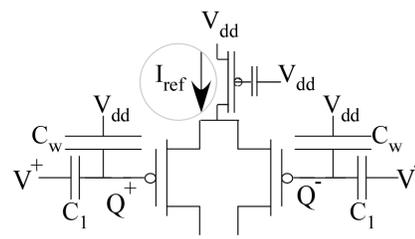


FG-Input OTA



Offset programmed by  $Q^+$  and  $Q^-$

FG Wide-Input Linear Range OTA



Linear Range Increase by  $\frac{C_1 + C_w}{C_1}$  & No noise increase by linearization  
 $VMM_1$  (first beam)

Figure 5-4: Three key OTA (Operational Transconductance Amplifier) advantages using FG devices. These include programmable bias currents (over 6 orders of magnitude, < 0.5%), programming or eliminating input offsets, and designing the resulting OTA linear range. These advantages drastically simplify and modularize OTA(s) required in nearly any analog design.

decrease in power, as well as x100 in speed, and x10000 decrease in power.

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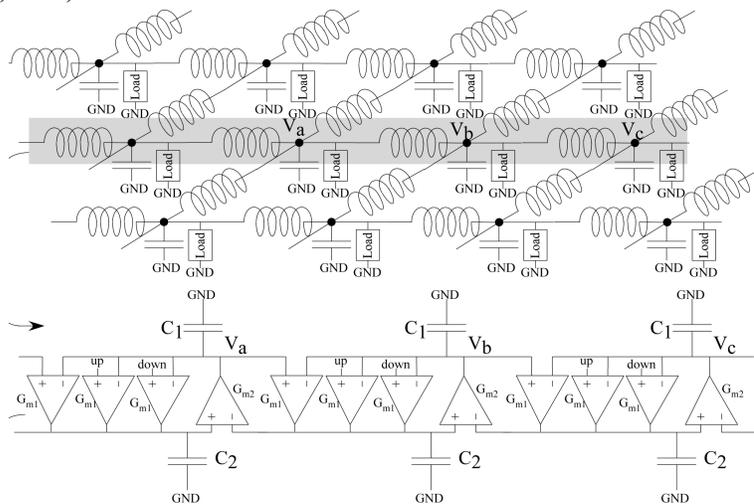


Figure 7: Implementation of physical-based FPAA solution for PDEs. We show an example for solving Maxwell's equations for Electric field vector using a network of capacitors and inductors. The load sets up the effect of charge in the network. Without a load, one gets typical transverse waves described in EM wave discussions. This approach can be transformed on-chip as a ladder-filter implementation using on-chip, FG tunable OTA devices. The tunable approach enables non-uniform sampling densities; one should choose the grid spacing for the particular problem.