Temperature Sensitivity and Compensation on a Reconfigurable Platform

Sahil Shah, Hakan Toreyin, Jennifer Hasler, and Aishwarya Natarajan

***Abstract*— This brief investigates temperature compensation techniques for circuits and systems on a reconfigurable platform. The work demonstrates use of large-scale reconfigurable system-on-chip for reducing the variability of circuits and systems compiled on a floating gate (FG)-based field-programmable analog array (FPAA). The work presents current and voltage reference which could help in reducing the variability caused due to changes in temperature. These references are standard blocks in the Scilab/Xcos environment, which could be easily compiled on the FPAA. An FG-based current reference is then used for biasing a second-order $G_m - C$ bandpass filter to demonstrate the compilation and usage of these voltage/current reference in a reconfigurable fabric. The large-scale FG FPAA presented here is fabricated in 350-nm CMOS process.**

***Index Terms*— Circuits and system, field-programmable analog array (FPAA), reference generator, temperature dependence.**

I. Analog Processing and Temperature Dependence

The number of systems combining elements from within and among the emerging technologies of sensors, communications, and robotics grows every day. Computational abilities of these systems affect the overall system performance through various aspects (e.g., functionality, battery-life, and foot-print). Traditionally most computational tasks have been performed in the digital domain, which can achieve high resolution computation at the cost of high power consumption [1]. For systems with limited power budget, however, low-power real-time computation techniques have been sought after. Accordingly, analog-signal-processing has been used extensively as an energy-efficient alternative to digital options [2].

Recent mixed-mode large-scale field-programmable analog array (FPAA) enables advanced functionality for a wide spectrum of sensor applications [3]. The current FPAA is fabricated in 350-nm technology. In general, floating gates (FGs) have been shown to be operational at even 40-nm technology node [4]. These FPAAs combines the energy-efficiency, reconfigurability, and programmability of floating-gate-based analog signal processing with the precision and compatibility of digital, thereby a variety of analog circuitry implemented on FPAAs serve as building blocks of more complex signal processing functions [5]. For performing these tasks, the FPAA and its circuits have to operate at different temperatures and, hence, the need to investigate temperature dependence and compensation techniques.

This brief presents a range of techniques and models to estimate and reduce temperature variability of various systems. Fig. 1 shows the proposed method a user could follow depending on the specific application. A set of voltage and current reference generator are presented, which can be compiled on the FPAA to reduce temperature variability of the system. Here, we propose to use FG as a programmable element to achieve reasonable temperature insensitivity rather than trimming or programming single value FG to achieve

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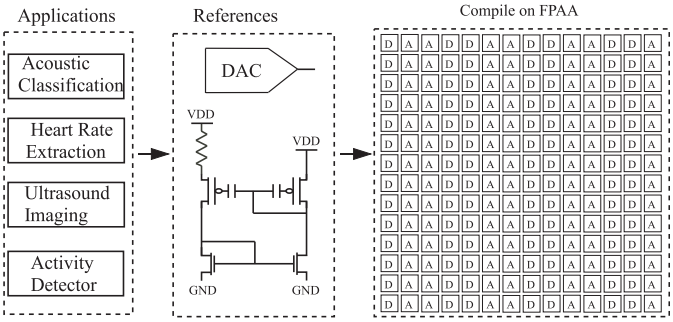

Fig. 1. Proposed method to reduce temperature variability while compiling a system for a desired application on an FPAA. The user would choose from multiple voltage and current references depending on the application. Then the system along with the selected references would be compiled on the FPAA. Here, FPAA fabric consisting of analog and digital blocks are shown [3].

precision [6]. These references form standard blocks in the open source tools built in Scilab/Xcos environment available online [7]. This brief utilizes an Xcos tool simulation model [7] to model circuits block temperature variation. All temperature measurements were performed using ZPlus (Cincinnati Subzero Products LLC, Sharonville, OH, USA) temperature chamber. For each temperature value, 15 min is allowed to ensure that the FPAA die reaches the desired temperature value.

II. Modeling Temperature Dependence

As a part of the tool infrastructure for an FPAA, a simulation model adapted from the EKV model [8] for all regions of operation is developed [7]. Based on the model, the channel current for a pMOS transistor is governed by the following equation:

$$I_d = I_{\text{th}} \ln^2\left(1 + e^{(\kappa(V_{\text{DD}} - V_g - V_{T0}) - (V_{\text{DD}} - V_s) + \sigma(V_{\text{DD}} - V_d))/2U_T}\right) - I_{\text{th}} \ln^2\left(1 + e^{(\kappa(V_{\text{DD}} - V_g - V_{T0}) - (V_{\text{DD}} - V_d) + \sigma(V_{\text{DD}} - V_s))/2U_T}\right) \quad (1)$$

where Ith is the specific current at threshold voltage given by $((2\mu C_{\text{ox}}(W/L)U_T^2)/\kappa)$, σ is the drain-induced barrier lowering coefficient, and V_d, V_s, V_{T0}, and U_T are the drain-source, threshold, and thermal voltages, respectively. Temperature dependence of I_d in (1) arises from V_{T0}, Ith, and explicit U_T. The dependence of V_{T0} on temperature could be modeled using $A_1 + A_2 * U_T$. Ith has dependence on temperature due to the mobility (μ) and presence of U_T^2, which could be modeled using $I\text{thr} * (T/T_r)^{0.5}$. Here, T_r is the reference temperature. It should be noted that the model in [8] has a more number of parameters and is much more generalized. In the case of (1), the model has a reduced number of parameters, which allow faster simulation, with the ability to closely predict data from the FPAA. This model has been integrated as a part of Scilab/Xcos environment [7]. Fig. 2 shows measurement of pFET compiled onto the FPAA and simulation performed using the EKV model. The tool incorporates the associated temperature dependencies of U_T, threshold voltage (V_{T0}), and current at threshold voltage (Ith). Fig. 2 compares the temperature dependencies between the simulated model and the measured results over a change of 60 °C. The measurements are silicon data obtained from the FPAA fabricated in 350-nm technology.

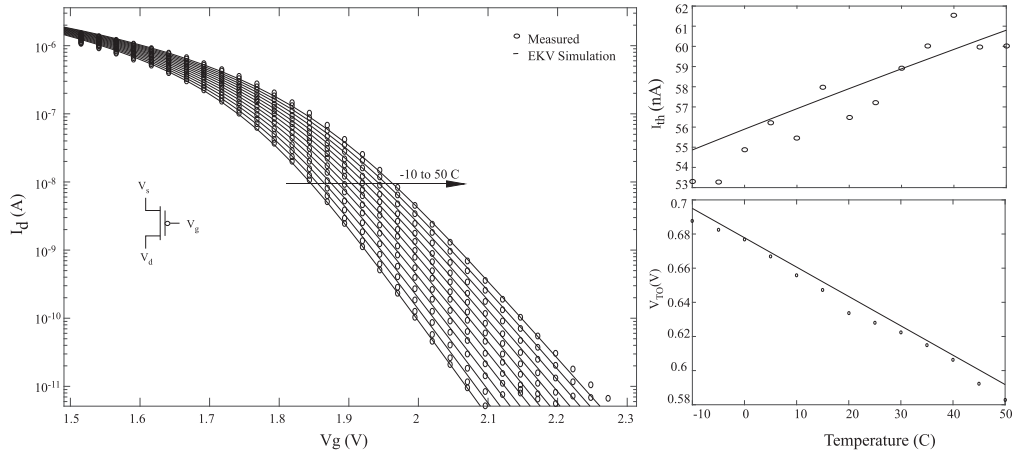

Fig. 2. Transfer characteristics of pMOS over temperature. EKV modeling is used for modeling the transfer characteristics of a pMOS [7]. Ith, current at threshold voltage, and V_{TO}, threshold voltage, are also plotted over temperature. The simulated values are consistent with the measured values. The Ith and V_{T0} are extracted by curve fitting onto to the output current in both measurement and simulation to be consistent.

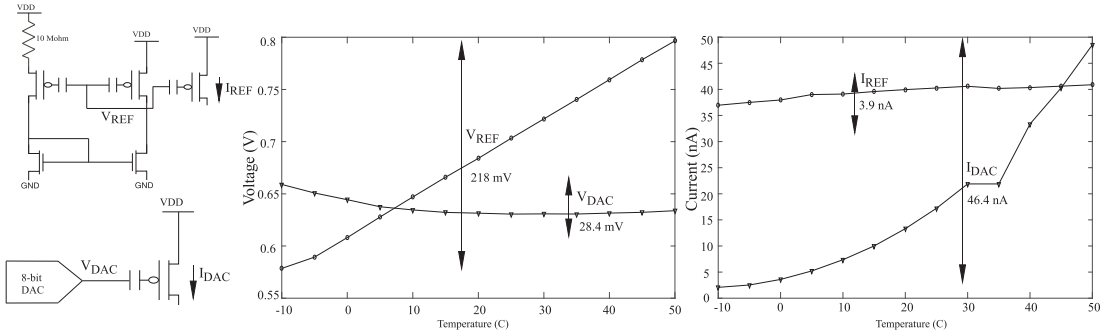

Fig. 3. FG-based bootstrap reference circuit compiled on the FPAA for biasing the FG transistors. The DAC generally used to bias the FG transistor is also characterized over temperature. Output of the reference generator (V_{REF}) is plotted over a temperature variation of 60 °C. The output of the DAC is also measured over the same temperature range. Also, the effects of temperature on the drain current is studied by biasing an FG transistor in both modes, i.e., bias using a DAC and the bootstrap reference circuit.

III. Reducing Temperature Dependence in Programmable Circuits and System

Programming and biasing of FG switch or FG current source in an FPAA [3] is generally done using a digital-to-analog converter (DAC). During programming mode, when the circuits and systems are getting compiled on the FPAA, the DAC allows for varying the bias of the gate for compensating the variation and mismatch on the FPAA [9]. It is assumed that temperature would not vary drastically while programming the device. In run mode, however, when the implemented system is used for computation and processing on the FPAA, the temperature could vary based on the application, for example, in wearable systems [5] or as a sensory node for analyzing speech [5]. A subthreshold current reference circuit, similar to a conventional current reference circuit [10] would bias the gate of a pFET, which would reduce the temperature variation of the output current to 12.0%. The biasing current is constant and is not programmable unless (W/L) of its transistor and the resistor values are changed. In the case of an FPAA, it would be possible to change (W/L) by adding pFETs and nFETs in parallel. However, this would mean adding extra capacitance by the way of routing to different computational analog blocks (CABs).

A. FG-Based Reference Circuit in Subthreshold Region

The reference circuit in Fig. 3 is based on the bootstrap reference architecture. However, unlike the conventional bootstrap reference architecture where the difference between the aspect ratios of pFETs is responsible for the reference generation, the V_{REF} in Fig. 3 is generated because of the difference in the amount of charge stored at the floating node of the FG pFETs. The bootstrap reference circuit in Fig. 3 is compiled using FG pFET from the switch fabric, which are part of the local interconnect routing present in the CAB, and nFET current mirror, which is a part of the CAB elements described in [3]. Current and voltages were measured using an external pico ammeter (Keithley Instruments, Cleveland, OH, USA), and the Analog Discovery portable oscilloscope (Digilent Inc., Pullman, WA, USA), respectively.

Fig. 3 also shows measurements of V_{REF}, I_{REF}, V_{DAC}, and I_{DAC} against temperature. A variation of 28.4 mV was observed in the DAC, thereby resulting in temperature variation of 189 ppm/°C with a linear range of 2.5 V. This manifests as a large change in current, when used to bias an FG, since the voltage does not scale with temperature to compensate the variation in threshold voltage and Ith. The bootstrap current reference has a variation of 218 mV in V_{REF} and the current mirror output has a temperature drift of 3.9 nA.

Evaluating the relationship of I_{out} and I_{in} over temperature of a current mirror built with an FG pFET, such as that used in Fig. 3 for biasing, is given by $I_{\mathrm{out}} = I_{\mathrm{in}} e^{\kappa(V_1 - V_2)/U_T}$, where if V_1 and V_2 are equal then we have $I_{\mathrm{out}} = I_{\mathrm{in}}$. In general, for a non-FG current mirror there is a threshold voltage mismatch between the transistors, which will lead to variation of I_{out} with temperature. The variation of current in this case could be modeled as $I_{\mathrm{out}} = I_{\mathrm{in}} A = I_{\mathrm{in}} A_0^{T_0/T}$, where $A = e^{\kappa(V_1 - V_2)/U_T}$ where T_0 is a reference temperature which could be room temperature for simplicity.

IV. Variation of Bandpass Filter

A $G_m - C$-based second-order bandpass filter is used extensively for several signal processing systems [3]. A second-order

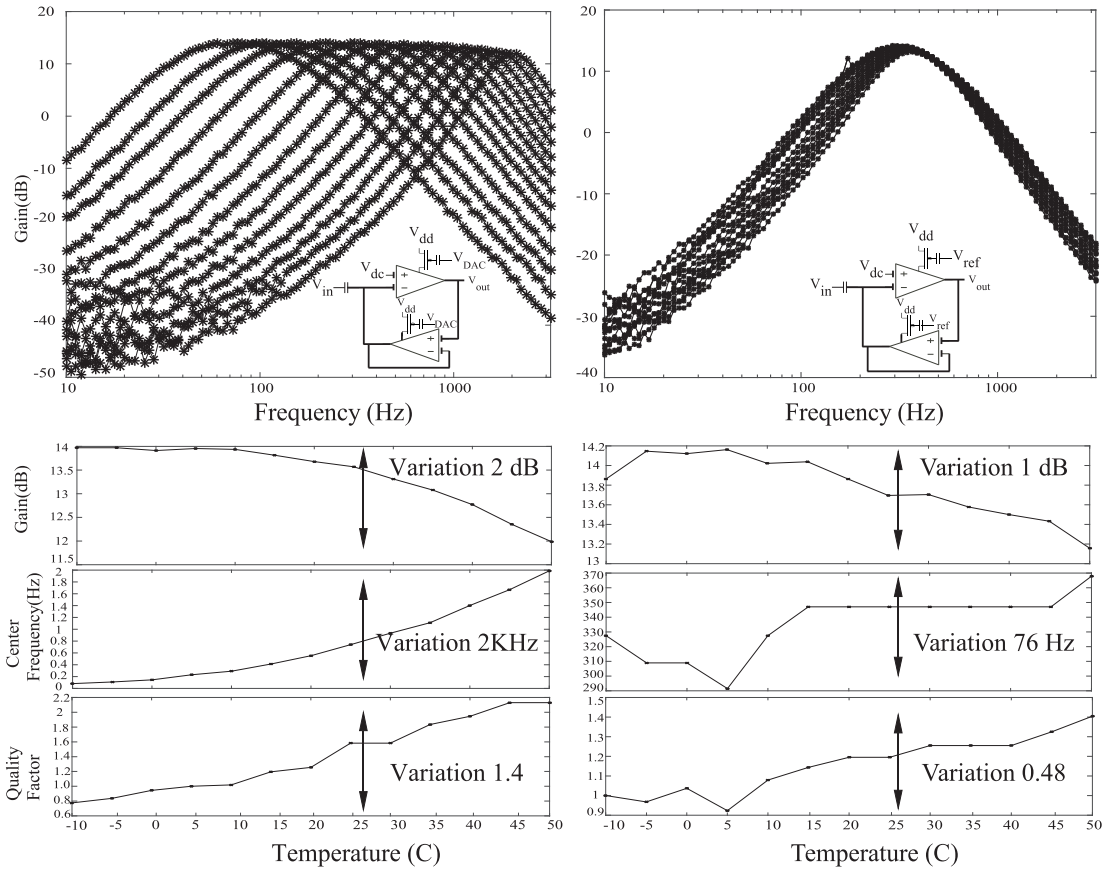

Fig. 4. Frequency response of bandpass filter over temperature. The measurement is performed in two different modes, one where the FG pFET is biased using a DAC and the other being the bootstrap reference generator. Bottom: reduction in sensitivity to temperature of three different bandpass filter parameters while using the reference generator for biasing. A variation of 2 kHz in center frequency, 2 dB in gain, and 1.4 in the quality factor was observed when the bandpass filter was biased using a DAC. In case of the bootstrap reference generator, a variation of 76 Hz in center frequency, 0.48 in quality factor, and 1 dB in gain of the filter was observed.

$G_m - C$ filter enables extracting frequency-based features from the input signal with a low power consumption. The topology allows the user to program a large range of center frequencies (sub-Hz to a few KHz) as compared to a highly linear RC-active filter [11], [12], where one would require banks of capacitors or resistors to tune the filter after fabrication. In case of an application where the center frequency is in sub-Hz, the size of on-chip RC components would be fairly large on an IC compared to a $G_m - C$ filter, where one could bias the OTA with pA of currents. An LC implementation using ladder topology would also require G_m elements and, hence, would need temperature compensation. An FG-based $G_m - C$, implemented in this brief, offers programmability over broad range of center frequencies by changing the bias of the FG operational transconductance amplifier (FGOTAs). An FGOTA is an OTA with capacitively coupled input to increase the linearity of the G_m element. The PSRR, CMRR, input referred noise, and other characteristics of the filter are described in detail here [13].

The inset in Fig. 4 shows the schematic of a $G_m - C$ filter compiled in a single CAB of the FPAA. The FGOTA are biased using an FG pFET as seen in Fig. 4. Fig. 4 shows the frequency response of the bandpass filter over 60 °C of temperature change when biased using a DAC. Fig. 4 also shows variation in the center frequency (f_c), quality factor (Q), and gain of the bandpass filter. The variation in center frequency is 2 kHz for a center frequency of 840 Hz at room temperature. This variation would lead to a significant error in the processing and extraction of features in different signal processing systems.

An FG-based current reference generator introduced in Section III-A would be suitable for biasing the $G_m - C$ filters. Fig. 4 shows the bootstrap reference compiled along with the bandpass filter. Fig. 4 also shows the frequency response of the bandpass filter over a temperature variation of 60 °C. The PTAT response of the FG-based bootstrap reference helps in compensating the CTAT variation in V_T. Fig. 4 also shows the variation in the characteristics of the bandpass filter, namely, Q, f_C, and gain at the center frequency. As compared to the case where it was biased by a DAC, the variation in f_C is reduced to 76 Hz, gain variation is 1 dB as opposed to 2 dB, and Q variation is 0.48 compared to 1.4. Measurements in Fig. 4 were performed consecutively where the filter were biased first with a DAC and then with an FG current reference to keep other variations constant. The resulting temperature-dependent variation of 76 Hz observed in Fig. 4, could be explained due to the fabrication-related device mismatch between the FG pMOS used in the reference circuit and the FG pMOS used as the biasing transistor of the FGOTAs in the bandpass filter. In addition, there are design-related mismatches in the aforementioned FG pMOS devices as well. For instance, the coupling capacitor of the FG pMOS in the reference circuit is 8 fF as opposed to 43 fF in case of the FGOTA biasing device. The other source of mismatch is also due to different (W/L) of the FG pMOS transistors, which is [(1.8 μm)/(600 nm)] in case of FG reference circuit and [(6 μm)/(2 μm)]. In subsequent designs of the FPAA, these variations will be reduced by keeping a single size of FG transistors for all the devices on the SoC.

V. Summary and Discussion

There has been a growing interest in using FPAA for rapid prototyping of mixed signal systems, performing mixed and analog signal processing for wide ranging applications and using programmability and reconfigurability to increase system performance and energy efficiency [14]. Hence, it becomes more important to study the effects of temperature on a reconfigurable platform and investigate methods that could reduce these variations.

A bootstrap current reference is introduced to bias FG devices on the FPAA. The performance of the bootstrap reference is studied over temperature and measured results from the FPAA are presented. The FG reference circuit is also used to bias a second-order bandpass filer. Their performance over temperature when biased using a DAC and the FG reference circuit is studied. The bandpass filters f_C varies by 2 kHz when biased with a DAC whereas in case of FG reference circuit it varies by 76 Hz. Here, the focus of this brief is studying the variability and compensation techniques for low power analog signal processing. Using a reconfigurable platform for compensating RF circuits such as power amplifiers, LNA, and mixers could be a focus of a separate study.

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