MULTIPLE-INPUT TRANSLINEAR ELEMENT NETWORKS

Bradley A. Minch[†]*, Paul Hasler, and Chris Diorio*

[†]School of Electrical Engineering
Cornell University
Ithaca, NY 14853–5401
minch@ee.cornell.edu

ABSTRACT

We describe a class of nonlinear circuits that accurately embody product-of-power-law relationships in the current signal domain. We call these circuits multiple-input translinear element (MITE) networks. A MITE is a circuit element that produces an output current that is exponenial in a weighted sum of its input voltages. We describe intuitively the basic operation of MITE networks and we show experimental data from a squaring-reciprocal circuit breadboarded from bipolar–floating-gate MOS (biFGMOS) MITEs that we fabricated in a 2–µm double-poly CMOS process available through MOSIS.

1. PRODUCT-OF-POWER-LAW CIRCUITS

Products, quotients, and power-law relationships figure prominently in many signal and information processing algorithms. Consequently, analog circuits embodying such relaionships are important components in the construction of analog VLSI information processing systems. In the *Nonlinear Circuits Handbook* from Analog Devices, we find the following clear description of a general principle by which such functions may be realized:

> When compound multiplications, involving roots and powers are performed (e.g., $x_1^{\alpha} \times x_2^{\beta} \times x_3^{\gamma} \times x_4^{\delta} \times \ldots$), each input is "logged," multiplied by a constant...exponent of appropriate magnitude and polarity, the terms are summed and/or differenced, then the antilog is taken to convert the result back into the "world of phenomena" [1, p. 469].

A few power-law circuits that function according to this principle have been described in the literature [2–4]. Vittoz [4] cites Arreguit and his associates [3], and indicates that such circuits are based on a "generalization of the translinear principle" [4, p. 37]. Arreguit and his associates, in turn, cite the *Nonlinear Circuits Handbook* [1], and mention that, in analyzing such circuits, they can "apply the generalized translinear principle that translates the sum of voltages into a product of currents and their multiplication by a constant *k* into the elevation of the currents to the power *k*" [3, p. 443]. It seems that Arreguit and his colleagues are referring to the lines just quoted from the *Nonlinear Circuits Handbook* [1]. Despite these claims, these power-law circuits seem to have been conceived as a collection of special forms: one for powers between zero and unity, one for powers greater than unity, and one for negative powers. It seems that no unifying conception of these circuits has been heretofore achieved.

In this paper, we describe a framework for implementing such circuits and intuitively present the basic principles upon which they operate. We have formalized this intuitive analysis and have obtained systematic analysis and synthesis procedures for this important class of circuits [5].

2. BASIC MULTIPLE-INPUT TRANSLINEAR ELEMENT CIRCUIT STAGES

Consider the three basic circuit stages that are shown in Fig. 1. Each of these comprises a single multiple-input translinear element (MITE) [5], which accepts K input voltages, V_1 through V_K, and produces an output current, I, that is given by

$$I = \lambda I_{\mathrm{s}} \exp\left[\sum_{k=1}^{K} \frac{w_k V_k}{U_{\mathrm{T}}}\right], \tag{1}$$

where I_{s} is a pre-exponential scaling current, which could be temperature dependent, λ is a dimensionless quantity that scales I_{s} proportionally, and U_{T} is the thermal voltage, $\frac{kT}{q}$.

The first of the three basic MITE stages, shown in Fig. 1a, is a voltage-in, current-out (VICO) stage. Here, we apply input voltages, V_i and V_k, to two different input terminals of MITE Q_n, which, in response, generates an output current, I_n. To see how I_n depends on V_i and V_k, using Eq. 1, we write

$$I_n \propto \exp\left[\frac{w_{ni} V_i + w_{nk} V_k \ldots}{U_{\mathrm{T}}}\right].$$

By breaking out the first two terms of the weighted summation and using the fact that $e^{x+y} = e^x e^y$, we rewrite the preceding expression as

$$I_n \propto \exp\left[\frac{w_{ni} V_i}{U_{\mathrm{T}}}\right] \exp\left[\frac{w_{nk} V_k}{U_{\mathrm{T}}}\right]. \tag{2}$$

The second of the three basic MITE stages, shown in Fig. 1b, is a current-in, voltage-out (CIVO) stage. Here, we source a current, I_i, into the output of MITE Q_i, and we feed the output voltage, V_i, back through the self-coupling coefficient, w_{ii}. This feedback configuration adjusts V_i, so that the current sunk by Q_i just balances the input current, I_i. A MITE in this feedback configuration is analogous to a diode connected transistor, so we say that it is *diode connected* through w_{ii}. To determine how the output voltage, V_i, depends on the input current, I_i, we begin with Eq. 1, and solve for V_i in terms of I_i. So, we write

$$I_i \propto \exp\left[\frac{w_{ii} V_i \ldots}{U_{\mathrm{T}}}\right],$$

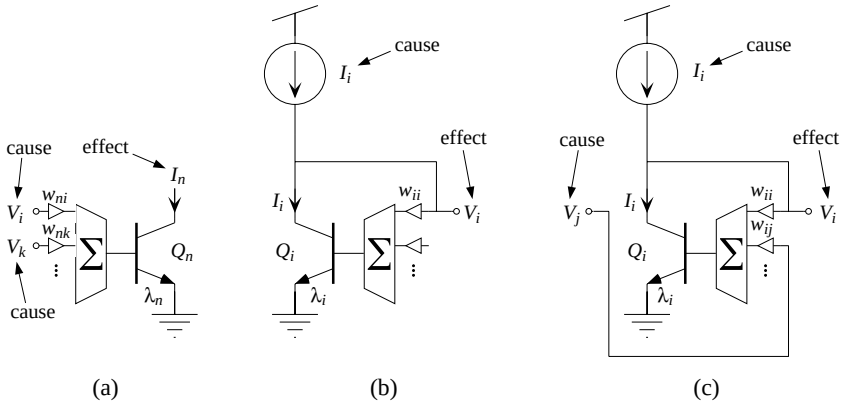

Figure 1. Three basic circuit stages, each comprising a single multiple-input translinear element (MITE). (a) A voltage-in, current-out (VICO) stage. (b) A current-in, voltage-out (CIVO) stage. (c) A voltage-in, voltage-out (VIVO) stage.

which we rearrange to find that

$$V_i = \frac{U_\mathrm{T}}{w_{ii}} \log I_i - \ldots . \tag{3}$$

The third basic MITE stage is a voltage-in, voltage-out (VIVO) configuration, shown in Fig. 1c. This configuration is identical to the CIVO stage of Fig. 1b, except that we now hold the current, I_i, fixed, and we are instead concerned with how the output voltage, V_i, depends on an input voltage, V_j, which we apply to another of the input terminals of MITE Q_i. Beginning with Eq. 1, we write that

$$I_i \propto \exp\left[\frac{w_{ii}V_i + w_{ij}V_j \ldots}{U_\mathrm{T}}\right],$$

which we rearrange to solve for V_i in terms of V_j as follows:

$$V_i = -\frac{w_{ij}}{w_{ii}} V_j - \ldots . \tag{4}$$

We can use the circuit stage of Fig. 1c as *both* a CIVO stage *and* a VIVO stage simultaneously. In this case, it is easy to see that V_i depends on V_j and I_i through a combination of Eqs. 3 and 4 as follows:

$$V_i = \frac{U_\mathrm{T}}{w_{ii}} \log I_i - \frac{w_{ij}}{w_{ii}} V_j - \ldots . \tag{5}$$

3. BASIC MULTIPLE-INPUT TRANSLINEAR ELEMENT NETWORKS

In this section, we describe two simple current-in, current-out circuits (CICO), each comprising two CIVO stages and a single VICO stage. These two CICO circuits illustrate all of the basic intuition behind the functioning of all MITE networks.

In the first CICO circuit, shown in Fig. 2a, we connect the outputs of two different CIVO stages directly to a single VICO stage through separate inputs. To analyze this circuit, we begin with Eq. 2 applied to the output stage as follows:

$$I_n \propto \exp\left[\frac{w_{ni}V_i}{U_\mathrm{T}}\right] \exp\left[\frac{w_{nk}V_k}{U_\mathrm{T}}\right]. \tag{6}$$

Substituting Eq. 3 into Eq. 6 for each of V_i and V_k, we obtain

$$I_n \propto \exp\left[\frac{w_{ni}}{U_\mathrm{T}}\left(\frac{U_\mathrm{T}}{w_{ii}} \log I_i - \ldots\right)\right] \exp\left[\frac{w_{nk}}{U_\mathrm{T}}\left(\frac{U_\mathrm{T}}{w_{kk}} \log I_k - \ldots\right)\right].$$

When we break out the first term in each of the two summations and regroup, this equation becomes

$$I_n \propto \exp\left[\frac{U_\mathrm{T}}{U_\mathrm{T}} \frac{w_{ni}}{w_{ii}} \log I_i\right] \exp\left[\frac{U_\mathrm{T}}{U_\mathrm{T}} \frac{w_{nk}}{w_{kk}} \log I_k\right]. \tag{7}$$

Note that, if MITEs Q_i, Q_k, and Q_n are operating at the same temperature, then the primary temperature dependence of the relationship between I_i, I_k, and I_n disappears from Eq. 7. In this analysis, we have not kept track of the scaling currents, I_s, which can be strongly temperature dependent, but, a more rigorous analysis [5] shows that, if the product of the input currents raised to their respective powers has units of amperes (i.e., as opposed to amperes raised to a power other than unity), then the relationship between the output current and the input currents is generally insensitive to isothermal variations. Now, because $x \log y = \log y^x$ and $e^{\log x} = x$, we can rewrite Eq. 7 as

$$I_n \propto I_i^{\frac{w_{ni}}{w_{ii}}} \times I_k^{\frac{w_{nk}}{w_{kk}}}. \tag{8}$$

Thus, the output current is proportional to the input current raised to a power that is set by a ratio of weighting coefficients.

For the second basic CICO circuit, instead of connecting the output of the second CIVO stage directly to a second input of the output VICO stage, as we do in the circuit of Fig. 2a, we connect the output of the second CIVO stage to the output stage through the first CIVO stage, as shown in Fig. 2b. This first CIVO stage both generates a voltage that is logarithmic in the input current, I_i, and serves as a VIVO stage for the second CIVO stage. This connection will allow us to obtain negative powers. To show that it will, we again begin with Eq. 1 applied to the output stage as follows:

$$I_n \propto \exp\left[\frac{w_{ni}V_i + \ldots}{U_\mathrm{T}}\right]. \tag{9}$$

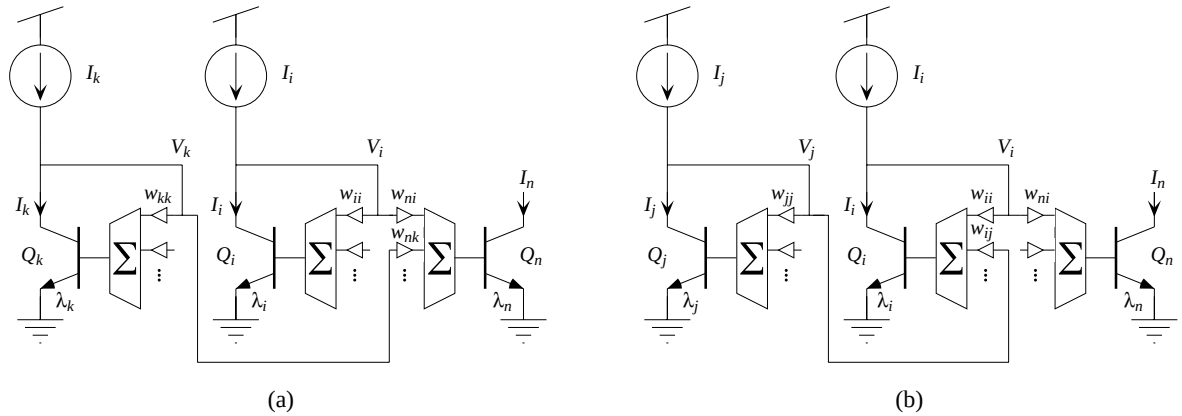

Figure 2. Two current-in, current-out circuits comprising two CIVO stages and one VICO stage. (a) A product-of-power-law circuit. (b) A quotient-of-power-law circuit.

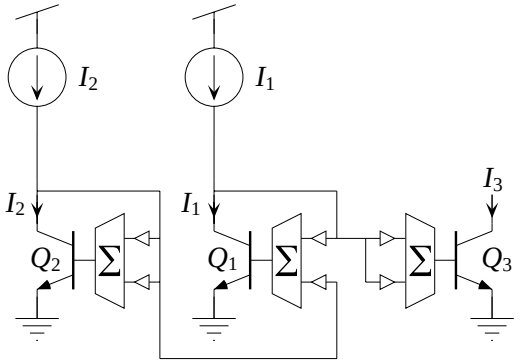

Figure 3. A squaring-reciprocal MITE network.

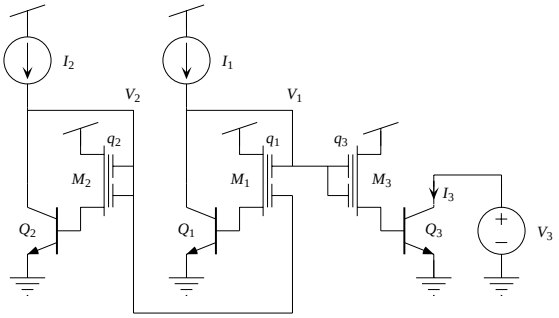

Figure 4. The squaring-reciprocal MITE network of Fig. 3 implemented with two-transistor, bipolar-FGMOS MITEs.

Substituting Eq. 5 into Eq. 9, we get

$$I_n \propto \exp\left[\frac{w_{ni}}{U_\mathrm{T}}\left(\frac{U_\mathrm{T}}{w_{ii}}\log I_i - \frac{w_{ij}}{w_{ii}}V_j - \ldots\right)\right],$$

into which we substitute Eq. 3 for V_j, and thus obtain

$$I_n \propto \exp\left[\frac{w_{ni}}{U_\mathrm{T}}\left(\frac{U_\mathrm{T}}{w_{ii}}\log I_i - \frac{w_{ij}}{w_{ii}}\left(\frac{U_\mathrm{T}}{w_{jj}}\log I_j - \ldots\right)\right)\right].$$

Now, if we break out the first two terms of the summation and regroup, we find that

$$I_n \propto \exp\left[\frac{U_\mathrm{T}}{U_\mathrm{T}}\frac{w_{ni}}{w_{ii}}\log I_i\right]\exp\left[-\frac{U_\mathrm{T}}{U_\mathrm{T}}\frac{w_{ni}}{w_{ii}}\frac{w_{ij}}{w_{jj}}\log I_j\right]. \quad (10)$$

Again, because $x\log y = \log y^x$ and $e^{\log x} = x$, we can express Eq. 10 as

$$I_n \propto I_i^{\frac{w_{ni}}{w_{ii}}} \times I_j^{-\frac{w_{ni}}{w_{ii}}\frac{w_{ij}}{w_{jj}}},$$

which, in turn, we can write as

$$I_n \propto \frac{I_i^{\frac{w_{ni}}{w_{ii}}}}{I_j^{\frac{w_{ni}}{w_{ii}}\frac{w_{ij}}{w_{jj}}}}. \quad (11)$$

Thus, the output current is proportional to the quotient of the two input currents, each raised to a power that is set by ratios of weighting coefficients. Here, the powers are not completely independent of each other—however, for any value of $\frac{w_{ni}}{w_{ii}}$, we can adjust the value of $\frac{w_{ij}}{w_{jj}}$ to set the power of I_j as desired. This quotient-of-powers relationship is also insensitive to isothermal variations.

These two basic CICO circuits capture the intuition behind all MITE networks. We generate voltages that are logarithmic in the input currents using diode-connected MITEs. We set power laws through ratios of weighting coefficients. We obtain negative powers by using voltage-inversion stages. We get products by summing two or more logarithmic voltages on MITEs. We have formalized this intuitive analysis and have obtained systematic analysis and synthesis procedures for this class of nonlinear circuits [5].

4. AN EXAMPLE AND EXPERIMENTAL RESULTS

Consider the MITE network shown in Fig. 3; note that this circuit has the same form as that of Fig. 2b. We assume that each of the weighting coefficients have the same nominal value, w. The first input current, I_1, couples into MITE Q_1

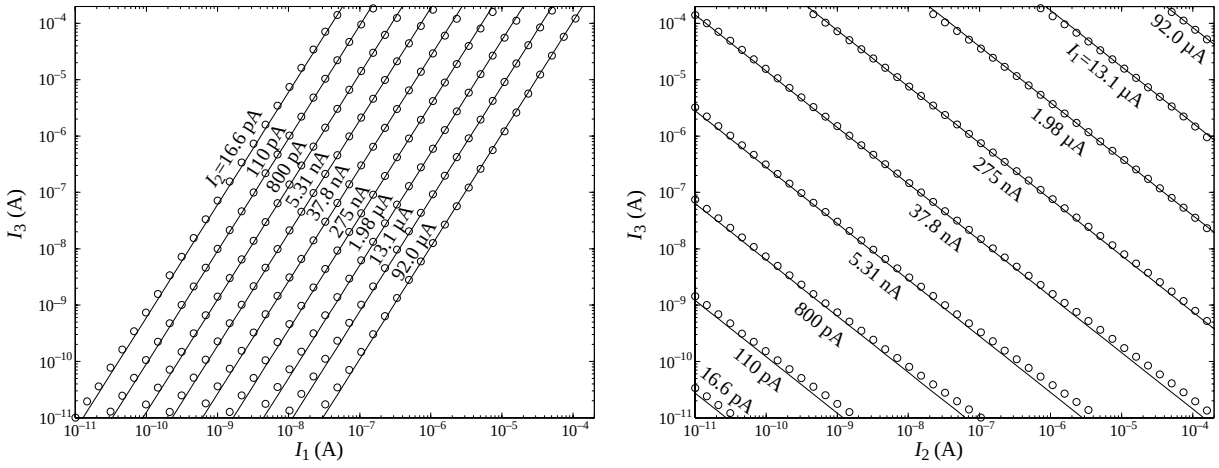

Figure 5. Measured data from the circuit of Fig. 4. Circles are measured values of I_3 plotted as a function of (a) I_1 for various values of I_2, and (b) I_2 for various values of I_1. Solid lines show the ideal expression, $I_3 = I_1^2 / I_2$, calculated for the values of I_1 and I_2 at each point.

with a weight of w and into MITE Q_3 with a weight of $2w$. Thus, from Eq. 11, we have that $I_3 \propto I_1^2$. The second input current, I_2, couples into MITE Q_2 with a weight of $2w$ and into MITE Q_3 with a weight of $2w$ through a unity-gain inverting VIVO stage (i.e., MITE Q_1). Thus, from Eq. 11, we have that $I_3 \propto I_2^{-1}$. Combining these results, we have that

$$I_3 \propto \frac{I_1^2}{I_2} .$$

Thus, the MITE network of Fig. 3 is a squaring-reciprocal circuit.

Figure 4 shows the MITE network of Fig. 3 made from three two-input, bipolar-FGMOS MITEs [5]. We breadboarded this circuit using three four-input bipolar-FGMOS MITEs that we fabricated in Orbit's 2–µm double-poly CMOS process. Then, we balanced the charge on the floating-gates by exposing them to short-wave UV light for about 20 minutes. After balancing the floating-gate charge, we measured the DC characteristics of this MITE network. The resulting data are shown in Fig. 5. The circles shown in Fig. 5a represent measured values of I_3 plotted as a function of I_1 over the nearly 7.5-decade current range from 10 pA to 200 µA for nine different values of I_2 ranging from 16.6 pA to 92.0 µA. The circles shown in Fig. 5b represent measured values of I_3 plotted as a function of I_2 over the nearly 7.5-decade current range from 10 pA to 200 µA for nine different values of I_1 ranging from 16.6 pA to 92.0 µA. In both plots, solid lines show values of the ideal theoretical expression,

$$I_1 = \frac{I_1^2}{I_2} ,$$

calculated for the values of and at each point. The data and fits agree well over much of the current range shown.

5. CONCLUSIONS

In this paper, we briefly described the intuition underlying the functioning of a class of nonlinear circuits called MITE networks. Using this intuitive understanding, we analyzed a simple squaring-reciprocal MITE network and showed experimental data from a breadboarded version of this circuit made from bipolar-FGMOS MITEs that we fabricated in a 2–µm double-poly CMOS process.

6. ACKNOWLEDGMENTS

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