Modeling and Implementation of Voltage-Mode CMOS Dendrites on a Reconfigurable Analog Platform

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***Abstract*—Many decades ago, Wilfrid Rall and others laid the foundations for mathematical modeling of dendrites using cable theory. With reconfigurable analog architectures, we are now able to accurately program different circuit architectures to emulate dendrites. Our work has shown that these circuits accurately reproduce results predicted from cable theory when inputs to the system are small. For large inputs, interesting nonlinear effects begin to take hold.**

***Index Terms*—Dendrite, field programmable analog array (FPAA), neuromorphic.**

I. The Neuromorphic Engineer's Thesis: Silicon Emulates Biology

NEUROMORPHIC engineering has garnered ever-increasing interest since Carver Mead's early explorations of the field [1]. Neuromorphic engineers claim that transistors can be used to emulate biological processes. Silicon devices and biological structures operate based on similar physical principles, so it is possible to make circuits which share many of the computational properties of neurobiological systems. There are two consequences of this statement: neuromorphic circuits can be used to natively simulate biological systems, and they can also be used to perform bio-inspired computation.

Although dendrites have typically been overlooked in terms of computation, recent results have hypothesized computational possibilities for dendritic components [2], [3]. Fig. 1 shows dendrites as the region of a neuron that connects the neuron's synapses to its soma. In order to begin to take advantage of this computation, we have verified that some of the most basic properties of dendrites can be observed using analog CMOS circuit models.

This paper explores how neuromorphic technology can be applied towards emulation of dendritic behavior. Our previous work showed the basic structure of a transistor-channel implementation [4] of a dendritic circuit [5] that has been proposed as a key component for hardware-enabled biologically-inspired classifiers [6]. To make these approaches practically usable in both neurobiological modeling as well as classification systems, we require building these systems to have careful modeling of these approaches. The classic computational model for dendritic structures comes from the work of Wilfrid Rall [7], which has been the classic model of linearized passive dendrites for decades. We present in this paper a Si transistor channel dendritic model that displays similar behavior to Rall's model of passive dendritic structures, both in the steady-state response and the dynamic response. Further, with the emergence of

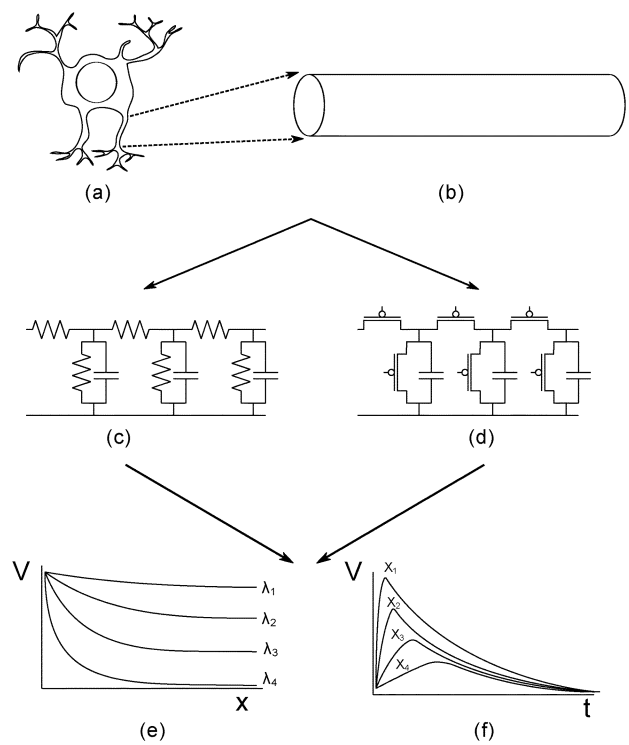

Fig. 1. When operated in the correct regime, a VLSI dendrite model produces the behavior predicted by canonical linear models. (a) Dendrites are the structures which connect synapses to the cell body. They perform linear (and sometimes nonlinear) summations of input currents. (b) Neuroscientists typically model these structures as passive linear cables. (c) The classical model for this linear cable is an equivalent RC delay line. The major predictions of linear cable theory are based on this model. (d) An alternative model for the linear cable is a network of aVLSI elements, primarily MOSFETs and capacitors, where input currents are translated into small voltage signals which swing around a DC operating point. If (c) and (d) are equivalent, they should behave similarly. (e) The steady-state behavior of both models is expected to be an exponential decay in voltage, where the amount of decay depends on physical parameters. (f) The dynamic behavior of both models is expected to be exponential decay in space and a delay in time.

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large-scale Field Programmable Analog Array (FPAA) approaches [8], we need the opportunity to compile such systems, to make these approaches widely accessible to others besides ASIC designers.

There is a long history of dendritic emulation of Rall's equations in the neuromorphic community. Elias [9] built passive compartmental models using multiple fixed IC resistors, capacitors, and MOSFET current sources, demonstrating spatial weighting of inputs, sublinear summation of nearby synapses, and tonic summation of inputs. Rasche and Douglas [10] modeled neural cable using switched capacitors and OTA leakage conductances, enabling some programmability (through clock rate, biases). They could observe changes due to these parameters, and observed propagation of action potentials down a cable. Recently, Wang and Liu [11] described a dendritic system with NMDA channels, nonlinearities, and a dendritic cable. They showed how activating NMDA channels leads to superlinear responses in the system and that these nonlinearities allow the dendrite to discriminate between input patterns with different spatial extents.

We present work on careful modeling of the dendrites on FPAA structures over the next few sections. Section II discusses the fundamental unit of computation in neuromorphic systems—the silicon channel—and states that it can be used to model biological channels. Section III overviews the hardware platform for connecting silicon channels to create more complex biological structures. Section IV discusses using this platform to bias silicon channels in a way that simulates the voltage-mode behavior of dendrites, and makes the connection to Rall's linear cable model where his model is appropriate. Section V discusses tools developed to aid in the design of dendritic circuits in an FPAA framework. Section VI overviews possible behaviors seen in the Si dendrite model that are outside the region of validity of Rall's model, but which we hypothesize are useful properties.

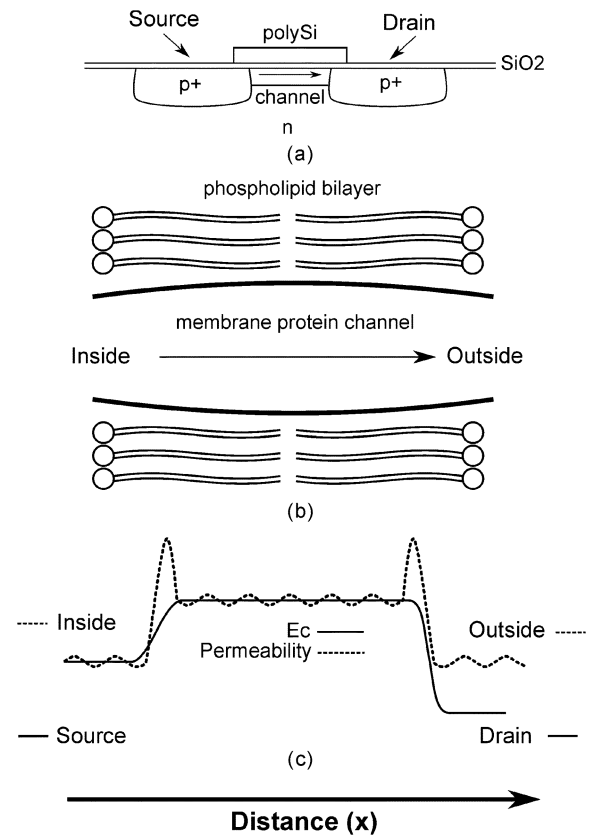


Fig. 2. (a) The physical structure of a MOSFET consists of polysilicon, silicon dioxide, and doped n-type silicon. A channel is formed between the source and the drain. (b) The physical structure of a biological channel consists of an insulating phospholipid bilayer and a protein which stretches across the barrier. The protein is the channel in this case. (c) The band diagram of silicon (solid line) has a similar shape to the classical model of membrane permeability proposed by Danielli [12] (dashed line). In both cases, carriers must overcome energy barriers in order to travel from one side of the device to the other.

II. The Silicon Channel

Neuromorphic engineering begins with the principle that the transistor acts as a biological analog. Carver Mead recognized that this is true because both silicon and biological channels behave according to the same natural principle. The channel of a transistor operated in its subthreshold regime is governed by the diffusion equation, as are many biological processes [1].

The channel of a transistor is a region of silicon that separates the drain from the source [see Fig. 2(a)]. This area forms an energy barrier to charge carriers at the source and at the drain. The number of charge carriers at the source or drain end of the channel is determined by the size of this barrier, which is modulated by the difference between the gate voltage and the source or drain voltage. Since the source is operated at a higher potential than the drain in the P-channel device, the barrier at the source end of the channel is lower, so there are more charge carriers at the source end of the channel than at the drain end. Therefore we have a gradient of charge carriers from the source end of the channel to the drain end. This is illustrated in Fig. 2(c). This means that carriers must diffuse from the source to the drain according to the diffusion equation from [1]:

$$v_{diffusion} = -D\frac{1}{N}\frac{dN}{dh} \tag{1}$$

where $v_{diffusion}$ is the velocity of carriers, D is the diffusion constant, N is the number of charge carriers per unit volume, and h is distance. When the diffusion equation is applied in the case of a gradient of charge carriers from the source to the drain of a pFET channel, the current is given in [13] as

$$\begin{aligned} I &= I_0 e^{\kappa(V_{dd}-V_g)/U_T}\left(e^{-(V_{dd}-V_s)/U_T} - e^{-(V_{dd}-V_d/U_T)}\right) \\ &= I_0' e^{-\kappa V_g/U_T}\left(e^{V_s/U_T} - e^{V_d/U_T}\right). \end{aligned} \tag{2}$$

V_{dd} is the well potential of the pFET, V_g is the gate voltage, V_s is the source voltage, and V_d is the drain voltage, all referenced to ground. I_0 is a collection of physical constants which is intuitively the saturation current when $V_g = V_s = V_{dd}$. κ is a measure of how well the gate voltage modulates the potential at the channel's surface. U_T is the thermal voltage (typically around 26 mV at room temperature). To simplify the nomenclature, we can reference the terminal voltages to V_{dd}, in which

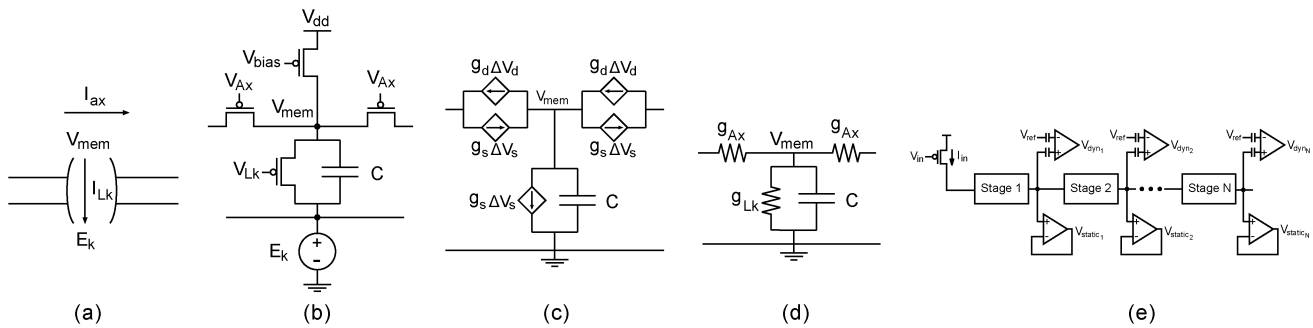


Fig. 3. Various models of a dendrite. A biological dendrite is modeled as a conductive cylinder surrounded by an insulating layer. A cross section of this model is shown in (a), where I_{ax} represents the current flowing along the axial direction of the dendrite, I_{Lk} represents current from the dendrite to extracellular fluid through a leak channel, and the internal and external potentials are V_{mem} and E_k, respectively. When we translate channels into transistors, we get the model shown in (b), where both the axial and leakage current flow through transistors. The external voltage is set by a voltage source E_k, and V_{mem} is set by the bias structure. When we linearize the transistor model, the result is shown in (c) and (d). Current sources can be reduced simply to small-signal conductances. (e) Schematic for taking measurements from the cable. Each block representing a stage consists of one bias, axial, and leakage transistor as shown in Fig. 3(b). At the output of each stage, two amplifiers relay the signal to a mux. The first is an open-loop floating-gate OTA which is used to measure step responses at each stage of the dendrite. The second amplifier is a buffer-connected OTA which is used to accurately read DC voltages for steady-state experiments.

case $I_0' = I_0$. To reference everything to ground, we let $I_0' = I_0 e^{\kappa V_{dd}/U_T} e^{-V_{dd}/U_T}$.

The idea of overcoming energy barriers to produce current is also seen in biological channels. In Fig. 2(b), we show the structure of a channel embedded in a membrane. Fig. 2(c) shows how both biological and silicon channels generate barriers to current, where the barrier is shown as a change in membrane permeability in the case of biological channels and a change in potential energy in the case of silicon channels.

III. A Reconfigurable Development Platform for Neuromorphic Systems

All of the data presented in this paper comes from a reconfigurable hardware platform that can be used to develop neuromorphic models. The Field-Programmable Analog Array (FPAA) is a mixed-signal CMOS chip which allows analog components to be connected together in an arbitrary fashion, allowing for rapid testing and measurement of many different circuit designs. The specific chip used for this paper is the RASP 2.8a [8].

The FPAA is organized into three functional blocks. The first is the Computational Analog Block (CAB), which is a physical grouping of analog circuits which act as computational elements. These elements include nFETs, pFETs, Operational Transconductance Amplifiers, capacitors, Gilbert multipliers, and others.

The interconnection of CAB components is accomplished with the FPAA's second functional block, the switch matrix. This is a collection of floating-gate pFETs which connect together rows and columns of routing lines. A floating-gate pFET is one whose gate has no DC path to ground. Voltage is applied to the gate through a capacitive divider. The lack of a DC path to ground means that once charge is stored on the gate, it will remain there without the need for a directly-applied potential. We are able to place charge on the gate and remove charge from it using the quantum mechanical processes of Fowler-Nordheim tunneling and hot electron injection.

The third functional block is the programmer, which selects a floating-gate device in the switch matrix and controls the processes of tunneling and injection to add or remove charge to the floating gate. This allows each device to be turned completely on, turned completely off, or operated somewhere in-between. This flexibility means that switch elements can be used for computation as well as routing, a benefit seen in other efficient routing applications [14], [15]. One example of a useful computational element created from floating-gates is a constant current source.

IV. Implementing the Linear Cable Model With Analog CMOS Circuits

Our basic thesis is shown in Fig. 3. We begin with the biological dendrite and model both the conductive medium and the leak channel using a silicon channel. We also provide a bias current to set the resting membrane potential, V_{rest}. We then assume small signals are applied as inputs, and our circuit reduces to a linear model.

A. Introduction to Linear Cable Theory

The simplest model neuroscientists use to describe the function of dendrites is known as the Linear Cable Model. The dendrite is treated as a conductive core surrounded by an insulating layer. The core is modeled as a long piece of resistive material, which can be discretized into many incremental resistances R_{Ax}. The insulating layer is a phospholipid bilayer, and it is modeled as a capacitance C because it separates the internal membrane potential from the extracellular potential. However, there is leakage current from the intracellular solution to the outside of the cell, so a leakage resistance R_{Lk} is also included in the model.

Koch gives a simple derivation of the mathematical cable model for this circuit in [16]. If one writes down Kirchhoff's Current Law (KCL) at the nodes V_{mem} and uses Ohm's Law $V = IR$ and the capacitor equation $I = C(dV/dt)$, then the following differential equation describes the system:

$$\lambda^2 \frac{\partial^2 V_{mem}}{\partial x^2} = \tau \frac{\partial V_{mem}}{\partial t} + V_{mem} - R_m I_{inj} \tag{3}$$

where I_{inj} is current injected into the dendrite, $\tau = R_{Lk}C$ and $\lambda = \sqrt{R_{Lk}/R_{Ax}}$. τ and λ are called the time constant and

the space constant. Intuitively, τ determines how voltages along the dendrite change with time, and λ determines how voltages change with distance down the dendrite. If we only care about the steady-state solution, we can set the differential with respect to time equal to zero. This results in a solution for the steady-state behavior given in (4)

$$V(x) = V_0 e^{-|x|/\lambda}. \tag{4}$$

B. Using Silicon Channels to Implement the Linear Cable Model

Our goal is to replace the resistances in the linear cable model with silicon channels. The most intuitive way to do this is to simply replace each resistance with a single pFET. The axial resistances are replaced with a pFET whose gate is set at a fixed potential, V_{Ax}. Similarly, the membrane resistances are replaced with pFETs whose gates are set at a fixed potential V_{Lk}. On an intuitive level, the conductance of the pFETs is set by their gate voltage. We will need to bias the dendrite at a fixed membrane potential, so a transistor which provides a DC bias current is inserted into each node of the dendrite. It has a gate voltage V_{bias}, and it sets the DC point V_{mem}. The final piece of the dendrite to consider is the capacitance. It is a fact of analog circuits that every node has some capacitance associated with it. So we do not have to place an explicit capacitance at each node to simulate a dendrite. If we so desire, the FPAA has the ability to compile 500 fF capacitances into the nodes. The final circuit is as shown in Fig. 3(b).

In order to model an equivalence to the linear cable model, we can simplify the full circuit into a linear one. Each transistor is replaced with a small-signal, linearized model. To do this, we take partial derivatives of the current equation for a pFET as formulated in (2).

Linear Model of Axial FET: In the operation of the circuit, we will leave the gate fixed at a DC bias, so we can simplify (2) by incorporating the gate voltage term into $I_{bias} = I_0' e^{-\kappa V_g/U_T}$. Therefore, the current through the axial and leakage pFETs can be expressed as follows:

$$I = I_{bias}\left(e^{V_s/U_T} - e^{V_d/U_T}\right).$$

Traditionally, we form a linear model for this device by taking the partial derivative of the current with respect to a changing terminal voltage. Since a signal is traveling in the axial direction of our dendrite, both the source and the drain of the axial FET are changing. We model this with two current sources in parallel pointing in opposite directions, with the values $g_s \Delta V_s$ and $g_d \Delta V_d$. Ignoring channel length modulation, the values for g_s and g_d are given in [13] as

$$g_s = \frac{\partial I_{Ax}}{\partial V_s} = \frac{I_{bias}}{U_T} e^{V_s/U_T}, \quad g_d = -\frac{\partial I_{Ax}}{\partial V_d} = \frac{I_{bias}}{U_T} e^{V_d/U_T}.$$

Note that, at rest, the dendrite will be biased such that all source and drain nodes of the axial pFETs will be at the same rest potential, V_{rest}. This means that $g_s = g_d$. We can combine the two current sources into one source with the value

$$I = g_{Ax}\Delta V_s - g_{Ax}\Delta V_d = g_{Ax}\Delta V_{sd}.$$

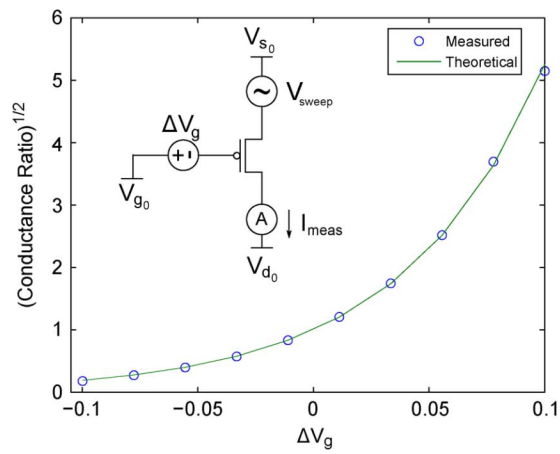


Fig. 4. Demonstration that the ratio of source conductances is a function of the difference between gate voltages. We took a CAB pFET and measured a reference source conductance by fixing the DC potential at all of its terminals (V_{s_0}, V_{g_0}, and V_{g_0}), and measuring the DC current. We then swept its source voltage through a very small range (V_{sweep}) and measured the change in current. The reference conductance was the slope of change in current with respect to change in source voltage. We performed this same experiment for ten different values of the gate voltage ($V_{g_0} - \Delta V_g$). We then plotted the square root of the ratio of source conductances as a function of the gate voltage. We used the difference in gate voltages to create a theoretical value of the conductance ratio from Eq. (7), and the two match very closely.

So this is simply a small-signal conductance,

$$g_{Ax} = \frac{I_{bias_{Ax}}}{U_T} e^{V_{mem}/U_T}. \tag{5}$$

Linear Model of Leakage FET: Modeling the leakage transistor is much easier. Both the gate and the drain are fixed to DC voltages. So any change in voltage across the device is completely due to a change in the source. Therefore, the small-signal conductance of the leakage FET is just the source conductance, as given above

$$g_{Lk} = \frac{I_{bias_{Lk}}}{U_T} e^{V_{mem}/U_T}. \tag{6}$$

Deriving the Space and Time Constants: The space constant is the parameter λ in the linear cable equation which describes how voltage in the dendrite decays with position along the dendrite. It is related to the ratio of the axial and leakage conductances. Now that we have linearized our model, we can define a space constant λ by taking the ratio of our conductances

$$\lambda \equiv \left(\frac{R_{Lk}}{R_{Ax}}\right)^{1/2} = \left(\frac{I_{bias_{Ax}}}{I_{biasLk}}\right)^{1/2} = e^{\frac{\kappa(V_{Lk}-V_{Ax})}{2U_T}}. \tag{7}$$

Fig. 4 verifies this expression experimentally using the FPAA. We measured how the conductance of a pFET changes as a function of its DC gate potential. To relate this back to (7), we measure a reference conductance and see how changing the gate voltage affects the square root of the ratio of the new conductance to the reference.

The time constant τ describes how voltages decay with time. It is defined as the product of the leakage resistance and the capacitance, or

$$\tau = \frac{C}{g_{Lk}} = \frac{CU_T}{I_{bias_{Lk}}} e^{-V_{mem}/U_T}. \tag{8}$$

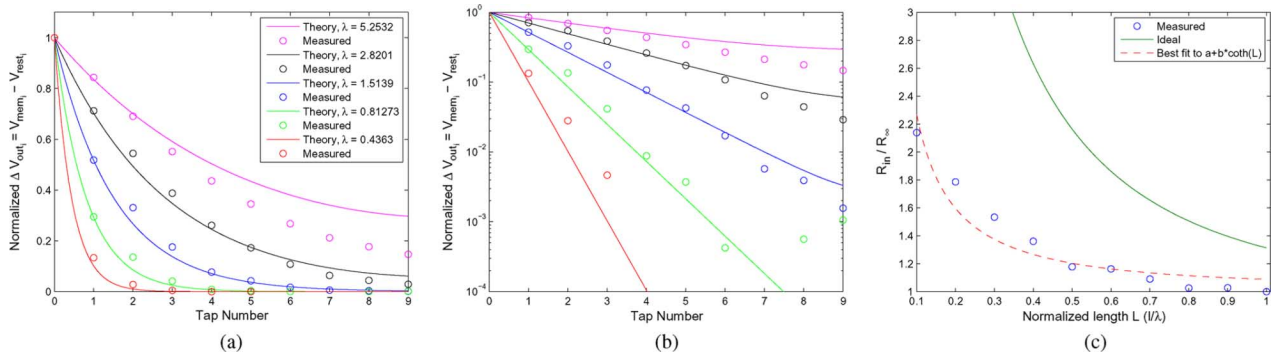


Fig. 5. (a) and (b) Steady-state decay of dendrite voltage. For five different values of λ, a ten-stage dendrite was biased at DC such that the V_{mem} nodes were about 20–50 mV above $E_k = 1$. Then a small DC current was injected into the first node. We then measured $\Delta V_i = V_{mem_i} - V_{rest_i}$ for every node in the dendrite. Then ΔV_i was normalized. The dots are experimental measurements, and the lines represent how the voltages should decay if λ matches the theoretical value perfectly. The theoretical values essentially predict the "slope" of the logarithmic response, and not the actual DC offset. This is why the normalized predictions are accurate for low values of stage number and seem to deviate as stage number increases. We're seeing error in the slope but not DC offset. The linear plot gives an intuitive physical feel for how the dendrite behaves, while the logarithmic plot demonstrates how these are approximately exponential responses. The log plot also shows how error in slope accumulates. Please note that any changes which were negative (all of which were small) are not shown on the log plot. (c) This plot shows how input resistance changes as dendrite length is increased. A fixed input current was injected into Node 1 of the diffusor, and the membrane voltage at that node was measured before and after injection. We then calculated the difference between these two ($V_{delta} = V_{mem} - V_{rest}$). This was done for many different dendrite lengths. To calculate R_{in}/R_{∞}, we divided all values of V_{delta} by the value for $\mathrm{L} = 1$. Since the injected current was the same for all tests, the ratio of resistances is therefore the ratio of the voltage responses. The response did not follow the quantitatively predicted curve, but it does demonstrate qualitative behavior similar to what we expect, as shown by the dashed curve, which is a curve fit to $\mathrm{a} + \mathrm{b} \times \coth(\mathrm{L})$.

Sources of Error: The above expressions hinge on perfect matching among all pFET devices. This unfortunately is rarely achieved. We measured the values of κ and I_0 for a sample of 15 pFET CABs in the FPAA and measured the statistical variation for these two parameters. This information is shown below

	μ	σ
κ	0.8393	0.0021
I_0	$4.5740fA$	$0.77549fA$

The above analysis assumes the system is processing "small" signals. We can no longer assume that the linear models behave if they are perturbed far from the DC bias. We limited inputs to the system such that the source nodes of the vertical pFETs never changed by more than 25 mV.

V. Demonstrating Equivalence to the Linear Cable Model

We now wish to demonstrate that our voltage-mode circuit retains many of the behaviors of a passive dendrite. We set up our cable using the system shown in Fig. 3(e).

Steady-State Experiments: The first test to perform is a steady-state analysis. In our experiment, we compiled a 10-stage dendrite onto the FPAA. We set $E_k = 1$ V and biased the membrane voltage to around 20 mV above E_k. Due to mismatch among the bias transistors and leak transistors, not all membrane voltages were exactly the same, and they could vary by as much as tens of mV. We attempted to compensate for some of the mismatch by an iterative process of measuring and changing the bias voltages on the gates of the I_{bias} transistors, but this did not remove all of the mismatch. Since this is a dendrite of finite length, the steady-state solution takes on a slightly different form than that given earlier. From [16], the solution is

$$V(X) = V_0 \frac{\cosh(L - X)}{\cosh(L)} \tag{9}$$

where $\mathrm{X} = \mathrm{x}/\lambda$ and $\mathrm{L} = \mathrm{l}/\lambda$. For this experiment, we defined the steady-state voltage of a particular node as the difference between its measured rest voltage and its voltage after applying an input. The results for this dendrite are given in Fig. 5(a) and (b).

The input resistance of a semi-infinite, sealed-end cable is also well-known. Its expression is given in [16] as

$$R_{in} = R_{\infty} \coth(L). \tag{10}$$

As L increases, R_{in} approaches R_{∞}. To test whether our dendrite follows this model, we applied a step input current of I_0 to our dendrite and varied the value of λ. For a fixed input current but variable dendrite length, we can predict what the voltage should be at various points along the dendrite. Our results are shown in Fig. 5(c).

Our theoretical results do not perfectly match the data, and there are a few possible reasons for this. Probably the largest contributor to the problem is biasing the dendrite correctly. For the experiments in Fig. 5(b) and (c), the resting membrane potentials were as much as 30 mV away from each other. The ratio of small-signal conductances is $e^{(\Delta V/U_T)}$, so this means that the ratio of two ideally matched conductances could be as high as 3.32. It should also be noted that κ changes with the source voltage, so a 30 mV mismatch in source voltage could also affect κ.

Dynamic Experiments: Cable theory provides us with a prediction for what the shape of the step response should look like at the site of current injection. The form is given in [16] as

$$V_{Step}(0, T) = \frac{I_0 R_{\infty}}{2} erf(\sqrt{T}). \tag{11}$$

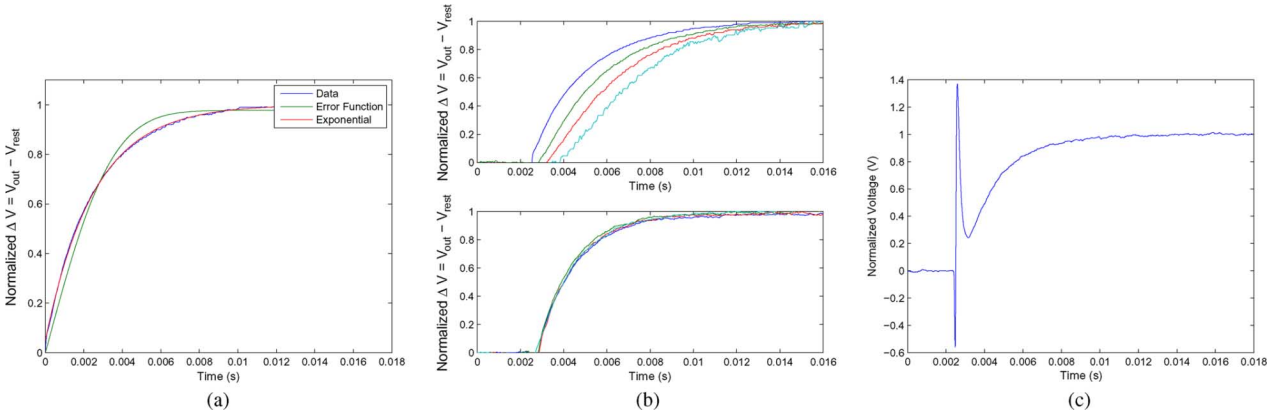


Fig. 6. (a) Step response for the first node of a diffusor, along with the best fit to the error function and an exponential function. The step response was obtained by setting the value of V_{ref} on the first node's floating-gate OTA such that V_{dyn_1} was midrail. Then the input current was pulsed, and the waveform was captured. We experimentally determined how much to pulse V_{in} by alternatively pulsing it, measuring how much the first node's voltage changed, and adjusting the gate until the first node's voltage changed by less than U_T, or 25 mV. We chose this value since the FETs would leave saturation if the source voltage changed by much more. We normalized the result by subtracting the DC offset and dividing by the maximum value reached. Linear cable theory predicts that the error function will be a closer fit than the exponential, but the data for our system mirrors an exponential response much more closely. It is possible that our step size was greater than needed to keep all devices in their linear regimes. (b) Step responses for four taps of the dendrite were taken for two different values of λ. For a small value of λ, the velocity of propagation is small, so one can see delays of the response as they travel down the dendrite. For higher values of λ, the velocity of propagation is very fast, so very little delay can be seen. Fig. 6(c) shows parasitic transients not visible in this figure. (c) Two parasitic effects seen at once for one particular step response. When the gate of the pFET is pulsed down, some of that voltage change is coupled into the input node of the dendrite, and therefore initially the voltage at the membrane decreases. This change can be seen propagating along the system. For this step response, we also see a spike upwards. This is likely due to capacitive coupling into the instrumentation amplifier (a floating-gate input OTA), because this change is not seen propagating down the dendrite in other plots.

We have plotted a representative step response for $x = 0$ along with a best-fit line to this theoretical function in Fig. 6(a).

Since the cable model is basically an RC network, we expect to see delay down the line. The propagation velocity of a step input down the line is given in [16] as

$$v = 2\frac{\lambda}{\tau}. \tag{12}$$

This means that we can increase the delay down the line (decrease the velocity of propagation) by decreasing λ or increasing τ. In our experiment, we changed λ and looked at how the velocity of propagation was affected. The results are shown in Fig. 6(b).

In both the steady-state and dynamic experiments, we have seen a trend in our results. Namely, they agree with cable theory qualitatively but do not match it precisely, quantitatively. We do not expect these nonidealities to affect usability of the dendrites greatly. This is because we believe the computation in dendrites is not governed by precise tuning of every parameter. Neural computation is inherently different from the von-Neumann architectures in which precision is key. They exhibit high levels of stochastic behavior, redundancy, and recurrent connections. Rather, for us it was more more important to see that the basic dendritic properties can be varied over a wide range, allowing gross tuning of parameters.

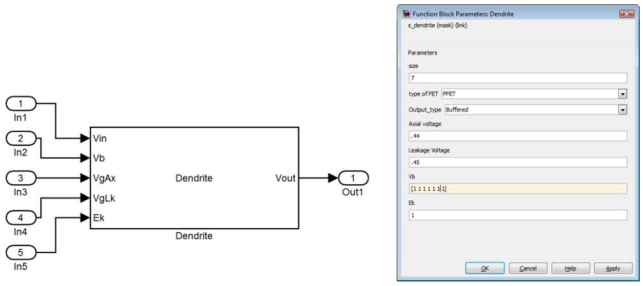
Effects of a Reconfigurable Testbed: A reality of working in a reconfigurable environment is that parasitics can cause nonidealities to crop up when experiments are run. Fig. 6(c) demonstrates this. To apply an input current to our system, the gate of a pFET is pulsed low. This pulse can capacitively couple both into the system and into the instrumentation measuring the system's response. The amount of coupling depends on how the system is routed, so certain care should be made to ensure that system components are routed to minimize such effects. For instance, the routing lines for the voltage measurement circuitry should not be physically close to the digital pulse on the gate of the input current source. Additionally, a cascode should be used on the input current source.

VI. Simulink Model for Simulating CMOS Dendrites and FPAA Configuration

For DSP and neuromorphic engineers with little or no hardware experience, it is beneficial to have a software tool that can provide an easy interface with the hardware. MATLAB Simulink allows users to add new blocks with user-defined functionality, providing the user an interactive graphical interface. DSP engineers are familiar with this tool to a large extent. Keeping this in mind, we developed a Simulink model for dendrites. The Dendrite Simulink block provides users with a block-level interface. Sim2spice [17] is the compiling tool we used to convert the block-level implementation to a Spice netlist. The GRASPER tool [18] is then used to configure the FPAA and the RAT tool [19] is used to view and edit the routing. The user can also simulate the behavior of dendrites.

Dendrite Simulink Block: The dendrite Simulink block is defined by level-2 M file S-funcions and corresponding netlist elements. The elements used to model the block are the CAB elements on the FPAA. The input parameters for the block are configurable. The Simulink block can be used to run a behavioral simulation of the CMOS dendrites and also generate a Spice netlist to configure the FPAA. It consists of mainly four files.

1) S-function Simulink block: Consists of the physical dendrite block with its inputs, outputs and other input parameters that need to be defined. It is the user-interface block as illustrated in Fig. 7(a). The input parameters that the user can specify are given in Fig. 7(b).
2) Matlab(.m) build script: Builds the spice netlist for the block.



(a) (b)

Fig. 7. (a) Dendrite Simulink Block. This is a fully connected block with five inputs, which are the biasing voltages required for the dendritic line and the output port which denotes the voltage at every tap. (b) Block parameter window for the Dendrite Simulink Block. The window asks users to specify input parameters needed for the block. The user is asked to specify the number of stages, the type of FET used (PFET/FG-PFET), if the output should be buffered or not, and the biasing voltages required for the circuit.

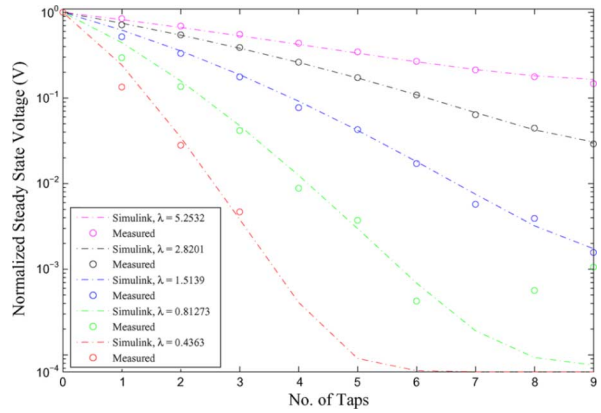


Fig. 8. Comparing Simulation results to data obtained using the FPAA. After modifying the I_0 parameter, injected current, and node capacitance, the two normalized curves have similar qualitative behavior.

3) Description file(.desc): Defines list of paramters needed by the parser.
4) Simulink(.m) behavior file: Simulates dendrites in Simulink using the mathematical model based on the device physics of the silicon devices.

Behavioral Modeling: The Simulink block simulates the behavioural characteristics of the dendrite structure. This provides the user an insight to the working of the dendritic circuit when implemented using the FPAA. The MOSFET parameters used are based on the MOSFETS present on the FPAA. It is characterized by coupled Ordinary Differential Equations (ODE) and solved using the ODE solver ode-45. The model has been tested for both static as well as time-varying inputs and has given reasonable results. We present below a detailed analysis of the mathematical model used, based on the device physics of silicon.

Consider a dendritic line as given in Fig. 3, with n number of nodes. Current is injected only at the first node and the axial and leakage conductances are the same throughout. Applying KCL at node 1, the injected current and the bias current are the sum of the axial and the leakage currents. The leakage current comprises of the current through the leakage capacitor and the leakage transistor. Applying KCL at node 2; the current through the first axial conductance equals the current through the second axial conductance, the leakage conductance, and the leakage capacitance.

Taking into account the boundary conditions, we can write a general expression for the node voltage in a vector form as,

$$\begin{aligned}\frac{d\vec{V}}{dt} = \frac{1}{C}(&a_1 \cdot I_{inj} + k_1(e^{a_2 \cdot \vec{V}/U_T} - e^{a_3 \cdot \vec{V}/U_T}) \\ &+ k_1(e^{a_4 \cdot \vec{V}/U_T} - e^{a_5 \cdot \vec{V}/U_T}) \\ &+ k_2(e^{a_6 \cdot \vec{V}/U_T} - e^{E_k/U_T}) + I_{bias})\end{aligned} \tag{13}$$

where,

$$\vec{V} = [V_1 \quad V_2 \quad V_3 \quad \ldots \quad V_n].$$

a_1, a_2, a_3, a_4, a_5 and a_6 are constant matrices whose size is dependent on the number of stages of the dendrite, C is the leakage capacitance and k_1 and k_2 are variables that are dependant on the axial and leakage conductances. In our experiments V_{Ax_n} and V_{Lk_n} are the same for all nodes, so k_1 and k_2 are the same for all nodes. Writing the equations in vector form is useful as it reduces the time required for Matlab computation. We define all the constants in the equations based on the MOSFETS used on the FPAA $(\kappa, I_0, \mathrm{C})$ along with the input parameters as defined for the block (V_{Lk}, V_{Ax}, E_k).

Results: We simulated a 10-stage dendrite using the Simulink Dendrite block. The nodes are biased at 1.02 V and a current is injected into the first node. The parameters used for the axial and leakage transistors are $\kappa = 0.8464$ and $I_0 = 0.05$ fA. For the bias transistors, $\kappa = 0.72$ and $I_0 = 0.45$ fA. The node capacitance was 70 pF, and the injected current was 5 pA. These simulation settings differ from our steady-state experiment in three ways. The input current is different from experiment, the node capacitance is higher than in experiment, and I_0 differs from the experimental I_0 by one or two orders of magnitude. We believe the higher capacitance was needed in order to allow the simulation to reach its steady-state results more quickly. Once the above parameters have been changed for best agreement, the average error between the normalized data and the simulation is 16.8%. The results are shown in Fig. 8.

VII. Nonlinear Behavior of Dendrites

Most of this paper has concerned the behavior of the dendritic circuit operated in its linear regime. When the input current becomes large, however, the qualitative behavior of the circuit changes, and nonlinear effects begin to take hold. Typically, a difference between drain and source of about $4U_T$, or 100 mV is typically considered the nonlinear regime of the dendrite. In order to get a qualitative understanding of the nonlinear effects, we will analyze one "section" of dendrite, shown in Fig. 9(a).

A. Math Modeling

Applying KCL and the current equations for a capacitor and a saturated transistor,

$$\frac{dV_s}{dt} = \frac{I_{in}}{C} - \frac{I_{bias}}{C} e^{V_s/U_T}. \tag{14}$$

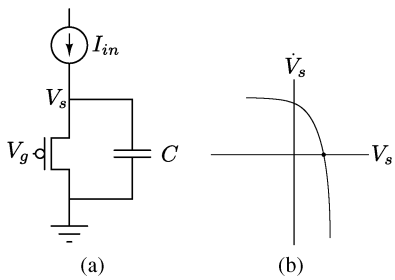


Fig. 9. (a) Illustration of nonlinear dynamics in dendrite circuit. A large-signal input current is sent into a node which sees a transistor and capacitor in parallel. (b) Illustration of the phase portrait resulting from the circuit in Fig. 9(a). The input current moves the line vertically, which changes the qualitative behavior of the system.

We can use (14) to plot a phase portrait. The basic shape is a negative exponential with a vertical offset, shown in Fig. 9(b).

This portrait gives us quantitative and qualitative information about our circuit's voltage response to an input current. First, it gives us the voltage where we expect V_s to settle:

$$V_s = U_T \ln \frac{I_{in}}{I_{bias}}. \tag{15}$$

Second, the picture tells us that we will get small time constants for large values of I_{in}. Note from (14) that the vertical offset of this plot is determined by the value of I_{in}. As I_{in} increases, the plot is shifted up, and the rate at which V_s changes for a given value of V_s will be increased, thus decreasing the time constant. It is also important to point out that the slope of the actual phase portrait is much steeper than what we drew in Fig. 9(b). This means that a shift up in the plot won't affect the steady-state value of V_s as much as it will affect the time constant.

B. Demonstration of Impact on Dendrite Circuit Behavior

If we apply a large enough input current such that the membrane voltage changes by more than 100 mV, we can measure the effects of nonlinear input currents on the dendrite.

Our first experiment was to see how the steady-state voltage decays, as shown in Fig. 10(a). The result is that the voltage decays linearly with space. This is a desirable effect, since it is essentially a compression operation. Recall that, for small inputs, the steady-state voltage decayed exponentially. If this trend were to continue for large inputs, the dynamic range of available voltages would be severely limited. However, for a large input, the FETs are no longer operating as resistors; they are in saturation, so we merely require linear changes in voltage to achieve exponential changes in current. Therefore the dendrite is using nonlinearity to increase its dynamic range.

Our second experiment is to see how the shape of the step response changes with an increase in input current. We can rewrite (16) in the current domain. Defining $I_1 = I_{bias} e^{V_s/U_T}$, we can differentiate with respect to time to get $\dot{I}_1 = I_1/U_T \dot{V}_s$. Substituting into (14),

$$\begin{aligned} I_{in} &= \frac{CU_T}{I_1}\frac{\partial I_1}{\partial t} + I_1 \\ \frac{\partial I_1}{\partial t} &= \frac{I_1}{CU_T}(I_{in} - I_1). \end{aligned} \tag{16}$$

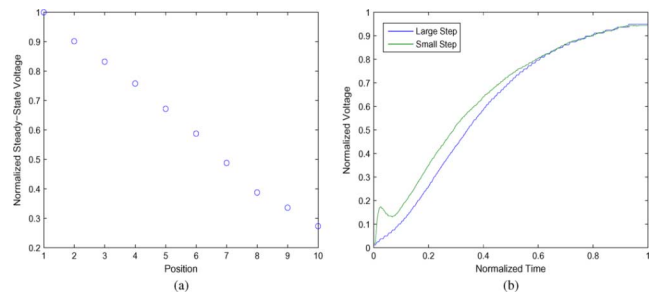


Fig. 10. (a) When the steady-state response of a 10-stage dendrite is measured with a large input current (causing a change of about 200 mV at the first node), the response is a linear degradation in voltage. (b) Comparing shapes of small step and large step response. The step response was normalized in voltage by dividing by the steady-state value, and time was normalized by finding the point at which the voltage rises to 95% of its steady-state value. The initial response of the small step is more of an RC response, while the large step shows a sigmoidal behavior. See Fig. 6(c) for a discussion of the transient at the beginning of the small step.

When (16) is solved, it behaves like a tanh function, so we expect the shape of our dendrite's step response to be sigmoidal for large current steps. Our results in Fig. 10 bear this out.

VIII. Implementing Dendrites in Large Reconfigurable Systems

A. Difficulties of Floating-Gate Diffusors

Modeling floating-gate dendritic circuits is more complicated than with regular FETs because the capacitive coupling from the source and drain to the floating-gate is more pronounced than with regular pFETs. In order to design a floating-gate dendrite, characterizing these coupling ratios is necessary. We need to know coupling ratios because floating-gate transistors are programmed with their terminal voltages at one potential in "program mode" and then undergo a change in "run mode," when the circuit is operating. An example of a floating-gate diffusor not behaving as expected is shown in Fig. 11(a).

The simplest way to characterize the capacitive coupling is to perform sweeps of each terminal and extract an "effective κ" for that terminal. Then if we have a desired membrane potential, we know how the floating-gate voltage will be affected. Once we know that floating-gate voltage, we can attempt to program the bias transistor to match the current it is drawing.

A second nonideality is due to the FPAA's "indirect programming" scheme. Methods to characterize these effects are discussed in detail in [20].

B. Benefits of Floating-Gate Diffusors

The most exciting aspect of dendritic circuits is that they can be made in an extremely compact manner. As we stated above, the switch matrix of the RASP 2.8a FPAA is made up of floating-gate switches. So there is potential to make huge arrays of dendrites using the switch matrix. Fig. 11(b) is an example of how such a diffusor might be made. Partitioning of the switch matrix allows for a large number of dendrites to be created.

We can estimate how large these dendrites can be based on the FPAA routing structure. Each CAB has an associated floating-gate switch matrix. The equivalent number of useful columns per CAB is 14. For CAB types 1 and 2, the number of available

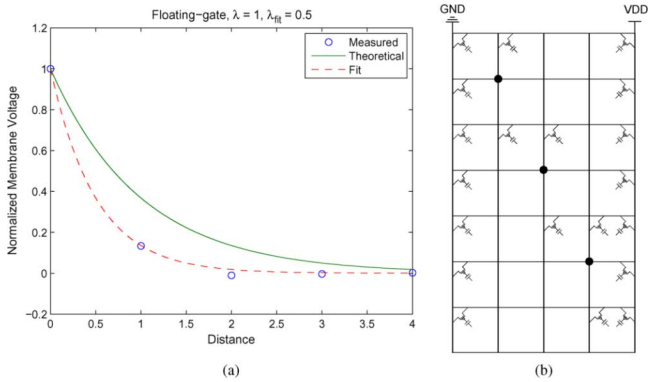


Fig. 11. (a) Illustration of offsets introduced by capacitive coupling from the drain of the diffusor. (b) Possible method of placing dendrite in switch matrix. In a switch matrix, a floating-gate transistor exists at every intersection of two wires which can short a horizontal line and vertical line. In this representation, an intersection with a black dot represents wires which have been shorted together with a floating-gate transistor. A picture of a transistor represents a floating-gate which is part of the diffusor structure and is programmed somewhere between open and closed circuit. No graphic at an intersection represents a floating-gate which has been programmed open-circuit. The leftmost column has been shorted to ground, and all the transistors connected to it are the vertical devices in the diffusor. The rightmost column has been shorted to V_{DD}, and all the transistors connected to it are the biasing devices. The pairs of two floating-gates in the middle are the horizontal transistors which connect the vertical legs together.

rows is 24 and 34. If we make a dendrite as shown in Fig. 11(b), each row connects to one vertical transistor, and each column connects to two horizontal transistors. We estimate that CAB types 1 and 2 can implement dendrites of approximately 24 and 28 stages.

It is also important to point out that neural systems are inherently imprecise. So the disadvantages listed above are not necessarily detriments. Some amount of variability from dendrite-to-dendrite caused by floating-gate transistor mismatch could be seen as a good thing. In fact, the inability to precisely model the behavior could be an asset, for it requires designers to get an intuitive feel for what parameters work well for a given system.

IX. Conclusion

We have seen mathematical modeling and behaviors that connect, for small inputs, to Rall's modeling for passive dendritic structures. For large inputs, we see deviations from Rall's model that we hypothesize could be useful properties. We experimentally demonstrated these results on an FPAA to create a voltage-mode CMOS dendrite.

This research builds a foundation to utilize these dendritic structures as computational primitives. Simple dendritic computations have been proposed for a long time, such as coincidence detection and boolean operations [2], [3]. Previously, we gave an early proposal that dendrites could be used to aid HMM-like classification [6]. We hope to leverage these units for useful classification and discrimination systems. Further, the inclusion of active channels, such as NMDA synapses and Na or Ca channels, enables dendrites to respond more strongly to a sequence of input events, which should have a powerful effect on understanding the computation of dendritic structures [21], [22].

References

[1] C. Mead, *Analog VLSI and Neural Systems*. Reading, MA: Addison-Wesley, 1989.
[2] C. Koch and I. Segev, "The role of single neurons in information processing," *Nature Neurosci.*, vol. 3, pp. 1171–1177, Nov. 2000.
[3] M. London and M. Hausser, "Dendritic computation," *Annu. Rev. Neurosci.*, vol. 28, pp. 503–532, Jul. 2005.
[4] E. Farquhar and P. Hasler, "A bio-physically inspired silicon neuron," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 52, no. 3, pp. 477–488, 2005.
[5] E. Farquhar, D. Abramson, and P. Hasler, "A reconfigurable bidirectional active 2 dimensional dendrite model," in *Proc. IEEE Int. Symp. Circuits and Systems*, 2004, vol. 1, p. I-313.
[6] P. Hasler, S. Koziol, E. Farquhar, and A. Basu, "Transistor channel dendrites implementing hmm classifiers," in *Proc. IEEE Int. Symp. Circuits and Systems*, 2007, pp. 3359–3362.
[7] I. Segev, J. Rinzel, and G. M. Shepherd, *The Theoretical Foundation of Dendritic Function: Selected Papers of Wilfrid Rall With Commentaries*. Cambridge, MA: MIT Press, 1995.
[8] A. Basu, S. Brink, C. Schlottmann, S. Ramakrishnan, C. Petre, S. Koziol, F. Baskaya, C. Twigg, and P. Hasler, "A floating-gate-based field programmable analog array," *IEEE J. Solid-State Circuits*, vol. 45, pp. 1781–1794, 2010.
[9] J. G. Elias, "Artificial dendritic trees," *Neural Comput.*, vol. 5, pp. 648–663, 1993.
[10] C. Rasche and R. J. Douglas, "Forward- and backpropagation in a silicon dendrite," *IEEE Trans. Neural Netw.*, vol. 12, no. 2, pp. 386–393, Mar. 2001.
[11] Y. Wang and S.-C. Liu, "Input evoked nonlinearities in silicon dendritic circuits," in *Proc. IEEE Int. Symp. Circuits and Systems*, 2009, pp. 2894–2897.
[12] B. Hille, *Ion Channels of Excitable Membranes*, 3rd ed. Sunderland, MA: Sinauer Assoc., 2001.
[13] S.-C. Liu, J. Kramer, G. Indiveri, T. Delbruck, and R. Douglas, *Analog VLSI: Circuits and Principles*. Cambridge, MA: MIT Press, 2002.
[14] C. Twigg, J. Gray, and P. Hasler, "Programmable floating gate fpaa switches are not dead weight," in *Proc. IEEE Int. Symp. Circuits and Systems*, May 2007, pp. 169–172.
[15] E. K. F. Lee and W. L. Hui, "A novel switched-capacitor based field-programmable analog array architecture," *Analog Integr. Circuits Signal Process.*, vol. 17, no. 1–2, pp. 35–50, 1998.
[16] C. Koch, *Biophysics of Computation*. New York: Oxford Univ. Press, 1999.
[17] C. Petre, C. Schlottmann, and P. Hasler, "Automated conversion of simulink designs to analog hardware on an fpaa," in *Proc. IEEE Int. Symp. Circuits and Systems*, May 2008, pp. 500–503.
[18] F. Baskaya, D. Anderson, P. Hasler, and S. K. Lim, "A generic reconfigurable array specification and programming environment," in *Proc. Euro. Conf. Circuit Theory and Design*, Aug. 2009, pp. 619–622.
[19] S. Koziol, C. Schlottmann, A. Basu, S. Brink, C. Petre, B. Degnan, S. Ramakrishnan, P. Hasler, and A. Balavoine, "Hardware and software infrastructure for a family of floating-gate based fpaas," in *Proc. IEEE Int. Symp. Circuites and Systems*, May 2010, pp. 2794–2797.
[20] S. Shapero and P. Hasler, "Precise programming and mismatch compensation for low power analog computation on an fpaa," *IEEE J. Emerging Selected Topics Circuits Syst.*, submitted for publication.
[21] T. Branco, B. A. Clark, and M. Hausser, "Dendritic discrimination of temporal input sequences in cortical neurons," *Science*, vol. 329, no. 5999, pp. 1671–1675, Sep. 2010.
[22] A. Destexhe, "Dendrites do it in sequences," *Science*, vol. 329, no. 5999, pp. 1611–1612, Sep. 2010.