Neural Dynamics in Reconfigurable Silicon

Arindam Basu, *Member, IEEE*, Shubha Ramakrishnan, *Graduate Student Member, IEEE*, Csaba Petre, *Graduate Student Member, IEEE*, Scott Koziol, *Graduate Student Member, IEEE*, Stephen Brink, and Paul E. Hasler, *Senior Member, IEEE*

***Abstract*—A neuromorphic analog chip is presented that is capable of implementing massively parallel neural computations while retaining the programmability of digital systems. We show measurements from neurons with Hopf bifurcations and integrate and fire neurons, excitatory and inhibitory synapses, passive dendrite cables, coupled spiking neurons, and central pattern generators implemented on the chip. This chip provides a platform for not only simulating detailed neuron dynamics but also uses the same to interface with actual cells in applications such as a dynamic clamp. There are 28 computational analog blocks (CAB), each consisting of ion channels with tunable parameters, synapses, winner-take-all elements, current sources, transconductance amplifiers, and capacitors. There are four other CABs which have programmable bias generators. The programmability is achieved using floating gate transistors with on-chip programming control. The switch matrix for interconnecting the components in CABs also consists of floating-gate transistors. Emphasis is placed on replicating the detailed dynamics of computational neural models. Massive computational area efficiency is obtained by using the reconfigurable interconnect as synaptic weights, resulting in more than 50 000 possible 9-b accurate synapses in 9 mm^2.**

***Index Terms*—Bifurcations, central pattern generator, dendritic computation, ion-channel dynamics, neuromorphic system, spiking neurons.**

I. Reconfigurable Analog Neural Networks: An Introduction

THE MASSIVE parallelism offered by very-large-scale integrated (VLSI) architectures naturally suits the neural computational paradigm of arrays of simple elements computed in tandem. We present a neuromorphic chip with 84 bandpass positive feedback (e.g., transient sodium) and 56 lowpass negative feedback (e.g., potassium) ion channels whose parameters are stored locally in floating-gate (FG) transistors. Hence, fewer but detailed multichannel models of single cells or a larger number (maximum of 84) of simpler spiking cells can be implemented. The switch matrix is composed of FG transistors that not only allow arbitrary topology of networks, but serve as synaptic weights since their charge can be modified in a continuum. This serves as a classic case of "computation in memory" and permits all to all synaptic connectivity (with a total of more than 50 000 of these weights in the 3 mm $\times$ 3-mm chip). In this context, we reiterate that the chip is reconfigurable and programmable; reconfigurability refers to our ability to compile different circuits by changing connections while programmability refers to changing the parameters of any of these circuits. Other components in the CABs also allow building integrate and fire neurons, winner-take-all circuits, and dendritic cables, making this chip a perfect platform for computational neuroscience experiments. Moreover, since this chip produces real-time analog outputs, it can be used in a variety of applications ranging from neural simulations to dynamic clamps and neural interfaces.

Several systems have been reported earlier where a number of neurons were integrated on a chip with a dense synaptic interconnection matrix. Though these chips definitely accomplished the tasks they were intended for, large-scale hardware systems modeling detailed neuron dynamics (e.g., Hodgkin-Huxley, Morris-Lecar, etc.) seem to be lacking. One attempt at solving this problem is presented in [1]. However, the implemented chip had only ten ionic channels and 16 synapses, with a large part of the chip area devoted to analog memory for storing parameter values. Another approach reported in [2] had four neurons and 12 synapses with 60% of the chip area being occupied by digital-analog converters for creating the various analog parameters.

In the following sections, we describe the architecture of the chip and the interface for programming it. Then, we present measured data showing the operation of channels, dendrites, and synapses. Finally, we show some larger systems mimicking central pattern generators or cortical neurons and conclude in the final section with some remarks about the computational efficiency, accuracy, and scaling of this approach.

II. System Overview

A. Chip Architecture

Fig. 1(a) shows the block-level view of the chip which is motivated by the framework in [3]. Since we presented architectural descriptions of similar chips earlier, we do not provide details about the architecture here, but note that the CAB components in our realization are neuronally inspired in contrast to the chip in [3] which had analog-processing components. Another unique feature of this chip is that we exploit the switch interconnect matrix for synaptic weights and dendritic cables. There are 32 CABs organized in a 4 $\times$ 8 array, each CAB occupying 244 μm $\times$ 122 μm. The first row of CABS has bias generators which can produce bias voltages that can be routed along

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A. Basu is with the School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore 639798 (e-mail: arindam.basu@ntu.edu.sg).

S. Ramakrishnan, C. Petre, S. Koziol, S. Brink, and P. E. Hasler are with the Department of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA 30332-250 USA.

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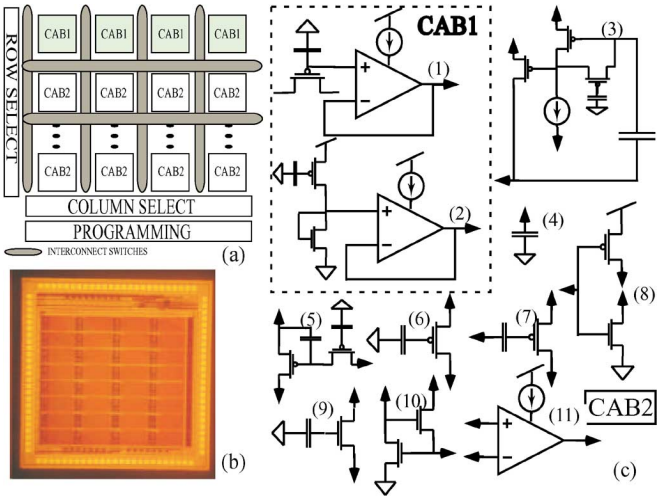

Fig. 1. **Chip Architecture**: (a) The chip is organized into an array of 4×8 blocks that can be interconnected using FG switches. (b) Die photo of the chip fabricated in 0.35 μmm CMOS. (c) CAB components that are used for computation along with the switch matrix elements. The tunneling junctions and programming selection circuitry for the floating gates are not shown for simplicity. The arrows on the components denote nodes that can be connected to other nodes through routing.

columns for all of the computational CABs. It should be noted that the regular architecture allows for tiling multiple chips on a single board to make larger modules. Fig. 1(b) is a die photo of the fabricated chip.

Fig. 1(c) shows the components in the CAB. The components ① and ② in the dashed square are in CAB1. In both cases, the floating gates are programmed to a desired level and the output voltage is buffered using a folded-cascode operational transconductance amplifier (OTA). The bias current of the OTA can also be programmed, allowing the amplifiers to be biased according to the application, thus saving power. As mentioned earlier, the CABs in the first row are of this type.

In CAB2, ③ and ⑤ are the positive feedback and negative feedback channels, respectively. In the context of Hodgkin–Huxley neurons, they are the sodium and potassium channels, respectively. However, from the viewpoint of dynamics, these blocks could represent any positive feedback (or amplifying [4]) inward current and negative feedback (or resonant) outward current. ⑪ is a programmable bias OTA which is included because of its versatility and omnipresence in analog processing. ④ is a 100-fF capacitance that is used to emulate membrane capacitance. Different magnitudes of capacitance are also available from the metal routing lines and OFF switches. One input of a current mode winner-take-all block is formed by ⑩ . A synapse following the implementation in [5] can be formed out of ⑥, ⑦, ⑧, and ⑨ and will be detailed later. The reason for choosing such a granularity is primarily component reuse. For example, component ⑧ can also be used as a variable current sink/source or a diode-connected field-effect transistor (FET) while component ⑥ can be used as a leak channel.

B. Software Interface

Fig. 2 depicts the processing chain used to map a circuit to elements in the chip. A library containing different circuits (sodium channel, winner-take-all, dendrite, etc.) is used to create a larger system in Simulink, a software product by The Mathworks. The circuits in the library correspond to preconstructed SPICE subcircuits whose parameters can be set through the Simulink interface. New blocks can also be added to the library by the user. The graphical user interface (GUI) mentions whether the input/output (I/O) ports are voltage or current mode and the user should connect only ports with the same type of signal. Though the current version of the software does not check for signal compatibility, the next generation of software being developed does include this feature.

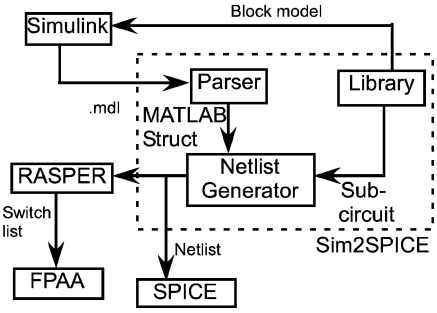

Fig. 2. Software interface: flow of information from the Simulink level of abstraction to SPICE, finally resulting in a list of switches and biases to be programmed on the chip.

A first code converts the Simulink description to a SPICE netlist, while a second one compiles the netlist to switch addresses on the chip. The methodology is borrowed from [6] and [7] and we refer the reader to it for details. The second level of compilation also provides information about the parasitic capacitance associated with each net for that particular compilation. The user can simulate this parasitic annotated SPICE file, and, if desired, can recompile his/her circuit. The possible modifications include changing the circuit parameters or placing the components in a way that reduces the routing parasitic. This simulation of the Simulink models can be performed using MATLAB's ODE solver based on our computation models of spiking neurons and synapses. However, in this paper, we do not discuss the computational models anymore and focus on intuitive explanations instead.

III. Spiking Neuron Models

A. Hopf Neuron

Fig. 3(a) shows the circuit for a Hodgkin–Huxley-type neuron consisting of a sodium and a potassium channel. For certain biasing regimes, the neuron has a stable limit cycle that is born from a Hopf bifurcation, the details of which are available in [8]. In this case, we have biased the potassium channel so that its dynamics are much faster than the sodium (M3 acts as an ON switch). Hence, the potassium channel acts like a leak channel. The whole system now becomes a 2-D set of differential equations since the dynamics of V_{mem} follow that of the sodium channel. The parameters of the sodium channel are set based on voltage clamp experiments on it (not shown here).

It is important to understand that these neurons have different computational properties when compared with integrate and fire neurons. For example, the frequency of spikes does not

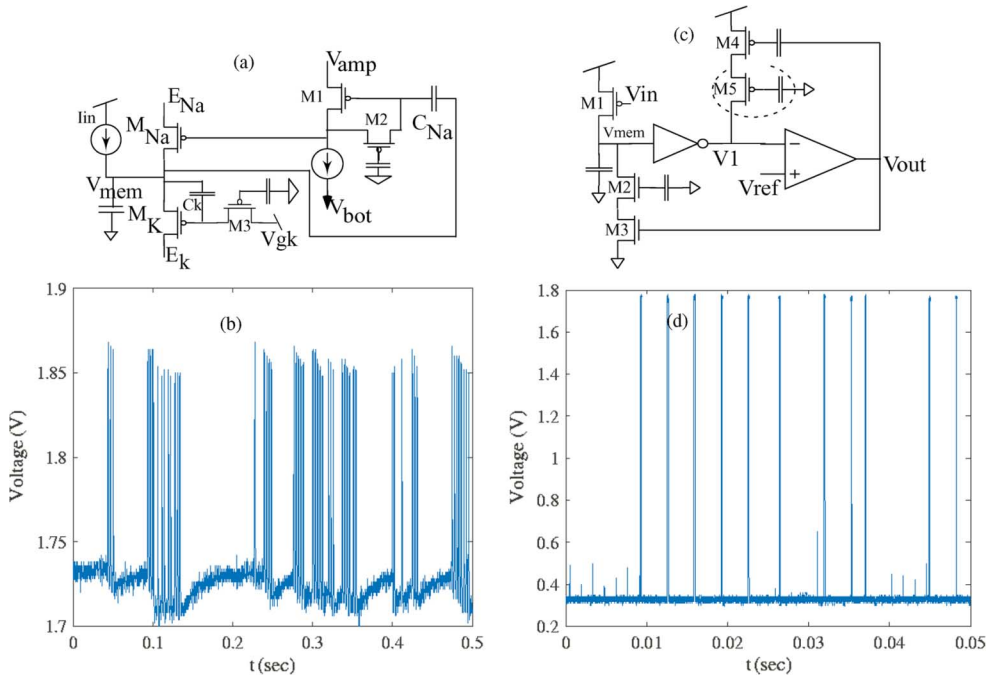

Fig. 3. Spiking Neuron. (a) Neuron model where spiking is initiated by a Hopf bifurcation. (b) Measured noise-induced spikes when the neuron in (a) is biased at the threshold of firing. (c) Integrate and fire neuron with the hysteresis obtained using M4 and M5. Here, the circled transistor, M5, is a switch element. (d) Measured noise-induced spikes when the neuron in (c) is biased at the threshold of firing.

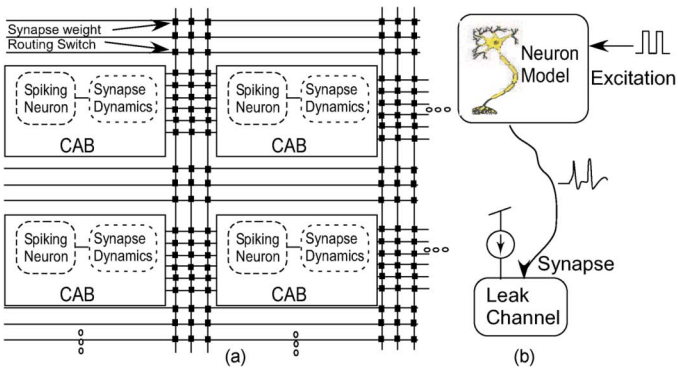

Fig. 4. Synapse architecture. (a) The synapse dynamics block for both excitatory or inhibitory synapses are placed in the CAB along with the model of the soma. The synapse weight is set by the interconnect network. (b) The test setup for the experiment has an excitable neuron with a synaptic connection to a leak channel that is biased by a current source.

reduce to zero as the bifurcation value is reached, a classical property of type II neurons [4]. Also, synchronization properties and phase-response curves of these neurons are significantly different from integrate and fire neurons. Hence, it is an indispensable component of a library of neuronal components. Fig. 3(b) shows a measurement of noise-induced spikes from a Hopf neuron biased at the threshold of firing. Note that the magnitude of the action potentials is similar to biology, thus opening the possibility of using the chip for interfacing with live neurons.

B. Integrate and Fire Neuron

Fig. 3(c) shows the circuit used for an integrate and fire neuron. The circuit has a hysteresis loop-based relaxation oscillation when the input current is large enough. The inverter exhibits hysteresis because of the feedback from M4 and M5. M4 and M5 act as a current source $I_{\rm hyst}$ when $V_{\rm out}$ is low, while it is turned OFF when $V_{\rm out}$ is high. M5 is a routing element that sets the value of $I_{\rm hyst}$ while M4 acts as a switch. The trip point of the inverter depends on the condition of $V_{\rm out}$, leading to hysteresis. The time period of the relaxation oscillations is given by

$$T = \frac{V_{\rm hyst}}{I_{in}} + \frac{V_{\rm hyst}}{I_{\rm in} - I_{\rm reset}} \tag{1}$$

where $V_{\rm hyst}$ is the magnitude of the hysteresis loop in terms of the membrane voltage, and $I_{\rm reset}$ is the reset current controlled by M2 and M3. It can be seen that the frequency of oscillations in this case does reduce to zero as $I_{\rm in}$ reduces to zero, akin to a type I neuron. This system can also be modeled by a differential equation with two state variables. Fig. 3(d) shows the output of this circuit due to noise when it is biased at the threshold of firing.

IV. Synapse

In this section, we describe three possible methods of implementing synaptic dynamics in the chip. The overall architecture is depicted in Fig. 4(a). Every CAB has a spiking neuron and a circuit to generate the dynamics of a postsynaptic potential (PSP). This node can now be routed to other CABs having other neurons. The FG switch that forms this connection is, however, not programmed to be fully ON. Rather, the amount of charge programmed onto its gate sets the weight of this particular connection that is accurate to 9 b. Hence, all of the switch matrix transistors act as synaptic weights, facilitating all to all connectivity in the chip.

Fig. 4(b) shows the setup for measuring the dynamics of the chemical synapse circuit. A neuron is biased so that it elicits

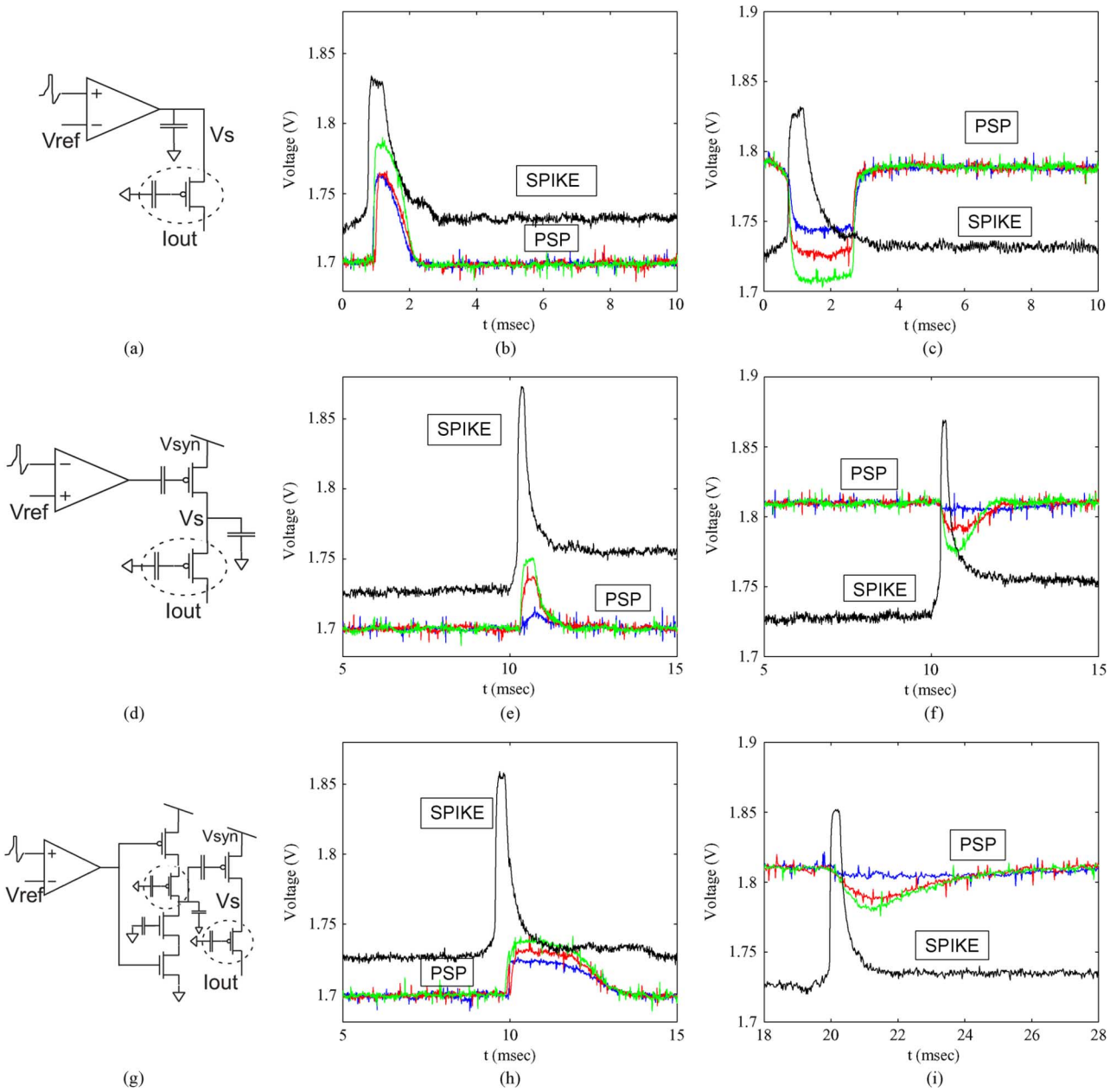

Fig. 5. Synapse. Three possible chemical synapse circuits. The circled transistor represents a switch element. PSP for three different weight values are shown. (a)–(c) The simplest excitatory synapse where reversing the positive and negative terminals of the amplifier changes it to an inhibitory synapse. (d)–(f) The amplifier acts as a threshold and switches a current source ON/OFF. The value of $V_{\rm syn}$ relative to the membrane potential makes it inhibitory or excitatory. (g)–(i) Similar to (d) with better control on the shape of the PSP waveform because of the current-starved inverter governing the charging and discharging rates independently.

an action potential when a depolarising current input is applied to it. This neuron has a synaptic connection to a passive membrane with a leak conductance where the PSP is measured. Out of the many possible synaptic circuits possible, we only show three here due to a lack of space. All of these circuits have the dynamics of a 1-D differential equation. Unlike these chemical synapses, electrical synapses are almost instantaneous and can be modeled by a floating-gate PMOS. We have also measured these circuits and their effects in synchronization of spiking neurons but do not discuss them here.

Fig. 5(a) depicts the simplest type of excitatory synaptic circuit. The amplifier creates a threshold at $V_{\rm ref}$ and charges or discharges the node V_S when the input voltage crosses the threshold. Depending on the charge on the floating-gate switch element (circled transistor), a certain amount of current is then incident on the postsynaptic neuron. The synapse becomes inhibitory if the input is applied to the negative terminal of the amplifier. We show measured data for both cases for three different synaptic weights in Fig. 5(b) and (c).

Fig. 5(d) shows the second circuit for a chemical synapse and measured results for the same. Here, the amplifier creates a digital pulse from the action potential. This switches the floating-gate PMOS current source ON which charges the node V_S while the second FG routing element sets the weight of the connection. The synapse is excitatory when $V_{\rm syn}$ is larger than the resting membrane potential and inhibitory otherwise.

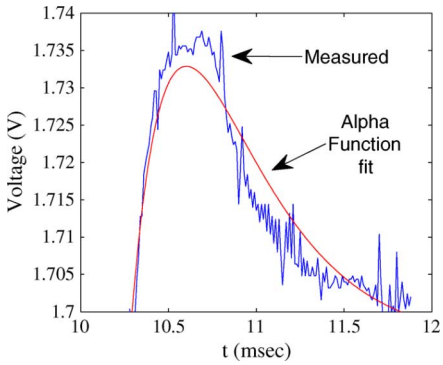

Fig. 6. Rall's alpha function: Rall's alpha function is fit to one of the EPSP plots from the earlier experiment with a resulting error of less than 10%.

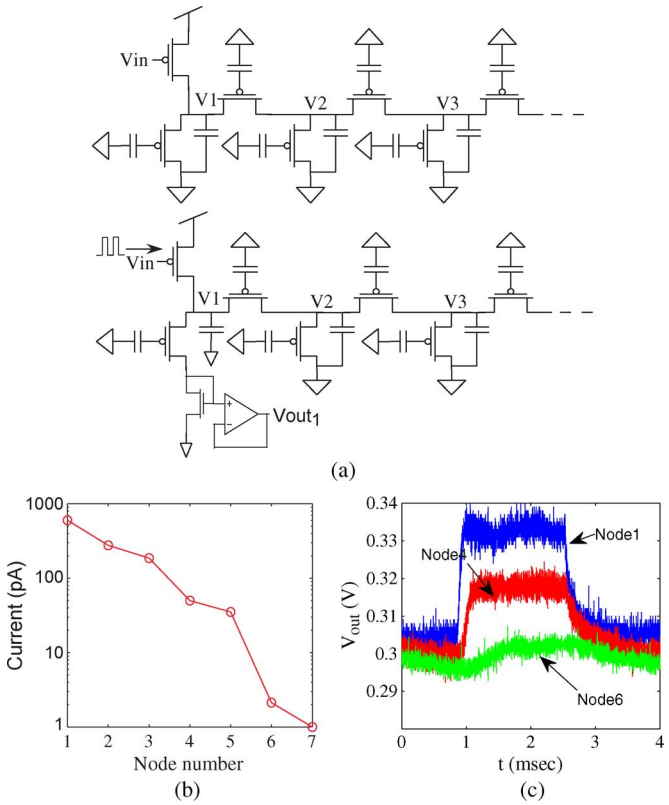

Fig. 7. Dendrite model. (a) Model of a passive dendrite based on a diffuser circuit and the experimental setup for measuring the transient response of a dendrite cable. The current through the desired node is converted to a voltage using the diode-connected NMOS. (b) Steady-state currents in a seven-tap diffuser. (c) Step responses at nodes 1,4, and 6 of a seven-tap diffuser showing progressively more delay.

Fig. 5(g) shows the circuit which replicates the synaptic dynamics most accurately [5]. After the amplifier thresholds the incoming action potential, the current-starved inverter creates an asymmetric triangle waveform (controlled by the FG PMOS and NMOS) at its output. The discharge rate is set faster than the charging rate leading to postsynaptic potentials that decay very slowly. Again, we show EPSP and IPSP waveforms for three weights of the synapse in Fig. 5(h) and (i). The waveforms shown are close to the ones recorded for actual neurons [9]. A

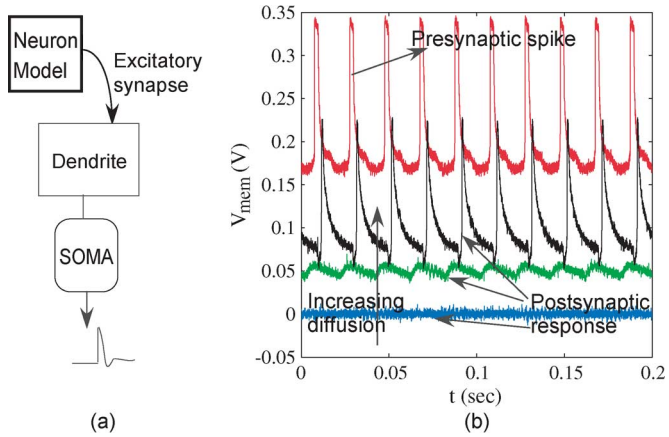

Fig. 8. Full neuron. (a) A spiking neuron is connected to another neuron through an excitatory synapse. The postsynaptic neuron in this case has a dendritic tree. (b) The diffusion length of the dendrite is slowly increased in the experiment. Though the postsynaptic neuron did not respond initially, increasing the diffusion resulted in visible EPSP waveforms and eventual spiking. Absolute voltages are not shown in this figure.

common method for modeling PSP is using Rall's alpha function as follows:

$$V_{\mathrm{PSP}}(t) = V_{\max}\alpha t e^{(1-\alpha t)}. \tag{2}$$

Fig. 6 shows a curve fit of such an alpha function to a measured EPSP waveform with an error that is less than 10%.

It should be noted that when using these synapses with integrate and fire neurons, the amplifier used for thresholding is not needed as it is part of the neuron circuit.

V. Dendrite

The circuit model of a dendrite that we use is based on the diffuser circuit described in [10]. This is one of the circuits built entirely on the routing fabric and fully exploits the analog nature of the switches. Fig. 7(a) shows the circuit and a modified version used to measure the different branch currents. The horizontal transistors connecting the nodes V_x allow diffusion of currents while the vertical transistors leak current to a fixed potential from every node. The dynamics of an n-tap diffuser circuit are represented by a set of n-dimensional differential equations which approximate a partial differential equation. The steady-state solution of the equation is exponentially decaying node currents as the distance of the node from the input node increases.

Fig. 7(b) plots the steady-state current through the compartments of a seven-tap diffuser. Fig. 7(c) shows the responses of a seven-tp diffuser. Voltages at the first, fourth,and sixth nodes are plotted here. The delayed response of the distant nodes is typical of dendritic structures. The effect of the changing diameter in dendrites can also be modeled in these circuits by progressively changing the programmed charge on the horizontal devices along the diffuser chain.

We can put together all of previous circuit elements by creating a spiking neuron that has a synapse connecting it to

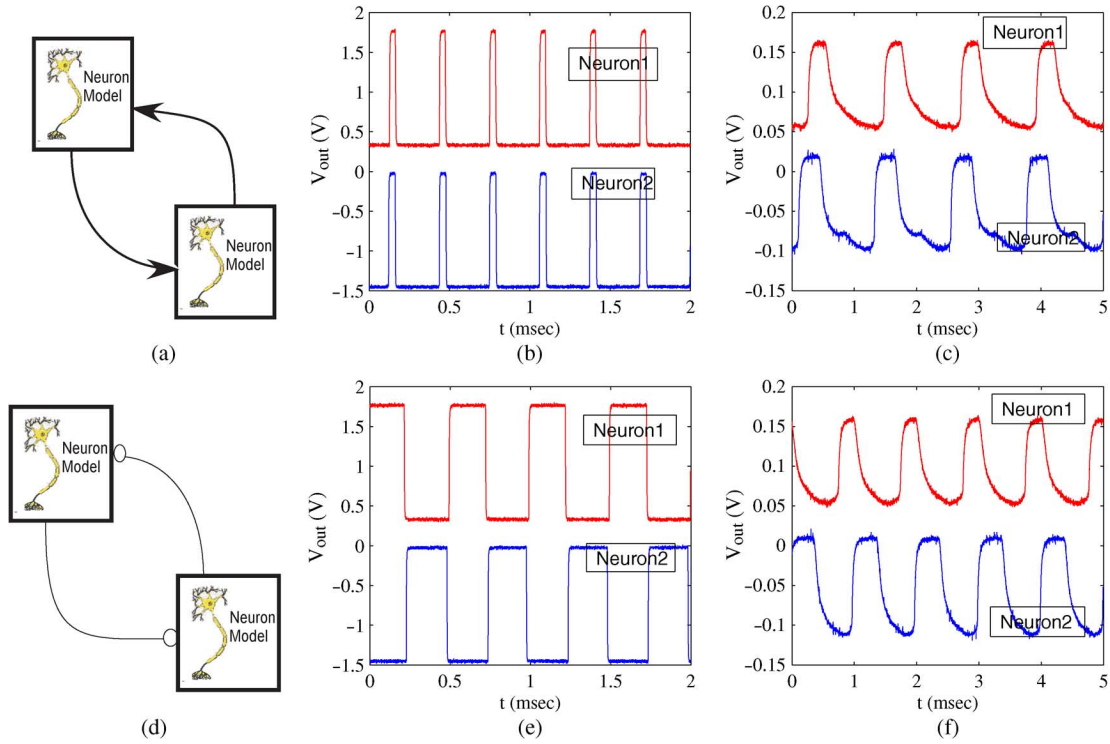

Fig. 9. Coupled oscillators. (a) and (d) Two neurons coupled by excitatory and inhibitory connections. (b) and (e) Measured output from integrate and fire neurons coupled with excitatory and inhibitory synapses. (c) and (f) Measured output from Hopf neurons coupled with excitatory and inhibitory synapses. Absolute voltage values not shown.

the dendritic tree of another neuron. Fig. 8(a) shows a picture depicting this experimental setup, the results of which are presented in Fig. 8(b). We can see that initially the postsynaptic neuron does not respond to the input spikes. However, increasing the dendritic diffusion results in visible postsynaptic potentials. Increasing the diffusion even more allows the postsynaptic neuron to fire in synchrony with the presynaptic one.

VI. Larger Systems

Spiking neurons coupled with synapses have been the object of considerable study over several years. While there are theories showing the existence of associative oscillatory memory [11] in networks of coupled spiking neurons, a lot of work has been devoted to looking at the simplest case of two coupled neurons and their role in generating rhythms for locomotion control [12]. The most popular circuit in this regard is the half-center oscillator where the neurons are coupled with inhibitory synapses. Here, we look at both cases [i.e., when the connections are inhibitory or excitatory as shown in Fig. 9(a) and (d)]. Intuitively, when the connections are excitatory, both neurons will try to fire at the same time, leading to inphase spikes. On the other hand, when the connection is inhibitory, the spiking of one neuron suppresses that of the other, giving rise to spikes out of phase. This phenomenon and its relation to synaptic strength can be studied better by transforming the differential equation into a phase variable. We can transform the equations using the moving orthonormal coordinate frame theory [13] and keep the first-order approximation of a perturbation analysis to obtain

$$\dot{\phi}_i = \alpha_i + \varepsilon \sum_{j \neq i} H_{ij}(\phi_i - \phi_j), \quad \phi \epsilon S^1 \tag{3}$$

where ε is the synaptic strength and α_i are frequency deviations from a nominal oscillator. For two oscillators, it can be seen that for a given frequency deviation, there is a fixed point only if ε is larger than a certain minimum value. In practice, no two spiking neurons have same frequency of oscillation even at the same biasing because of mismatch. So, in experiments, we slowly increased the synaptic strength until the oscillators synchronized. Fig. 9(b), (e), (c), and (f) shows the measured spiking waveforms obtained from integrate and fire neurons and Hopf neurons, respectively. We can see that in one case, the neurons are spiking inphase while they are antiphase in the other. All of these measurements were made with synapses of the first kind discussed earlier. They can be performed with different synaptic dynamics to analyze the effect of synaptic delay on synchronization properties of type I and II neurons. Detailed dynamics of escape and release phenomenon [14] can also be observed.

Fig. 10(a) shows the schematic for a central pattern generator for controlling bipedal locomotion [12] or locomotion in worm-like robots [15]. It consists of a chain of spiking neurons with inhibitory nearest neighbor connections. We implemented this system on our chip with Hopf neurons connected with the simple synapses described earlier. The resulting waveforms are displayed in Fig. 10(b). The current consumption of the neuron

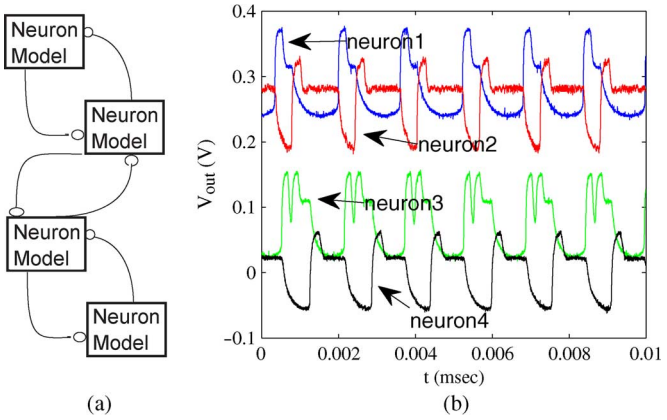

Fig. 10. Central pattern generator. (a) A set of four neurons coupled to its nearest neighbors with inhibitory connections. This models the central pattern generator in many organisms [12], [15]. (b) Measured waveforms of the four Hopf neurons showing different phases of oscillations. Absolute voltages are not shown.

in this case is around 180 nA and the synapse dynamics block consumes 30 nA of current leading to a total power dissipation of around 0.74 μW (excluding power for biasing circuits and buffers to drive off-chip capacitances). The low power consumption of the computational circuits and biological voltage scales make this chip amenable for implants.

The second system we present is a spiking neuron with four dendritic branches that act as a spike-sequence detector. Fig. 11(a) shows the schematic for this experiment. In this experiment, the dendrites were chosen to be of equal length and the neuron was biased so that input from any dendrite did not evoke an action potential. Since the neuron is of the Hopf type, it has a resonant frequency, the inverse of which we can call a resonant time period. Input signals that arrive at the soma at time intervals separated by the resonant time period and its multiples have greater chances of evoking action potentials since their effects add in phase.

Fig. 11(b) shows the pattern of inputs applied. Cases 1 to 3 shows three instances of input pulses with increasing time difference t_d between them. We show the case when the three pulses are on the same dendrite but the same experiment has been performed with input pulses on different dendrites too. Fig. 11(c) plots the resulting membrane potential for different values of t_d. For case 1, the small value of t_d leads to aggregation of the EPSP signals, making the neuron fire an action potential. This behavior is similar to a coincidence detector. When t_d is very large as in case 3, the EPSP signals are almost independent of each other and do not result in a spike. However, at an intermediate value of the time difference, we do observe multiple spikes because of the inphase addition of the EPSP (Case 2). The reason for this behavior is that the value of t_d in this case is close to the resonant time of the Hopf neuron as mentioned earlier. The lengths of the dendrite segments can be modified so that the neuron spikes only when the inputs on the different branches are separated by specific time delays. This serves as one example of possible dendritic computation.

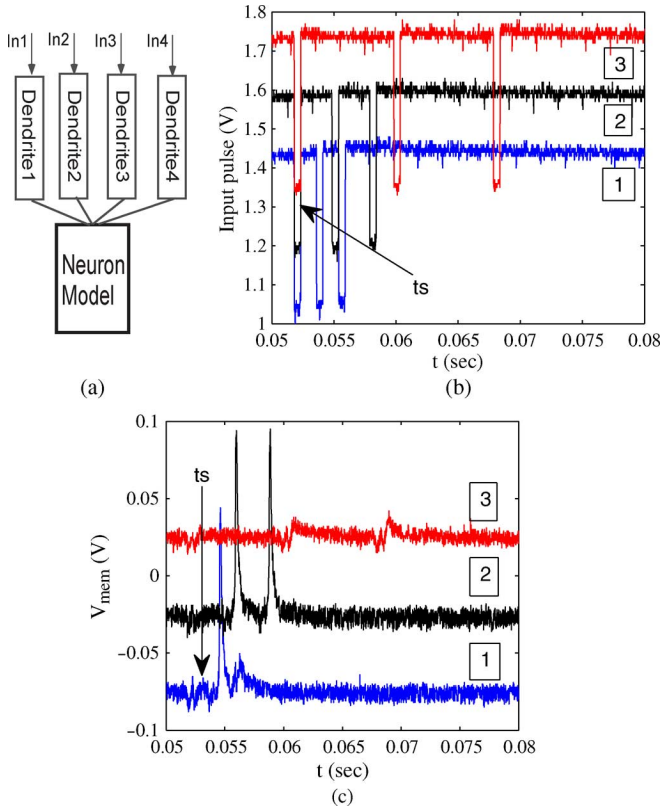

Fig. 11. Coincidence detector. (a) Schematic of a neuron with four different inputs incident on four dendritic branches. (b) This figure is indicative of the timing relationships between the input pulses (voltages are shifted for better viewing). t_s indicates the time when the first pulse was applied. (c) When the time delay between inputs is small, we see the classical aggregation of EPSP leading to a spike in case 1 while there is no spike in case 3 because of the large time delay between input pulses. Case 2 shows multiple spikes since the Hopf neuron is most excitable when the interpulse interval is close to the resonant time of the neuron. Absolute voltage is not shown here.

VII. Discussions

Having described several circuits and systems that can be implemented on the chip in earlier sections, we now discuss a few aspects relating to the computational efficiency, accuracy, and scaling of this reconfigurable approach.

A. Computational Efficiency

The efficacy of the analog implementation can be appreciated by considering the effective number of computations it is performing. Let us consider the case of the central pattern generator presented in the last section. In this case, we can model the whole system by a set of differential equations and compute the number of multiply-accumulate (MAC) operations needed to perform the same computation on a computer. We consider an RK fourth-order integrator (neglecting possible numerical problems because of multiple time scales) with a time step of 20 μs (since the spiking activity is on a scale of milliseconds). There are five function evaluations per integration step with around 40 MAC needed for every function evaluation (cosh, exp etc.). There are at least 12 state variables in this system (two per neuron and one per synapse dynamics block), leading

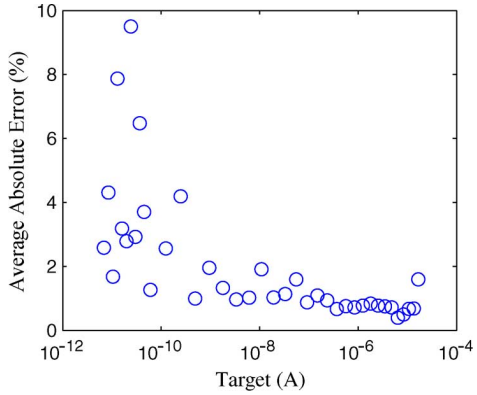

Fig. 12. Programming accuracy. Error in programming the FG elements over a wide range of currents. The average error is around 1% for currents higher than 100 pA.

to a computational complexity of 120 MMAC/s. Power consumption for this computation on a 16-b TI DSP is around 30 mW (excluding power dissipation for memory access) [16]. Our analog implementation consumes 0.74 μW, resulting in a performance of 162 GOPS/mW. The area needed for this system was 0.024 mm^2 in addition to routing. However, using the silicon area as a metric is misleading since, in this case, a lot of the area is traded for achieving reconfigurability. Compared to a digital signal processor (DSP), single-instruction multiple data (SIMD) paradigm-based cellular nonlinear network (CNN) systems [16]–[19] report performances that are closer to this chip. Though these systems do not replicate biological behavior at the level of ion-channels such as our chip, their designs are nevertheless based on abstractions of neural systems. The reported performance for some of these chips is 1.56 GOPS/mW [18] and 0.08 GOPS/mW [16], significantly lesser than our chip. There are, of course, other functionalities that these chips can do better than ours. It should also be noted that the DSP performs 16-b computations, while the analog one is less accurate. These inaccuracies are described next.

B. Sources of Error

The most obvious source of error is finite resolution in setting the circuit parameters and synaptic weights. This relates to FG programming accuracy which, in our case, is limited by the resolution of the adc for measurements. Fig. 12 plots measured accuracy in programming currents of different magnitudes. The resulting accuracy is around 1% for currents higher than 100 pA. Our measurement approach creates a floating-point adc [20] that combines this accuracy with the dynamic range of currents into an effective resolution of around 9 b.

The next source of error stems from mimicking a biological phenomenon by silicon circuits. Some of the approaches we presented are based on qualitative similarities between the silicon circuit and its biological counterpart. For example, Fig. 6 depicts the mismatch between a synaptic EPSP and a biological one is around 10%, corresponding to around 3.5 b. In general, this error is difficult to analyze and depends on the desired computation.

Finally, thermal noise presents a fundamental limit to the computational accuracy. The low-current, low-capacitance designs we presented save on power in exchange for thermal noise. This is actually close to the computational paradigm employed by biology and, hence, is not necessarily a problem.

C. Scaling

To expand these silicon systems to mimic actual biology, multiple chips need to be interconnected. The modular architecture of our chip does allow tiling of several chips. In that case, however, all-to-all connectivity has to be sacrificed due to the limited number of routing lines. This is also not unlike biology where local interconnects are more dense than global connections. To allow more flexibility in interchip connections, the next generation of these chips is being designed with address-event support [21].

VIII. Conclusion

We presented a reconfigurable integrated circuit for accurately describing neural dynamics and computations. There have been several earlier implementations of silicon neural networks with a dense synaptic interconnect matrix. But all of them suffer from one or more of the following problems: fixed connectivity of the synaptic matrix [22], inability to independently control the neuron parameters since they are set globally [23], [24], and excessively simple transfer-function-based neuron models [25].

In the chip we present, both the topology of the networks as well as the parameters of the individual blocks can be modified using floating-gate transistors. Neuron models of complexity varying from integrate and fire to Hodgkin–Huxley can be implemented. Computational area efficiency is considerably improved by implementing synaptic weight on the analog switch matrix resulting in all-to-all connectivity of neurons. We demonstrate dynamics of integrate and fire neurons, Hopf neurons of the Hodgkin-Huxley type, inhibitory and excitatory synapses, dendritic cables, and central pattern generators. This chip will provide users with a platform to simulate different neural systems and use the same implementation to interface with live neurons in a dynamic-clamp-like setup. The modularity of the architecture also allows tiling chips to make even larger systems. We plan to study active dendrites and their similarity with classifiers [10], oscillatory associative memory, and detailed cortical cell behavior in the future.

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Arindam Basu (M'10) received the B.Tech and M.Tech degrees in electronics and electrical communication engineering from the Indian Institute of Technology, Kharagpur, in 2005, and received the M.S. degree in mathematics and the Ph.D. degree in electrical engineering from the Georgia Institute of Technology, Atlanta, in 2009 and 2010, respectively.

He is an Assistant Professor in the School of Electrical and Electronics Engineering, Nanyang Technological University, Singapore. His research interests include nonlinear dynamics and chaos, modeling neural dynamics, low-power analog integrated-circuit design, and programmable circuits and devices.

Dr. Basu received the JBNSTS award in 2000 and the Prime Minister of India Gold Medal in 2005 from the Indian Institute of Technology Kharagpur. He received the best student paper award at the Ultrasonics Symposium in 2006, best live demonstration at ISCAS 2010, and a finalist position in the best student paper contest at ISCAS 2008.

Shubha Ramakrishnan (GSM'08) received the B.E. degree in electronics from the Birla Institute of Technology and Science, Pilani, India, in 2002, the M.S. degree in electrical engineering from Oregon State University in 2004, and is currently pursuing the Ph.D. degree in electrical engineering at the Georgia Institute of Technology, Atlanta.

Her interests include low-power analog design, bioinspired circuit design, and modeling biological learning processes in silicon.

Csaba Petre (GSM'07) received the B.S. degree in electrical engineering from the University of California, Los Angeles, in 2007, and is currently pursuing the Ph.D. degree in electrical engineering at the Georgia Institute of Technology, Atlanta.

His research interests include modeling neural systems in silicon and applications to machine learning.

Scott Koziol (GSM'06) received the B.S.E.E. degree in electrical engineering from Cedarville University, Cedarville, OH, in 1998, the M.S. degree in electrical engineering from Iowa State University, Ames, in 2000, and is currently pursuing the Ph.D. degree in robotics at the Georgia Institute of Technology, Atlanta.

His research interests include applying low-power analog signal processing to robotics.

Stephen Brink received the B.S.E. degree in bioengineering from Arizona State University, Tempe, in 2005, and is currently pursuing the Ph.D. degree in bioengineering at the Georgia Institue of Technology, Atlanta.

He is studying algorithms for signal processing that are inspired by neural systems.

Paul E. Hasler (SM'04) is an Associate Professor in the School of Electrical and Computer Engineering at the Georgia Institute of Technology, Atlanta.

Dr. Hasler received the National Science Foundation CAREER Award in 2001 and the ONR YIP award in 2002. He received the Paul Raphorst Best Paper Award from the IEEE Electron Devices Society in 1997, CICC Best Student Paper Award in 2006, ISCAS Best Sensors Paper award in 2005, and a Best paper award at SCI in 2001.