

# Programmable $G_m$ - $C$ Filters Using Floating-Gate Operational Transconductance Amplifiers

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**Abstract**—We present programmable, fully differential  $G_m$ - $C$  second-order sections (SOS) showing tunability over a wide range of frequencies. The SOSs use floating-gate operational transconductance amplifiers (FG-OTAs) to realize tunability. We present two FG programmable OTAs. The OTAs have a pFET input stage and employ current mirror topology. An FG common-mode feedback (CMFB) circuit as well as a conventional CMFB circuit is described for use with these OTAs. Their performance is compared. Expressions are derived for the differential and common-mode frequency response of the OTAs. Typical simulation and experimental results are shown for prototypes fabricated in a  $0.5\text{-}\mu\text{m}$  CMOS process available through MOSIS. The prototypes operate from a single 3.3-V supply with typical bias currents in the 10–100-nA range. We present experimental results showing frequency- and  $Q$ -tuning for a low-pass SOS (LPSOS) and a bandpass SOS (BPSOS) designed using these FG-OTAs also fabricated in a  $0.5\text{-}\mu\text{m}$  CMOS process. Measured 1-dB compression for LPSOS and BPSOS are  $-15$  and  $-11$  dBm, respectively.

**Index Terms**—Electron tunneling, floating-gate operational transconductance amplifier (FG-OTA), common-mode feedback (CMFB), FG, FG MOS, hot-electron injection, quality factor ( $Q$ ).

## I. MOTIVATION FOR LOW-POWER TUNABLE FILTERS

WE PRESENT continuous-time  $G_m$ - $C$  filters using our fully differential, programmable floating-gate operational transconductance amplifier (FG-OTA). Fig. 1 shows the topologies of two programmable FG biquads that we demonstrated experimentally (and agreed well with simulation); a low-pass second-order section (LPSOS) and a bandpass SOS (BPSOS). We demonstrate a programmable approach to using single-input FG transistors in programmable OTA blocks and OTA- $C$  filters that can be applied towards high-order (order  $> 2$ ) filters.

Fig. 1 shows how we use fully differential FG-OTAs as our  $G_m$  elements. Programmable FG MOS transistors can reduce the input offset from a  $G_m$  element, can improve the input linearity for a  $G_m$  element, and will allow wide-range, on-chip tunability after fabrication [1], [2]. These new advantages of programmable  $G_m$  elements make the use of continuous-time

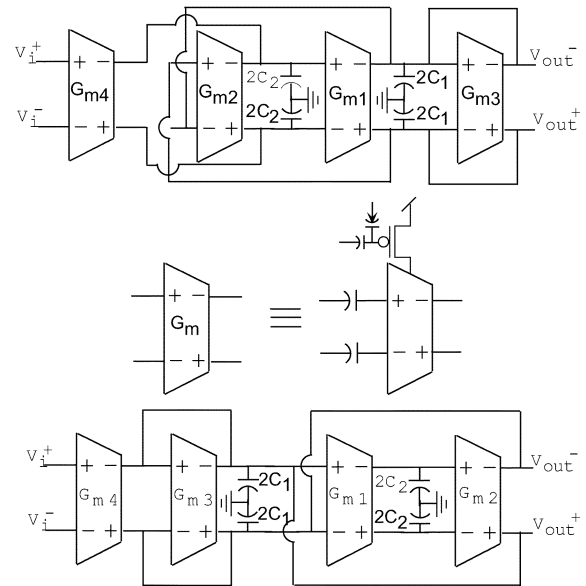


Fig. 1. Programmable, fully differential  $G_m$ - $C$  SOSs. Block diagram of a standard  $G_m$ - $C$  low-pass biquad and a bandpass biquad. Each  $G_m$  block is implemented using an FG-OTA.

$G_m$ - $C$  filters practical even at frequencies where switched-capacitor filters are currently seen as a preferred choice. Very early work on FG devices looked at the potential of this technique towards amplifier circuits using differential amplifiers [1]–[7]. Early work in multiple-input FG (MIFG) transistors showed the improved linearity in an OTA [7], [8], and techniques in pseudo-floating gate circuit techniques have been explored [9], but it fails to fully exploit the benefits of FGs especially the ability to program them [10]–[12].

In this paper, we expand and clarify upon the concept of programmable FG-OTAs that we introduced briefly [13], [14], as well as building SOSs using these amplifiers. Traditional approaches to realize programmable OTAs include digital and master-slave tuning [15]–[17]. Many of the techniques lead to storing the input-referred offset voltage due to these effects on a capacitor and then subtract it out in the normal operation. These techniques, although effective, require extra circuitry or switches and require the process to be repeated to refresh the charge on the capacitors. Digital schemes used in filters are complex and consume silicon real estate.

This paper presents programmable  $G_m$ - $C$  filters using FG amplifiers, as well as discusses design issues related to the use of FG circuit techniques for integrated filter applications. First,

Manuscript received July 8, 2005; revised October 17, 2005 and May 11, 2006. This paper was recommended by Associate Editor G. Cauwenberghs.

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Digital Object Identifier 10.1109/TCSI.2006.887473

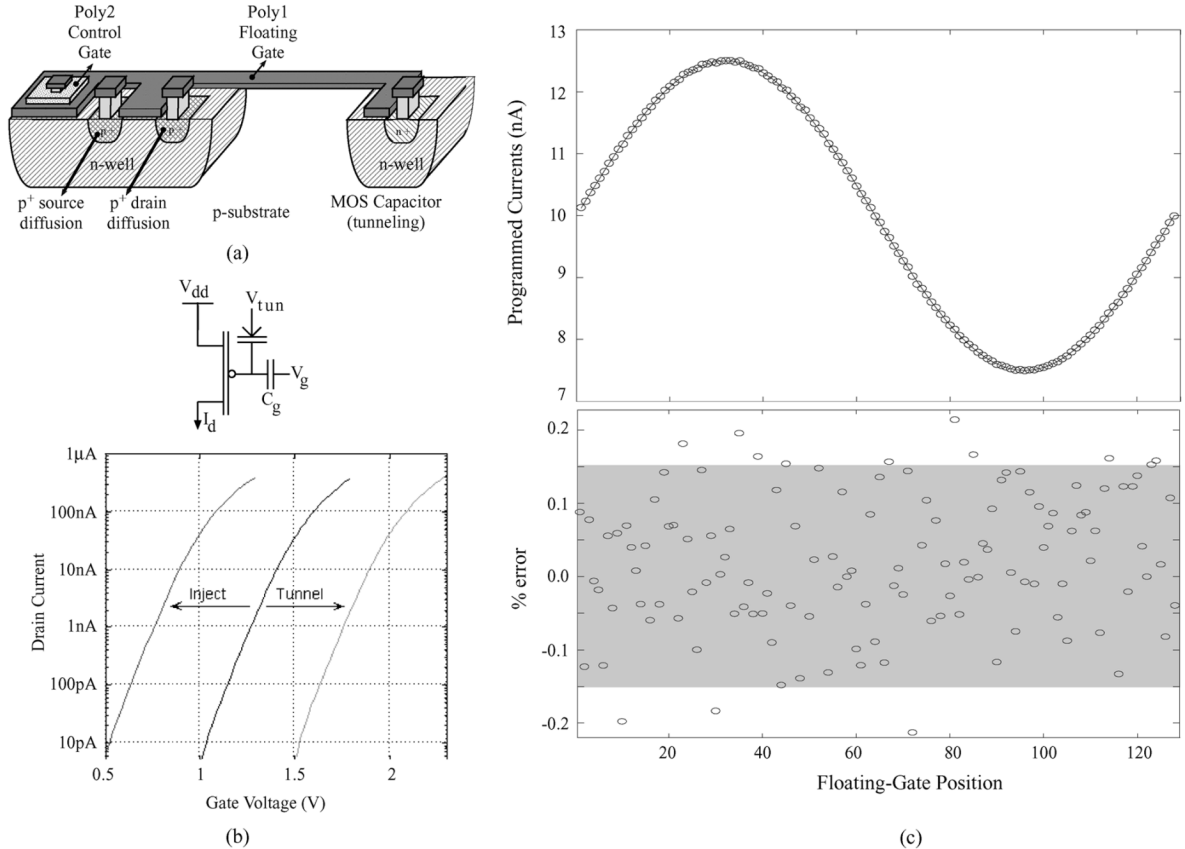


Fig. 2. Programmable FG transistor. (a) Cross section of an FG transistor. The device is a combination of a first-level polysilicon layer, combined with a standard pFET transistor in an n-well process, a MOS capacitor for electron tunneling, and capacitors coupling into the first-level polysilicon layer, known as the FG. (b) Circuit-level diagram and charge modification for the FG transistor. The FG transistor is programmed to a higher current (by decreasing the FG charge) using hot-electron injection, and is programmed to a lower current (by increasing the FG charge) using electron tunneling. (c) A sine wave with 5-nA variation and a dc of 10 nA was programmed onto 128 floating-gate elements with a percentage error bounded between  $-0.2\%$  and  $0.2\%$  error. If we change the dc bias current between  $1 \mu\text{A}$  and  $100 \text{ pA}$  with a similar percentage change for the sine wave, we get a similar percentage error due to programming.

we will discuss various applications of using FGMOS transistors in analog circuits such as offset removal, current matching and programmable current source. Second, we present the design, implementation, and experimental results of the programmable FG-OTAs that are used to design the second-order biquads. Next, we describe basic transfer functions for LPSOS and BPSOS, and we analyze how frequency and  $Q$ -peak of the two SOSs can be tuned by programming the transconductance of the OTA. Finally, experimental results for the SOSs are presented.

## II. BASICS OF FGMOS AND PROGRAMMING

A lot of work has been already published on FGMOS devices and their applications [3]–[14], [18]–[25]. For completeness, we will briefly discuss the FGMOS and accurate programming of such a device. Fig. 2(a) shows the layout cross section of our FG PMOS. An FG device is a MOS gate surrounded by silicon-dioxide with no dc path to ground and hence, the name FG. Charge on the FG node is stored permanently, providing a long-term memory, because it is completely surrounded by a high-quality insulator. The FG voltage, determined by the charge stored on the floating gate, can modulate a channel between a source and drain, and therefore, can be used in computation. Fig. 2(b) shows a circuit element description for the FG

transistor. The FG voltage ( $V_{fg}$ ) is determined from the input gate voltage ( $V_g$ ) through a capacitive-voltage divider described as

$$V_{fg} = \frac{C_g}{C_T} V_g + V_{\text{offset}} \quad (1)$$

where  $C_g$  is the capacitance between the gate terminal and the FG terminal,  $C_T$  is the total capacitance at the FG node, and  $V_{\text{offset}}$  is the voltage offset ( $Q/C_T$ ) resulting from the total charge ( $Q$ ) stored at the FG node. For a transistor operating in saturation with subthreshold currents (the well terminal connected to  $V_{dd}$ ), we get

$$\begin{aligned} I &= I_o e^{(\kappa(V_{dd}-V_{fg})-(V_{dd}-V_s))/U_T} \\ I &= I_{\text{bias}} e^{(-\kappa_{\text{eff}}\Delta V_g)-\Delta V_s/U_T} \end{aligned} \quad (2)$$

where  $I_o$  is the saturation current,  $U_T$  is the thermal voltage,  $\kappa$  is the effective capacitive divider from the gate input to surface potential,  $I_{\text{bias}}$  is the resulting bias current set through the charge on the FG voltage and bias value for  $V_s$ ,  $\kappa_{\text{eff}} = \kappa(C_g/C_T)$ ,  $\Delta V_g$  is the change in the gate voltage from its bias value, and  $\Delta V_s$  is the change in the source voltage from its bias value. A similar formulation can be given for above-threshold currents.

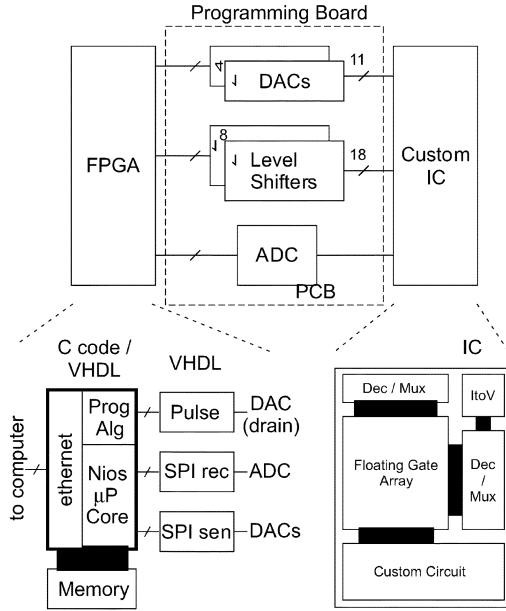


Fig. 3. System block diagram of our programming interface for these FG elements. We show a high-level block diagram using an FPGA providing fast digital control to a custom PC board, which we call our programming board, that connects to the IC we are testing. The PC board supplies the needed analog and digital voltages to the chip, as well as capability for reading analog voltages. The FG custom IC needs to reconfigure its FGs into an array when put in programming mode and have the required circuitry to select the desired column and row of the element to be programmed.

We modify the charge on a floating-gate device using hot-electron injection and/or electron tunneling, mechanisms that naturally occur in a standard CMOS process. Our programming scheme is based on using hot-electron injection for precision programming, and electron tunneling for erasing blocks of FG devices[10]–[12]. Fig. 2(b) shows the FG transistor is programmed to a higher current (by decreasing the FG charge) using hot-electron injection, and is programmed to a lower current (by increasing the FG charge) using electron tunneling.

For the circuits discussed in this paper, we programmed these devices using our second generation programming boards [21], which utilizes a field-programmable gate array (FPGA) board for the digital control of the FG device programming. Fig. 3 shows the system block diagram of our programming interface for these FG elements. Using on-board digital-analog converters (DACs), analog-digital converters (ADCs), and level shifters, we directly control using the FPGA 7 bias voltages (0–3.3 V), 4 programming voltage (0–8 V), 18 level-shifted digital signals, and one analog voltage measurement (0–5 V). The FPGA on the programming board is an Altera Stratix EP1S10 device on a board using 10/100 Mbit Ethernet interface. The FPGA is configured to implement a customized softcore processor (Altera 32 bit Nios processor) along with specialized VHDL modules that handle timing-critical communication between the programming board and the softcore processor. On the PC side, a Matlab interface has been developed that provides a direct link to the FPGA from the Matlab command line. All of the relevant circuitry could be directly

and compactly implemented on an IC, but is beyond the scope of this discussion.

The FG custom integrated circuit (IC) needs to reconfigure its FGs into an array when put in programming mode and have the required circuitry to select the desired column and row of the element to be programmed. For the IC described in this paper, we have less than 50 FG devices to program, therefore the resulting control devices are very small. This programming technique can be used to program the FG devices once when the chip is initially tested, as well as multiple times while the chip is in the field. In the second case, one must be able to apply the desired programming voltages to the chip or use on-chip charge-pump circuits [12].

Fig. 2(c) shows a measurement of a programmed  $5\text{nA}_{pp}$  sine-wave riding on a  $10\text{-nA}$  dc current for a 128 FG element row. The algorithm computes a drain voltage step based on the measured device current and the desired target current. The change due to an injection pulse depends exponentially on the resulting drain voltage, resulting in a wide dynamic range of FG charge movement to reach a target at a desired accuracy. The drain pulse is adjusted automatically as the device current approaches the target current. We obtained a worst case programming error of 0.2% and it takes about 10 pulses of 100  $\mu\text{s}$  to programmed each FG.

### III. PROGRAMMABLE FG DIFFERENTIAL TRANSISTOR PAIRS

Fig. 4 shows the circuits and data from programmable differential transistor pairs. Fig. 4(a) shows a differential transistor pair built using FG transistors. This approach can both eliminate the threshold voltage/flatband voltage differences between the two differential-pair devices, set a desired offset, and directly widen the linear input range of the differential amplifier, approaches not as easily available by other analog circuit techniques. More specifically, transistors M1 and M2 can be made equal practically with exactly as much nonlinearity as desired. Solving the capacitor-divider before getting to the FG nodes, the differential current is set by

$$I = I_{\text{bias}} \tanh \left( \kappa \frac{C_1}{C_T} \frac{V_{\text{in1}} - V_{\text{in2}} + V_{\text{offset}}}{2U_T} \right) \quad (3)$$

where  $V_{\text{offset}}$  includes  $V_T$  mismatch and charge programmed on the FG devices. If we have a mismatch between the two  $C_1$  capacitors, such that the difference between the two capacitors as  $\Delta C$ , then the resulting current-voltage relationship is

$$I = I_{\text{bias}} \tanh \left( \kappa \frac{C_1}{C_T} \frac{V_d + \frac{\Delta C}{C_1} V_c + V_{\text{offset}}}{U_T} \right) \quad (4)$$

where we define  $V_d = (V_{\text{in1}} - V_{\text{in2}})$ ,  $V_c = (V_{\text{in1}} + V_{\text{in2}})/2$ , and redefine the resulting offset accordingly. Assuming a 1 percent mismatch, the resulting common-mode rejection ratio (CMRR) of this differential pair is  $-40$  dB. Since FG transistors provide nonvolatile memory, the resulting programmed offset needs to be corrected for only once after fabrication. Fig. 4(b) shows a schematic of an FG differential pair with the necessary switches to fold this circuit into our standard programming structure. In

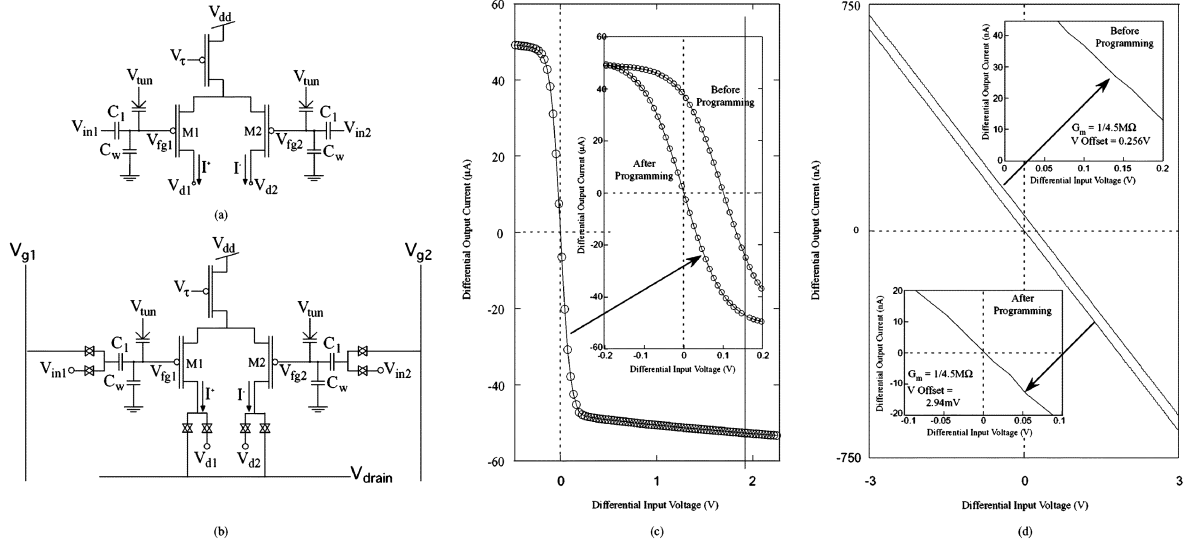


Fig. 4. Programmable FG differential transistor pairs. (a) Circuit schematic for the programmable FG differential pair. The charge stored on the FG nodes can be modified to correct for any input-referred offset. (b) Schematic of an FG differential pair with the necessary switches to fold this circuit into our standard programming structure. In program (*prog*) mode, all FG transistors must be connected to the rest of the FG transistors in a two-dimensional array. (c) Characterization of offset correction by programming of an FG differential pair with high  $\kappa_{eff}$  ( $= 0.55$ ). The larger figure shows the differential output current versus the differential input voltage. The inset shows the close up viewpoint of the FG differential pair before and after programming. The only change in the curve is a change in the offset voltage. Due to the FG capacitive divider at the inputs, we see a linear-input range of 200 mV. (d) Characterization of offset correction by programming of an FG differential pair with a very small  $\kappa_{eff}$  ( $= 0.005$ ). The larger figure shows the differential output current versus the differential input voltage, before and after programming. We achieve this large linear range ( $> 26$  V) by making  $C_T$  large relative to the input capacitor; this transistor is operating with subthreshold currents. The two insets magnify the curves before and after programming. The effective transconductance ( $G_m$ ) has no noticeable change, where the input referred offset decreases from 256 to 2.94 mV.

program (*prog*) mode, all FG transistors must be connected to the rest of the FG transistors in a two-dimensional array, as was initially specified in [22] and [23]. We can meet this requirement in multiple ways, depending upon the number of amplifiers and other FG devices to program, as well as choosing direct programming techniques (as in this paper) or indirect techniques (as in [24]). Significant amount of creativity is left to the IC designer to meet their desired specifications.

The programming circuitry for the circuits in this paper consists of T-gates at the gate and drains of each transistor in the differential pair controlling the operation of the transistor in either *prog* mode or *run* mode. Gates in a column are tied together, as are the two respective drains tied to their respective drain lines for each row. In *run* mode, the two-FG devices act as a differential pair, and hooked up to the rest of the system. This approach enables programming of each individual transistor in the differential pair. Procedure for correcting mismatch between two devices consists of programming the two devices to have same drain currents for identical node voltages.

In this paper, we limit our discussions to pFET differential pairs that allows for direct programming techniques, as described above. We can use indirect programming techniques [24] for programming either nFET or pFET FG devices, requiring additional programming complexity. This technique has the advantage of fewer switches in the signal path, and therefore potentially higher circuit performance.

Fig. 4(c) and (d) shows experimental results from two programmable differential pairs, one with a large  $\kappa_{eff} = 0.55$  for the differential pair transistors, and one with a small  $\kappa_{eff} = 0.0005$  for the differential pair transistors. Fig. 4(c) shows both a wide view on the differential current versus differential input

voltage, as well as a zoomed in view of the curves before and after programming. The resulting offset was less than 1 mV. The only change in the curve is a change in the offset voltage. Due to the FG capacitive divider at the inputs, we see a linear-input range of 200 mV.  $C_1$  and  $C_w$  were drawn to be roughly equal at 40 fF. Fig. 4(d) shows both a wide view on the differential current versus differential input voltage, as well as a zoomed in view of the curves before and after programming. We achieve this large linear range ( $> 6$  V) by making  $C_T$  large relative to the input capacitor; this transistor is operating with subthreshold currents. For these measurements,  $C_w$  was roughly 3.1 pF and  $C_1$  was roughly 26 fF. The effective transconductance ( $G_m$ ) has no noticeable change, where the input referred offset decreases from 256 to 2.94 mV.

#### IV. FGMOS FOR SINGLE-ENDED OTAs

From an FG differential pair, we can proceed to build basic differential amplifiers based on multiple FG transistors, as shown in Fig. 5. The remaining element required to building an FG-OTA are current mirrors; in practice, we would cascode key devices, but do not use them here to illustrate key concepts clearly. Unfortunately, most current mirrors have significant gain errors, a problem that easily destroys all of the advantages gained by programming the differential pair. We use an FG current mirror to compensate for threshold voltage errors between current mirror transistors. Fig. 5(a) shows a schematic of a current mirror using FGs. The multiplication/gain factor of the current mirror is set by the difference in floating gate charge between the two transistors. To construct an ideal current mirror, the floating gate is programmed such that the gain is equal to 1. This condition also reduces the temperature dependence of

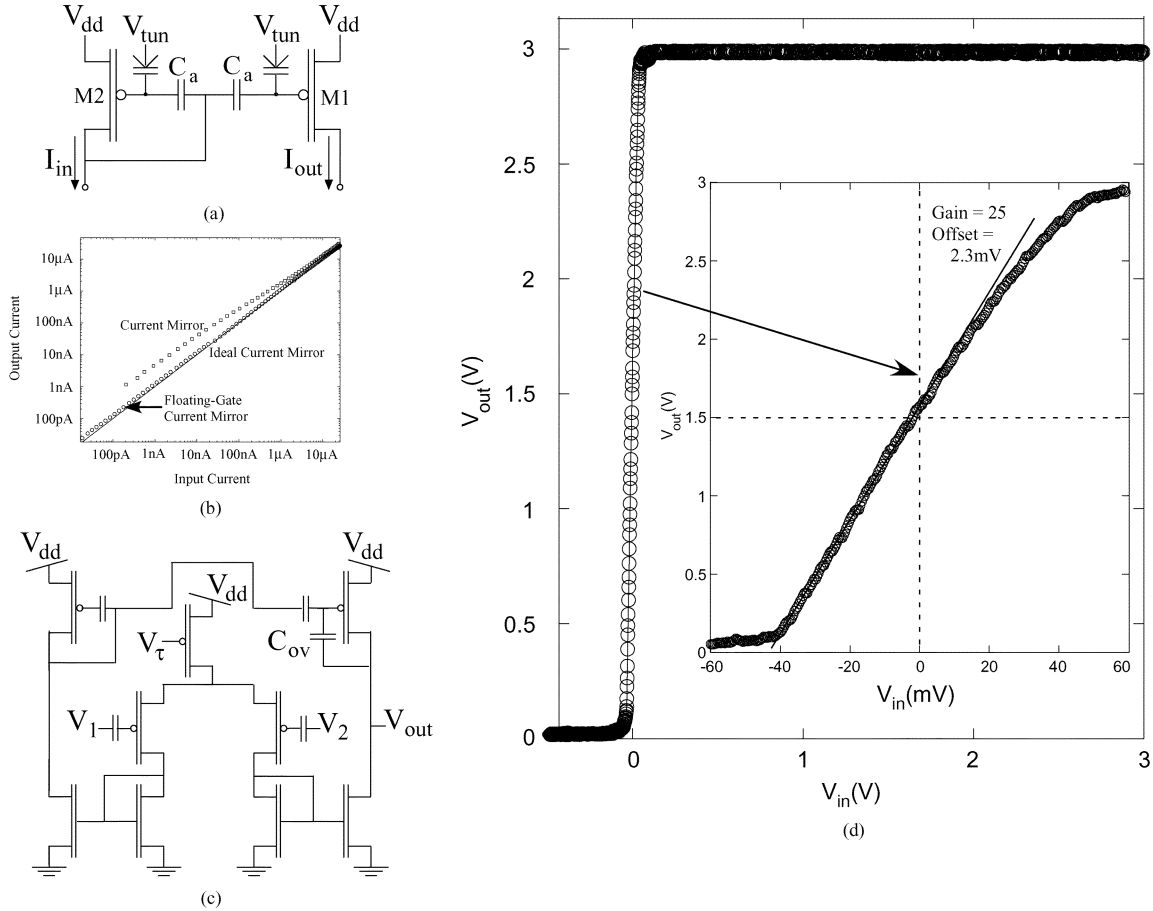


Fig. 5. (a) Schematic of the FG current mirror. The current mirror ratio is controlled by programming the FG charge. (b) Preliminary data from the current mirror structure. By programming the FGs, the current mirror has been made very close to ideal. (c) Schematic of the FG-OTA. The OTA is based on the FG differential pair and current mirror (Section V). Each FG transistor in the OTA is programmed to have the same value of effective threshold voltage. After an initial input voltage sweep, minor corrections are made to effective threshold voltage for the output pMOS transistor of the current mirror to compensate for any threshold mismatch of the nMOS current mirror pair. (d) Experimental results from an offset removed OTA. Voltage transfer function of the offset removed OTA. Inset: Voltage transfer function over a smaller differential input range. The  $V_{offset}$  of the amplifier is measured to be less than 5 mV. The measured offset is 2.3 mV, and the resulting gain is 25, which is limited by by the overlap capacitance on the output FG transistor.

the current mirror. Fig. 5(b) shows the result of a measurement after the currents have been programmed to identical. Since FG transistors can be programmed to any bias current value for a given reference voltage, they can be easily used to generate programmable accurate bias currents.

Fig. 5(c) shows the schematic of the single-ended FG-OTA, based on the FG differential pair and current mirror. The circuit has three sources of mismatch errors: the FG input differential pair, the FG pMOS current mirror, and two nMOS current mirrors. Each FG transistor in the 9-transistor OTA is programmed to be identical except to compensate for threshold voltage mismatches. The bias current is programmed using another FG element. The programmable pMOS current mirror compensates for threshold-voltage mismatch in the pFET transistors as well as the aggregate effect of threshold-voltage mismatch in the nFET transistors. The resulting correction is independent of temperature in this configuration. The OTA is programmed through array programming architecture. We initially program the FG transistors to be equal (same target drain current for their given target gate voltages), except for the programmable transistor setting the bias current, which is programmed directly. Then, using

a dc sweep of the OTA, we optimize the circuit performance by modifying the FG charge. Most of the resulting offset from this sweep is due to errors in the nMOS current mirrors in the OTA, thus the pMOS current mirrors are programmed to compensate for the n-channel mirrors.

Fig. 5(d) shows the resulting dc voltage transfer functions for a trimmed OTA. The amplifier is operated in subthreshold for a dc bias current of 20 nA. The resulting offset for the amplifier was 2.3 mV, and could be programmed tighter given more accurate voltage measurements. The voltage gain of the amplifier was measured to be 25, resulting from the overlap capacitance ( $C_{ov}$ ) of the output pFET transistor; the gain proportional to the input capacitance over  $C_{ov}$ . Much larger gains are and have been experimentally achieved by cascoding this pFET transistor; we show these results to illustrate the key FG circuit effects.

V. FG-OTA

To build balanced-differential designs, we investigate and characterize two different types of common-mode feedback (CMFB) circuits. In both cases, FG transistors set the tail current source, set the differential input pair, and implements part

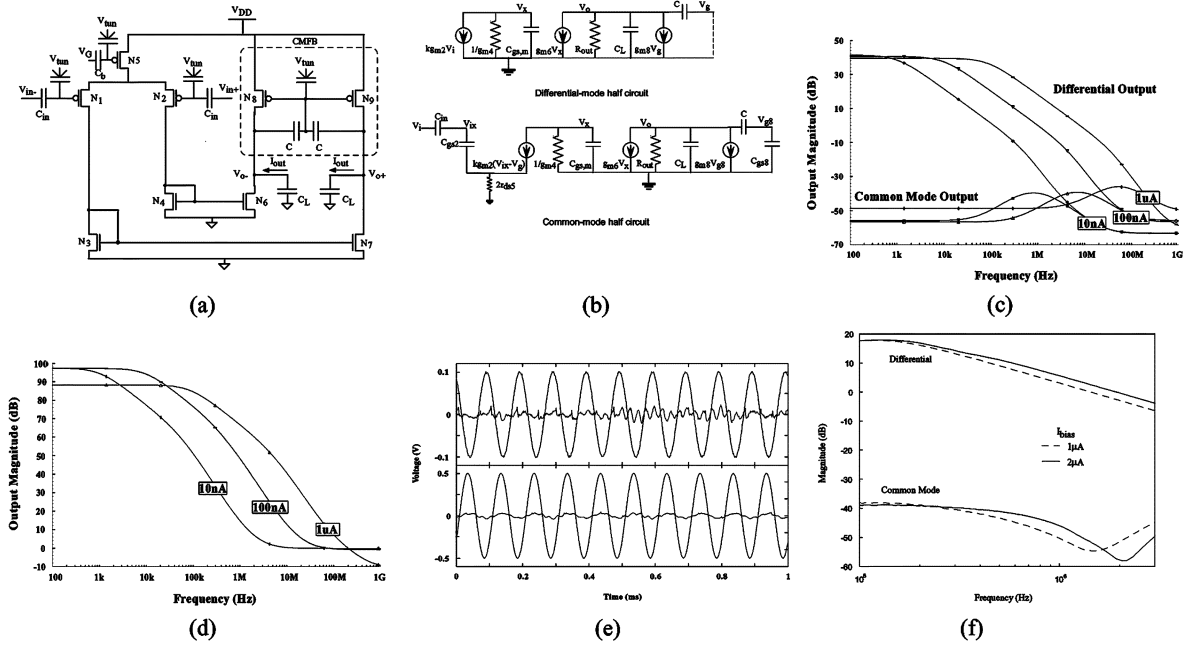


Fig. 6. Fully differential FG-OTA with FG CMFB circuit (FG-OTA1) and measurements. (a) Fully differential FG-OTA with FG CMFB circuit (FG-OTA1). (b) Small-signal circuit schematics for differential- and common-mode analysis of FG-OTA1. (c) SPICE simulation results of small signal common-mode and differential-mode response of FG-OTA1. Plot shows data for three values of OTA bias currents—10 nA, 100 nA and 1  $\mu$ A. (d) SPICE simulation results of CMRR versus frequency of FG-OTA1. (e) Transient common-mode response of FG-OTA1 circuit with FG transistors. Response is shown for 10-kHz input common-mode signal at 200 mV<sub>pp</sub> and 1 V<sub>pp</sub>. The input signal rides on a dc level (not shown) of  $V_{CM} = 1.2$  V. (f) Experimental frequency response of FG-OTA1 for two different programmed bias currents.

TABLE I  
DIFFERENTIAL-MODE AND COMMON-MODE PARAMETERS FOR FG-OTA1

Parameter	Differential Mode	Common Mode
DC gain	$g_{m2}(r_{o8}/r_{o9})$	$C_{ov}/C_{in}$
Dominant Pole	$(C_L + C)(r_{o8}/r_{o9})$	$\frac{C_L C_T}{g_{m9} C}$
Second Pole	$\frac{2(1-\kappa)C_{ox}}{g_{m2}}$	$\frac{2(1-\kappa)C_{ox}}{g_{m2}}$

of the CMFB circuit. Through programming, we set the bias currents, and the offset between the differential pair transistors.

Fig. 6 shows the circuit, simulation, and measurement for the first OTA design, which we refer as FG-OTA1. The CMFB circuit is build using two capacitors to sum the two outputs, thus computing the output common mode, and directly applying this signal as feedback to the output current sources. Fig. 6(b) shows the small signal differential-mode and common-mode half-circuits. Table I shows the calculated differential-and common-mode parameters for FG-OTA1, assuming the capacitors are matched. Mismatch in  $C$ , will result in a differential feedback, that will limit the gain, similar to the overlap capacitance for the single-ended case. Further, CMRR is degraded by the input capacitance mismatch as in the single-ended case. In this design, the sizes of the nFET transistors were identical, and the sizes of the pFET transistors were identical. Fig. 6 shows we get reasonable dc gain (40 dB) and CMRR (95 dB) from this noncascoded amplifier through simulation with no mismatch. The  $-3$ -dB frequency is directly related to the bias current; an order of magnitude increase (decrease) in the bias current, corresponds to an analogous increase(decrease) in the corner frequency. Unfortunately, mismatch between N8 and N9 will significantly reduce the differential gain, as seen experimentally in Fig. 6; the re-

sulting gain shows that the mismatch between M8 and M9 is roughly 20%.

Fig. 7 shows the circuit, simulation, and measurement for the second OTA design, which we refer as FG-OTA2. FG-OTA2 has the advantage of a higher CMFB loop gain, better current mirror matching, higher output impedance with output cascoding and higher differential open-loop gain. Fig. 7(a) shows the circuit schematic. Output FG transistors,  $M_{12}$  and  $M_{13}$ , help correct any mismatch in the output current-source transistors, thereby aiding CMFB circuit in improving the CMRR. The output stage of the FG-OTA was cascoded to give a high output resistance, which decreases the dominant pole of the OTA- $C$  block, giving it a more ideal integrator behavior over a wider frequency range.

Fig. 8 shows the CMFB circuit for the differential FG-OTA. The bias current and, hence, the corner frequency of the OTA is determined by the current flowing through the FG transistor  $M_{16}$ . Thus, the  $G_m$  of the OTA can be adjusted by programming  $M_{16}$ . The output of this circuit is  $V_{bias}$ , which was the same  $V_{bias}$  that set the tail current for the input differential pair. The differential and common-mode gain for the FG-OTA can be analyzed using the small-signal model and is given as

$$A_{dm,dc} = g_{m1} \frac{g_{m9} R_{out}}{g_{m3}}$$

$$A_{CM,dc} = \frac{g_{m24}}{2r_{ds5} g_{m5} g_{m20}}$$

$$CMRR = 2g_{m1} g_{m20} r_{ds5} R_{out}$$

$$R_{out} = g_{m11} r_{ds11} r_{ds9} // g_{m15} r_{ds15} r_{ds13} \quad (5)$$

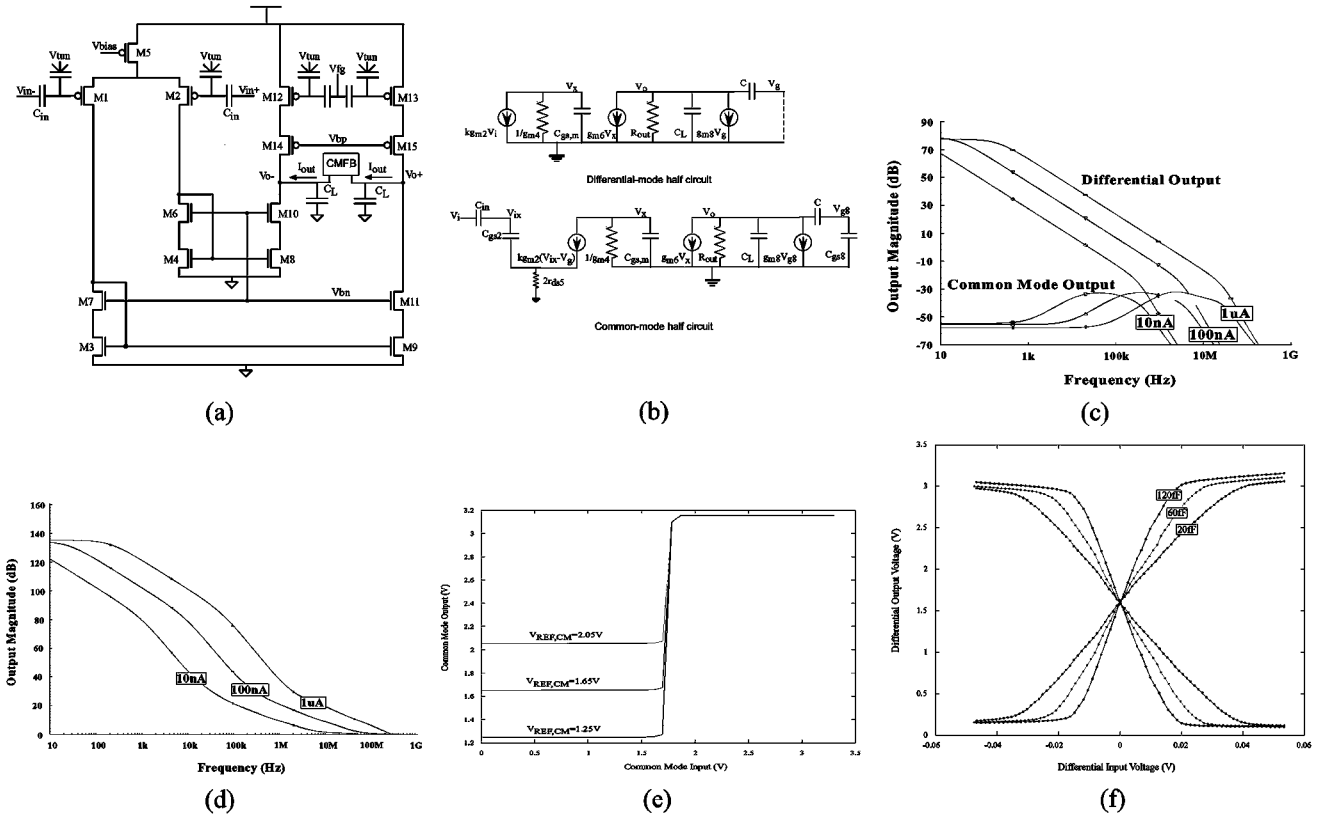


Fig. 7. Programmable FG-OTA with CMFB (FG-OTA2) and measurements. (a) Circuit schematic for the programmable FG-OTA (FG-OTA2). Inherent offsets of the amplifier are compensated by programming the FG transistors. FG transistors  $M_1$  and  $M_2$  are used to eliminate the input referred offset of the amplifier. Transistors  $M_{12}$  and  $M_{13}$  account for any error at the output. (b) Small-signal circuit schematics for differential and common-mode analysis of FG-OTA2. (c) SPICE simulation results of small signal common-mode and differential-mode response of FG-OTA2. Plot shows data for three values of OTA bias currents—10 nA, 100 nA and 1  $\mu$ A. (d) SPICE simulation results of CMRR versus frequency of FG-OTA2. (e) Plot shows output common-mode voltage for FG-OTA2 as the reference voltage to the CMFB circuit is varied. The input voltage where the common-mode output goes to  $V_{dd}$  can be changed by programming the FG current-source charge. (f) dc differential input sweep for the FG-OTA2 circuit with varying  $C_{in}$  values—20 fF, 60 fF and 120 fF. Measured dc gains are 40.01 V/V, 60.77 V/V and 95.75 V/V, respectively. The gain is a function of the capacitance  $C_{in}$  connecting the differential input to the FG node.

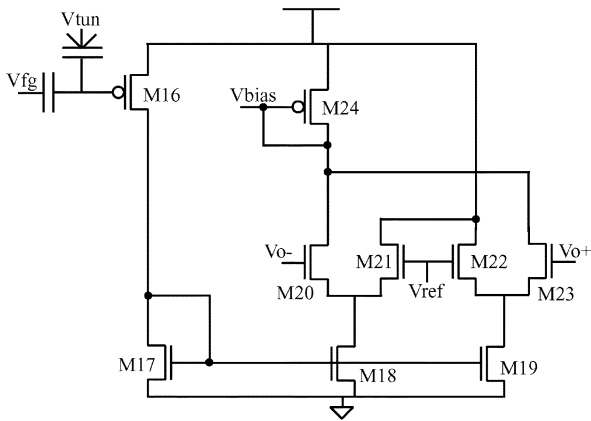


Fig. 8. CMFB for FG-OTA2: CMFB circuit with FG current source to program the corner frequency as desired. Transistor  $M_{16}$  sets the bias current for the FG-OTA; therefore the  $G_m$  of this amplifier can be adjusted by programming  $M_{16}$ .

where we define  $a//b = 1/(a^{-1} + b^{-1})$ . Simulation and experimental results agree closely to these theoretical expressions. It is seen that for the OTAs the input common-mode range is restricted to less than 1.7 V. This limitation is caused by bias transistor operating out of saturation region due to voltage headroom

issues. We will use FG-OTA2 for the as the OTA- $C$  for the following section.

Both circuits use the programmable current sources and FG differential pair elements. CMRR is limited by the input capacitance mismatch as in the single-ended case. The first approach uses a simple but elegant CMFB system that uses capacitors to linearly compute the output common-mode voltage and feedback this signal to set the output common-mode voltage. This technique, as currently used, is directly affected by mismatch of the two CMFB capacitors, and the resulting mismatch acts as a feedback on the differential mode signal, reducing the differential mode gain of the amplifier. The second approach uses two FG current sources to program the output stage, which could be programmed to eliminate other offsets in the programming path, sufficiently so to potentially eliminate the need for any CMFB circuit. For robust circuit implementation, we still implemented a CMFB element, and a typical CMFB circuit was chosen, which computes a nonlinear function of the common mode. As a result, FG-OTA2 has the advantage of a higher CMFB loop gain, better current mirror matching, higher output impedance with output cascoding and higher differential open-loop gain. An improved version of this circuit would combine these two techniques, that is use capacitive CMFB computation (in the first case) to directly affect  $V_{bias}$  (as in the second case),

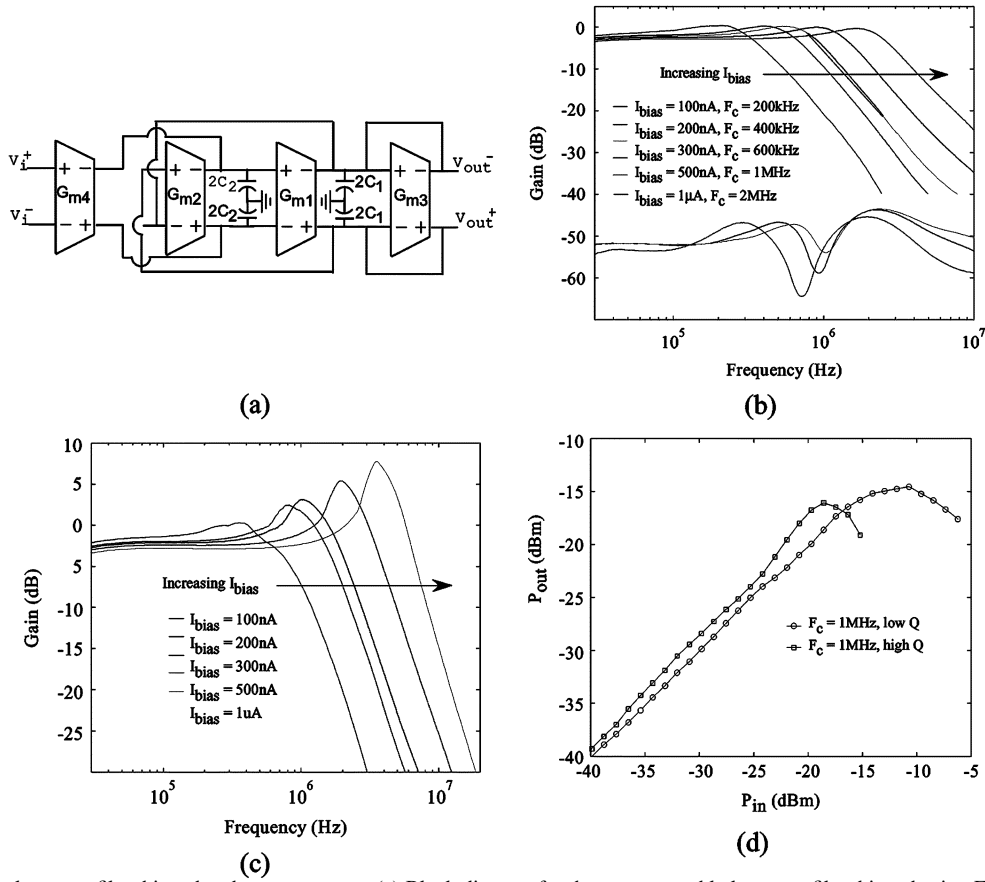


Fig. 9. Programmable low-pass filter biquad and measurements. (a) Block diagram for the programmable low-pass filter biquad using FG-OTAs. (b) Measured differential and common-mode gain for the LPF programmed to different corner frequencies (200 kHz–2 MHz). The measured common mode gain for low-pass biquad agreed with simulated values. (c) Measured differential gain for the LPF showing the  $Q$  variation for different programmed bias currents. (d) Measured plot to compute the 1-dB compression point for a LPF tuned at 1 MHz for two different programmed  $Q$  values. The currents were initially programmed to give a flat response and then current setting the lower time constant was increased using injection to make the poles complex and give a  $Q$ -peak.

where the common mode will be linearly computed, but the differential mismatch between these capacitors will not effect the amplifiers differential mode gain.

## VI. PROGRAMMABLE SOSs

We designed and fabricated both a programmable, fully differential LPSOS and an BPSOS [Fig. 9(a) and (b)] on a  $0.5\text{-}\mu\text{m}$  n-well CMOS process available through MOSIS. Any higher order filter can be realized as a cascade of biquad filters. Although there are several ways to realize higher order filters, cascade filters are the easiest to design as well as to tune. FG-OTAs are used as programmable  $G_m$  elements described earlier. Fig. 12 shows the circuit prototype fabricated in a  $0.5\text{-}\mu\text{m}$  n-well CMOS process. The total area for the BPSOS and LPSOS is  $0.135\text{ mm}^2$ . This allows filters to be programmed to desired corner frequencies and  $Q$  values. The sizes of the drawn capacitors were roughly 350 fF. For  $G_m$ - $C$  filters, the time constants are set by the ratio of  $G_m$  and the resulting capacitances. For these differential pairs, the  $G_m$  is (obtained by expanding the  $\tanh$  function)

$$G_m = \frac{C_1 \kappa I_{bias}}{C_T 2U_T}. \quad (6)$$

After fabrication, the time constant is tuned only through the bias current, which can be programmed from 100-fA range [25]

to tens of microamperes and higher, resulting in roughly eight orders of magnitude of tuning range. For an output capacitance of 100 fF, we are looking at a tuning range from 5 Hz to 500 MHz. If the input transistors are not sized properly, we may not get quite as much tuning range at the upper limit due to the devices going above threshold. Further, by drawing different size load capacitors, the range of possible frequencies can be further increased by potentially more orders of magnitude.

### A. Low-Pass SOS

Fig. 9 shows the block diagram of the low-pass biquad (LPSOS) using FG-OTAs. The transfer function of the SOS is given by

$$\frac{V_{out}}{V_{in}} = \frac{\frac{G_{m4}}{G_{m2}}}{\frac{s^2 C_1 C_2}{G_{m1} G_{m2}} + \frac{s G_{m3} C_1}{G_{m1} G_{m2}} + 1}. \quad (7)$$

Assuming  $C = C_1 = C_2$  and  $G_m = G_{m1} = G_{m2}$ , the time constant (or corner frequency) and  $Q$  for complex-conjugate poles is given by

$$\tau = \frac{C}{G_m}; \quad Q = \frac{G_m}{G_{m3}}. \quad (8)$$

A desired corner frequency can be obtained by programming the bias current that control  $G_m$ , while the  $Q$  of the filter can be independently set by adjusting  $G_{m3}$ . Programming accuracy for



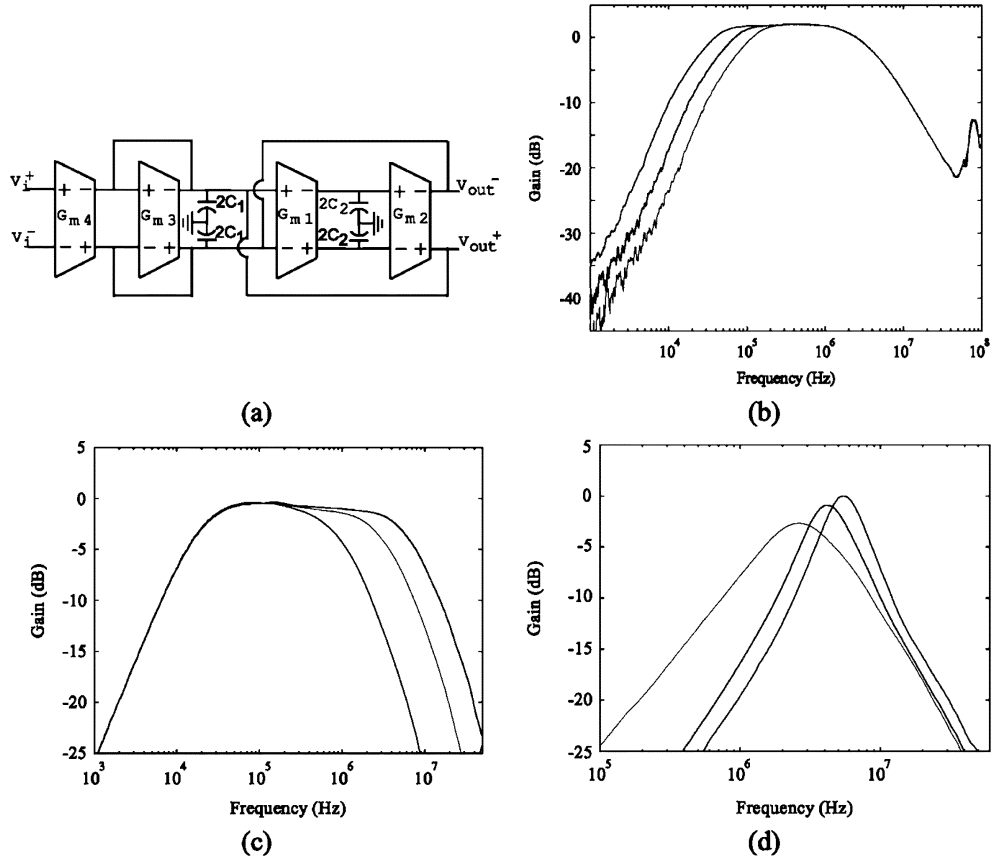


Fig. 10. Programmable bandpass filter biquad and measurements. (a) Block diagram for the programmable bandpass filter biquad using FG-OTAs. (b) Experimental results showing the programming of the low corner of the Bandpass filter. Corner frequencies were programmed at 25, 50, and 100 kHz. (c) Experimental results showing the programming of the high corner of the bandpass filter. Corner frequencies were programmed at 1, 2, and 4 MHz. (d) Experimental results showing programming of the low corner of the bandpass filter for different  $Q$  values. As the  $G_m$  is increased,  $Q$  increases and the center frequency also increases as predicted by (10).

the center frequency and the  $Q$  is related to the current programming accuracy, therefore roughly 0.1% for center frequency and 0.2% for  $Q$ . Practically, the mismatch in the capacitors, which is primarily the load capacitors, will alter the center frequency and  $Q$ , and therefore we typically take a few frequency points to precisely target absolute values. We have programmed  $Q$  values up to 10 for this implementation.

Fig. 9(b) shows measured data of the differential gain of the LPSOS for different programmed  $G_m$ 's while keeping the ratio  $G_m$  over  $G_{m3}$  constant. The corner frequencies move linearly (200 kHz–2 MHz) with the bias current as long as the input transistors operate in subthreshold, due to the fact that transconductance varies linearly with bias current in this region. Fig. 9(b) also shows the common-mode gain for these structures for different bias currents suggesting a good CMRR. The experimental results correlated well with the simulations for these plots. Fig. 9(c) shows experimental results for different programmed  $Q$  values that are adjusted by programming  $G_{m3}$ . Fig. 9(d) shows the measured output power for varying input power of the low-pass SOS when tuned to 1-MHz corner for the two different  $Q$  values. This measurement can be used to find the 1-dB compression point of the system by doing a simple curve fit. The linearity of the system deteriorates with higher  $Q$  due to higher gain in the system. The measured 1-dB

compression for the high  $Q$  and low  $Q$  case was 160 mV<sub>pp</sub> and 280 mV<sub>pp</sub>, respectively.

### B. Bandpass SOS

Fig. 10(b) shows the block diagram of a  $G_m$ - $C$  BPSOS using four FG-OTAs. The transfer function of the SOS is given by

$$\frac{V_{out}}{V_{in}} = \frac{\frac{sG_{m4}C_1}{G_{m1}G_{m2}}}{\frac{s^2C_1C_2}{G_{m1}G_{m2}} + \frac{sG_{m3}C_1}{G_{m1}G_{m2}} + 1}. \quad (9)$$

Assuming  $C = C_1 = C_2$  and  $G_m = G_{m1} = G_{m2}$ , the time constant (or corner frequency) and  $Q$  for complex conjugate poles is given by:

$$\tau = \frac{C}{G_m}; \quad Q = \frac{G_m}{G_{m3}}. \quad (10)$$

The corners and the center frequency of the BPSOS can also be set by programming the FG-OTAs.

Fig. 10(a) shows the experimental response of the BPSOS with different programmed  $G_m$ 's. The low corner changes while keeping the high corner constant ( $G_{m3}$  is kept fixed). Fig. 10(b) shows the measured response for the BPSOS, where the high corner has been moved independent of the

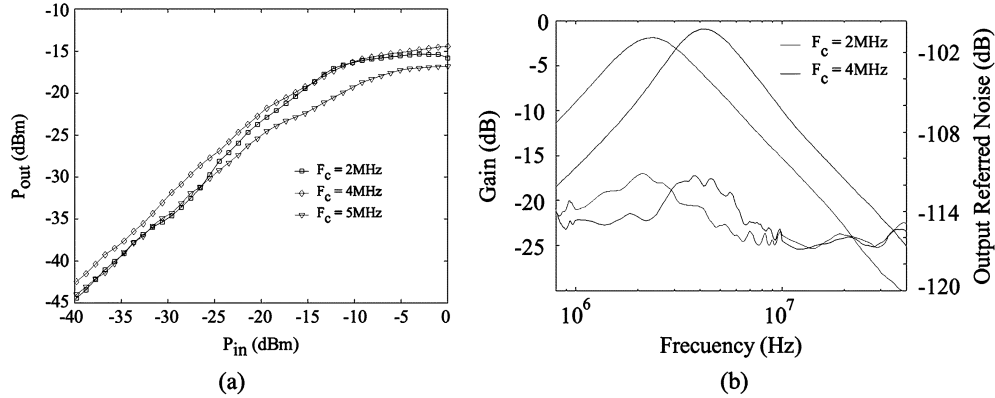


Fig. 11. BPSOS Performance. (a) 1-dB compression points for a BPF tuned at different frequencies. (b) Output referred spot noise of Bandpass filter tuned at 2 and 4 MHz. The noise obtained at these frequencies is mostly thermal.

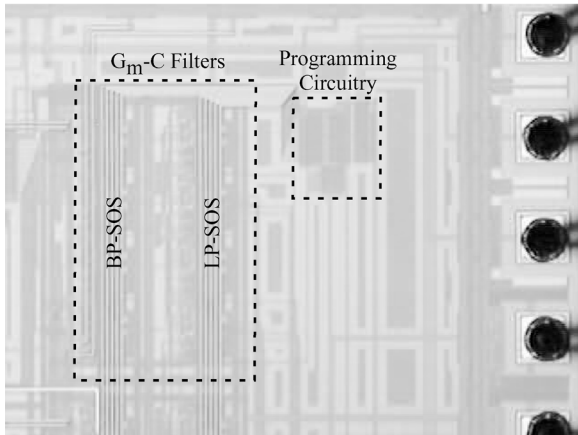


Fig. 12. Die micrograph. The circuit prototype was fabricated in a  $0.5\text{-}\mu\text{m}$  n-well CMOS process. The total area for the BPSOS and LPSOS is  $0.135\text{ mm}^2$ .

low corner frequency, accomplished by programming the bias currents controlling  $G_{m3}$ , and keeping the ratio  $G_{m3}$  over  $G_m^2$  constant. Fig. 10(c) shows the filter response for different  $Q$  values, where  $G_m$  was programmed so complex poles were obtained. The center frequency will also vary as a function of  $G_m$ . Careful programming of these FG-OTAs can give varying values of  $Q$  for different center frequencies.

The measurement used to compute 1-dB compression of the BPSOS for three different corner frequencies, with similar  $Q$  and gain, is shown in Fig. 11(a). The linearity is similar for the three different frequencies in this case by design and is about 397 mVpp (or  $-11$  dBm). Fig. 11(b) shows the output-referred noise spectrum of the programmed BPSOS with center frequencies of 2 and 4 MHz. The spectrum looks like that of the tuned filter response as expected. The noise at these frequencies is purely thermal as can be observed from the measured data. The worst-case input-referred spot noise power occurs at the center frequencies and is  $-109$  dBm.

## VII. CONCLUSION

This paper presents an approach for designing programmable  $G_m$ - $C$  filters using FG transistors. The paper presents two different programmable FG-OTAs. The designed OTAs were used

to implement programmable second order  $G_m$ - $C$  low-pass and bandpass sections. The programmability of the transconductance allows for the center frequency and  $Q$  value to be tuned to multiple values. Basic building blocks such as low-pass bi-quad and bandpass bi-quad were discussed and measured results from the same were presented. The filters can be programmed to desired corner frequencies and  $Q$  values. Detailed discussion on fast and accurate programming can be found in [12]. Based on these results, it is possible to design a fully programmable higher-order bandpass filters that can be tuned to different responses (like Butterworth, Chebyshev) at different frequencies. The filter coefficients can be set by accurately programming the FG currents.

With decreasing power-supply voltages and low-power requirements in analog and mixed-mode circuits, subthreshold operation is an obvious choice. This work demonstrated the implementation of  $G_m$ - $C$  filters with the used of programmable OTAs operating in subthreshold operation. Advantages of the FG-OTA over the conventional OTA circuit has been discussed previously in [7]. A wider linear range can be easily obtained due to the capacitive division of the FG transistor. This improvement in linear range comes as expense of the input-referred-noise with increases by the same amount [26], [27] thus the dynamic range is practically unchanged.

This offset will greatly degrade the performance of the filter. The presented architecture takes advantage of the FG transistor used for increased linearity and allows for offset cancellation by programming these input differential pair. Filter parameters such as gain,  $Q$ , and corner frequency had been shown to be  $G_m$  dependent. In [28], these parameters were tuned with voltages or independent current sources. In this work on-chip nonvolatile storage of filter parameters is achieved through the used of FG transistors in the tail current of the FG-OTAs.

Although additional IC area maybe required for the programming circuitry, this is the typical tradeoff between IC area and device matching. When precise filter parameters and high performance are required, higher matching between the IC devices is needed. Device matching shows a quadratic relationship with area, which is not the case when using FG transistor. Additionally, this technique allows for tuning the filter parameters which is not possible otherwise.

## ACKNOWLEDGMENT

The authors wish to thank E. Farquhar for fabricating some of the chips used in these measurements.

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