Switched Capacitor Circuits I

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Switched Capacitor Circuits

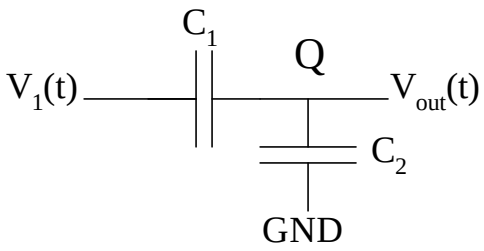
- Making a resistor using a capacitor and switches;
  therefore resistance is set by a digital clock and the capacitor.

- Filters built in this technology are set by external clocks,
  and ratio of capacitors (matching of 0.1% to 1%)

The precision of the frequency response is realized by ratios of capacitors
(1% to 0.1%…better matching, larger caps; therefore more power/area),
and a clock signal (which can be set precisely with a crystal reference)

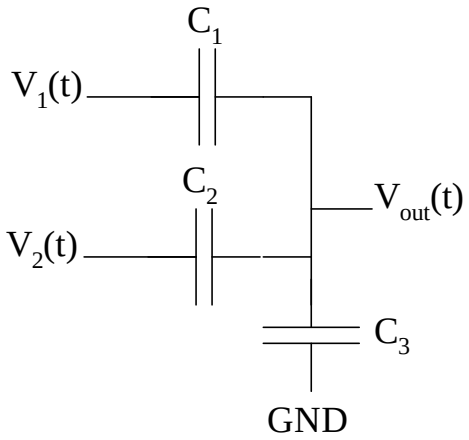
Capacitor Circuits

Capacitive Voltage Divider



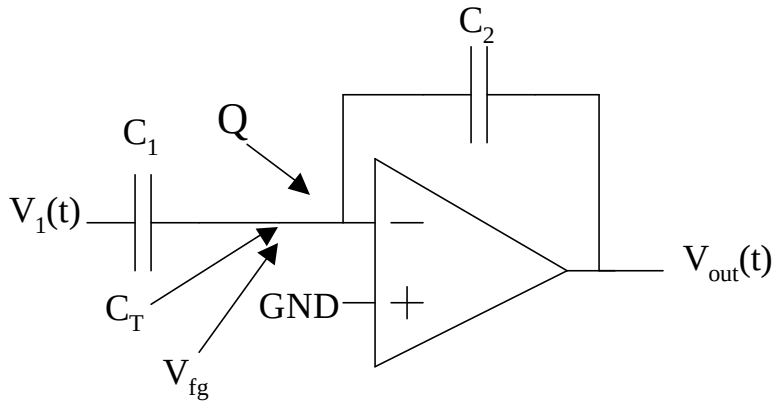
$$V_{out}(t) = \frac{C_1}{C_T} V_1(t) + \frac{Q}{C_T}$$

Multiple Input Voltage Divider

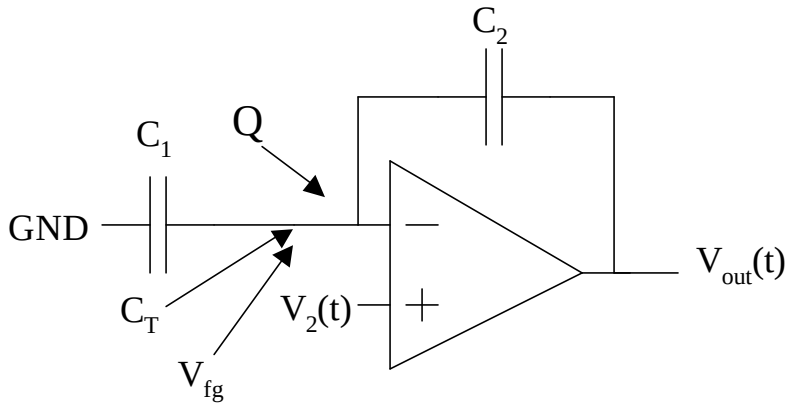


$$V_{out}(t) = \frac{C_1}{C_T} V_1(t) + \frac{C_2}{C_T} V_2(t) + \frac{Q}{C_T}$$

Capacitive Feedback



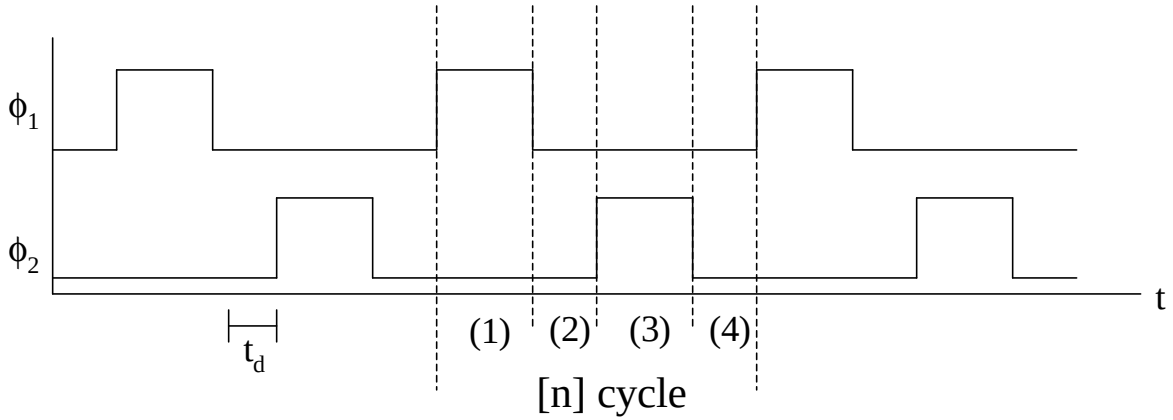
$$V_{out}(t) = -\frac{C_1}{C_2} V_1(t) - \frac{Q}{C_2}$$



$$V_{out}(t) = \left(1 + \frac{C_1}{C_2}\right) V_1(t) - \frac{Q}{C_2}$$

Non-Overlapping Clocks

We will always be using non-overlapping clocks; therefore, we want a waveform like



We effectively have four phases.

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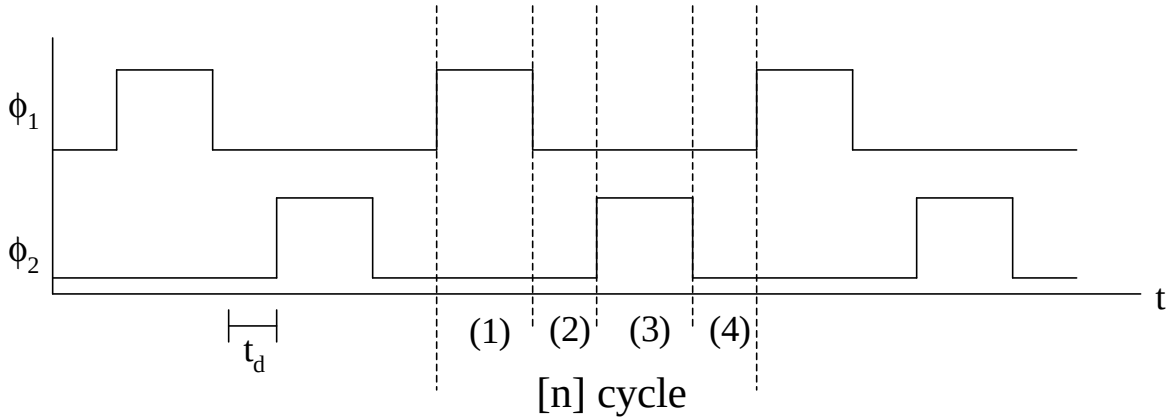

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Would want t_d as small as possible for proper operation

We will also assume that the input is held constant through the entire [n]th cycle

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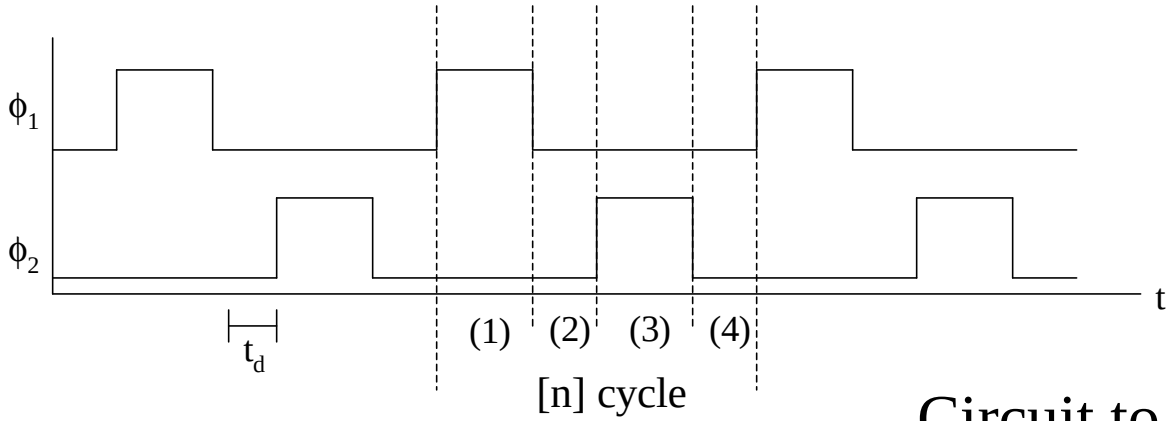

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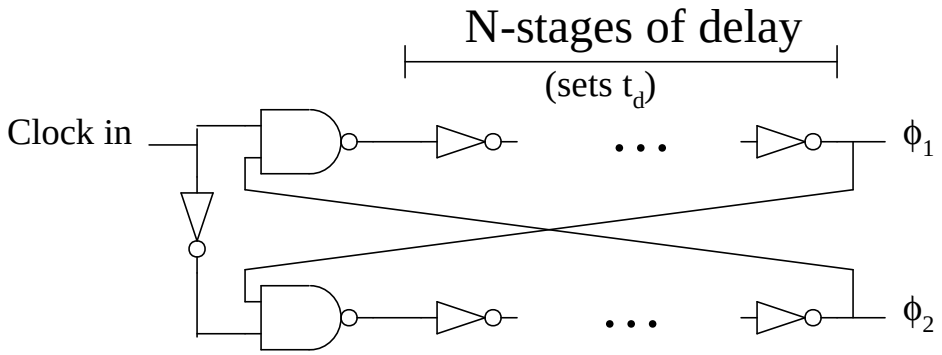
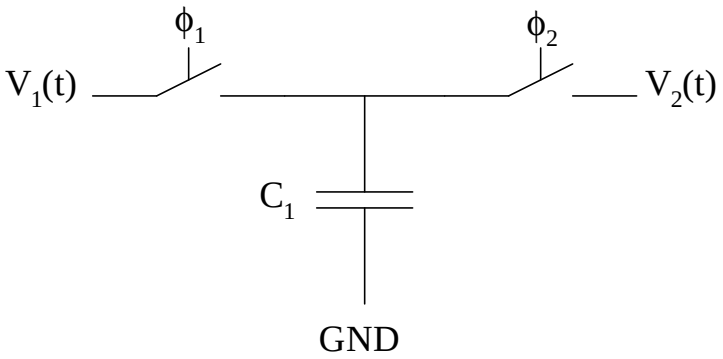
Circuit to generate waveform



Basic Switched Capacitors



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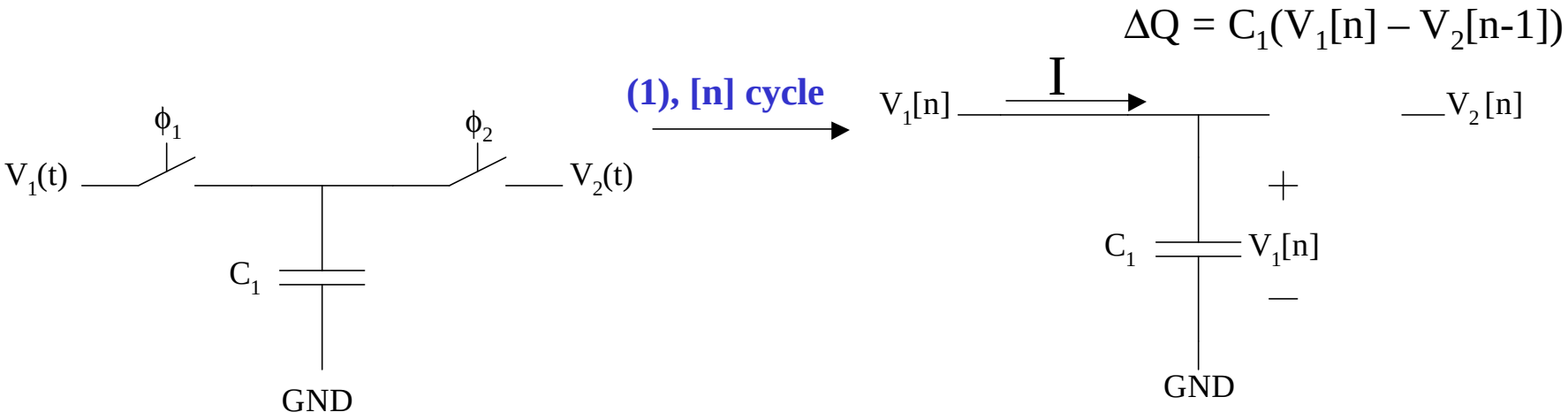

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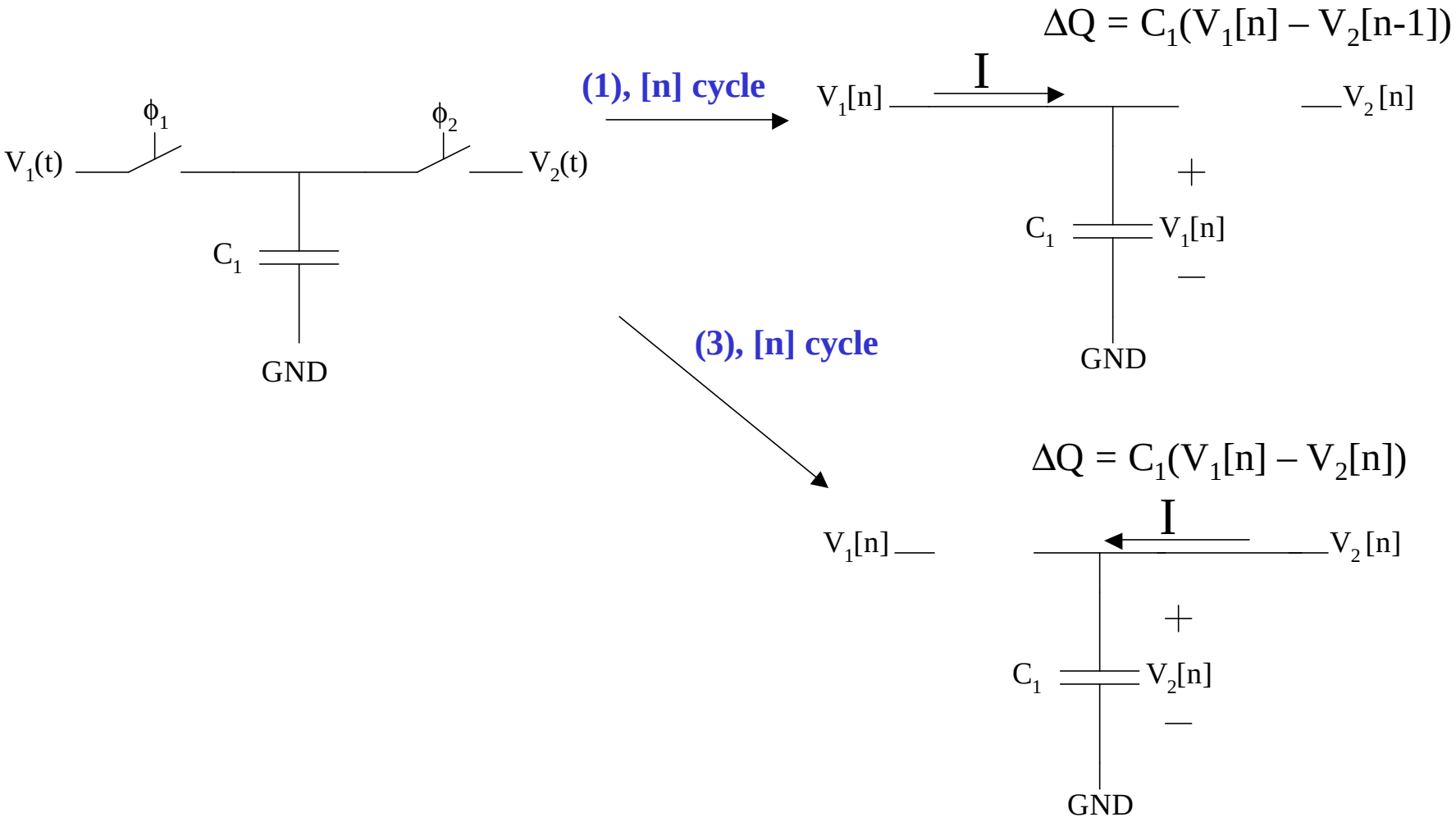

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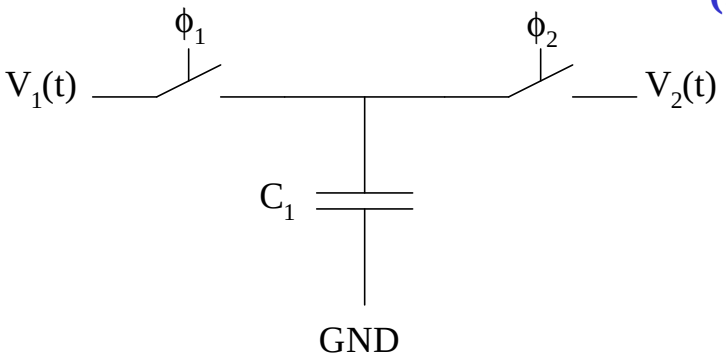
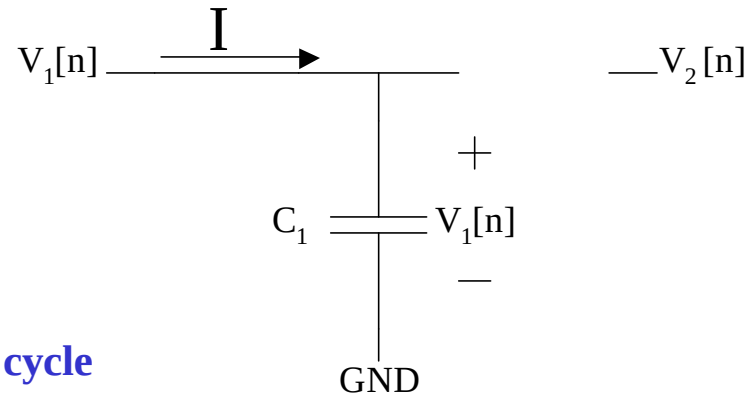


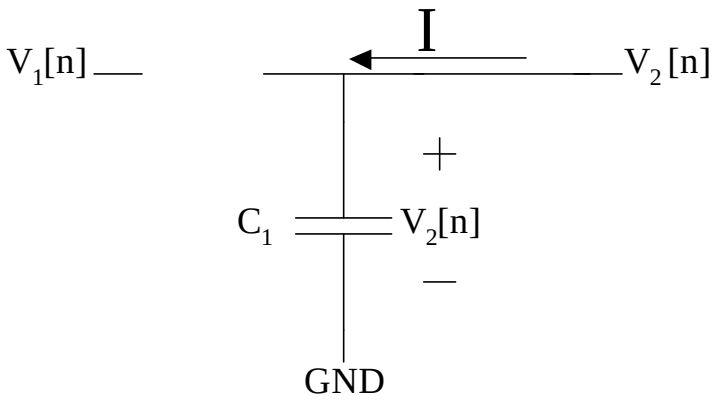
(1), [n] cycle

$\Delta Q = C_1(V_1[n] - V_2[n-1])$



(3), [n] cycle

$\Delta Q = C_1(V_1[n] - V_2[n])$

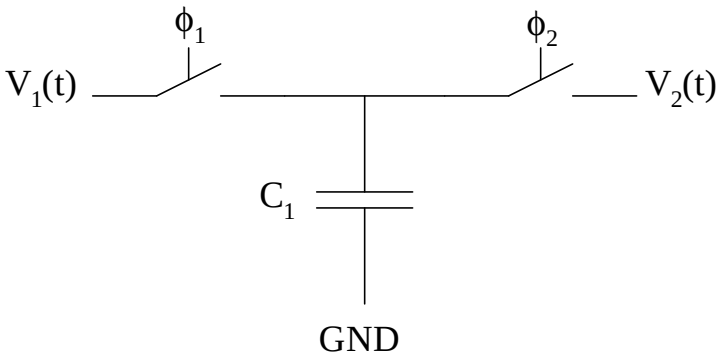


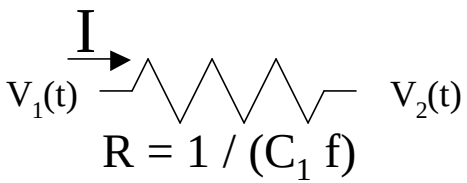
If we assume the input changes slowly ($V_2[n-1] \sim V_2[n]$; therefore we are oversampling), we get

$$I = Q\,f = f\,C_1(V_1(t) - V_2(t)) \; ; \; R = 1 / (C_1\,f)$$

where f = clock frequency.

Basic Switched Capacitors





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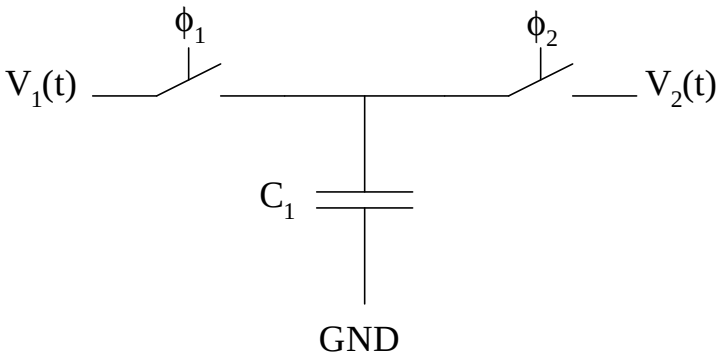


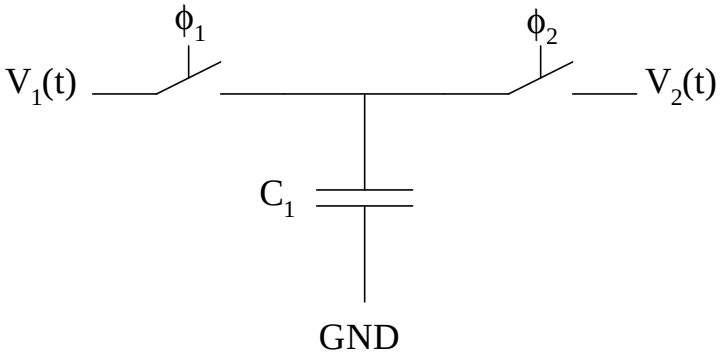
$\sim$

$R = 1 / (C_1 f)$

where f = clock frequency.

For 0.1pF capacitor,
and a 10kHz clock,
we get a resistance of 1GOhm

Basic Switched Capacitors



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For 0.1pF capacitor,
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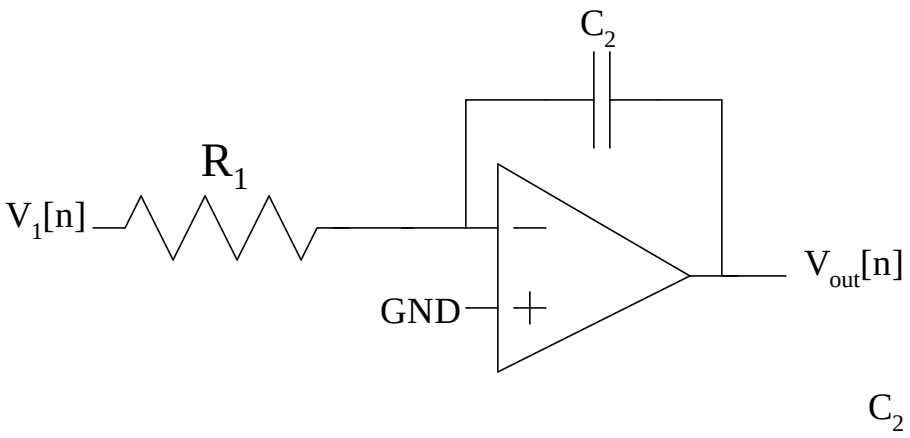
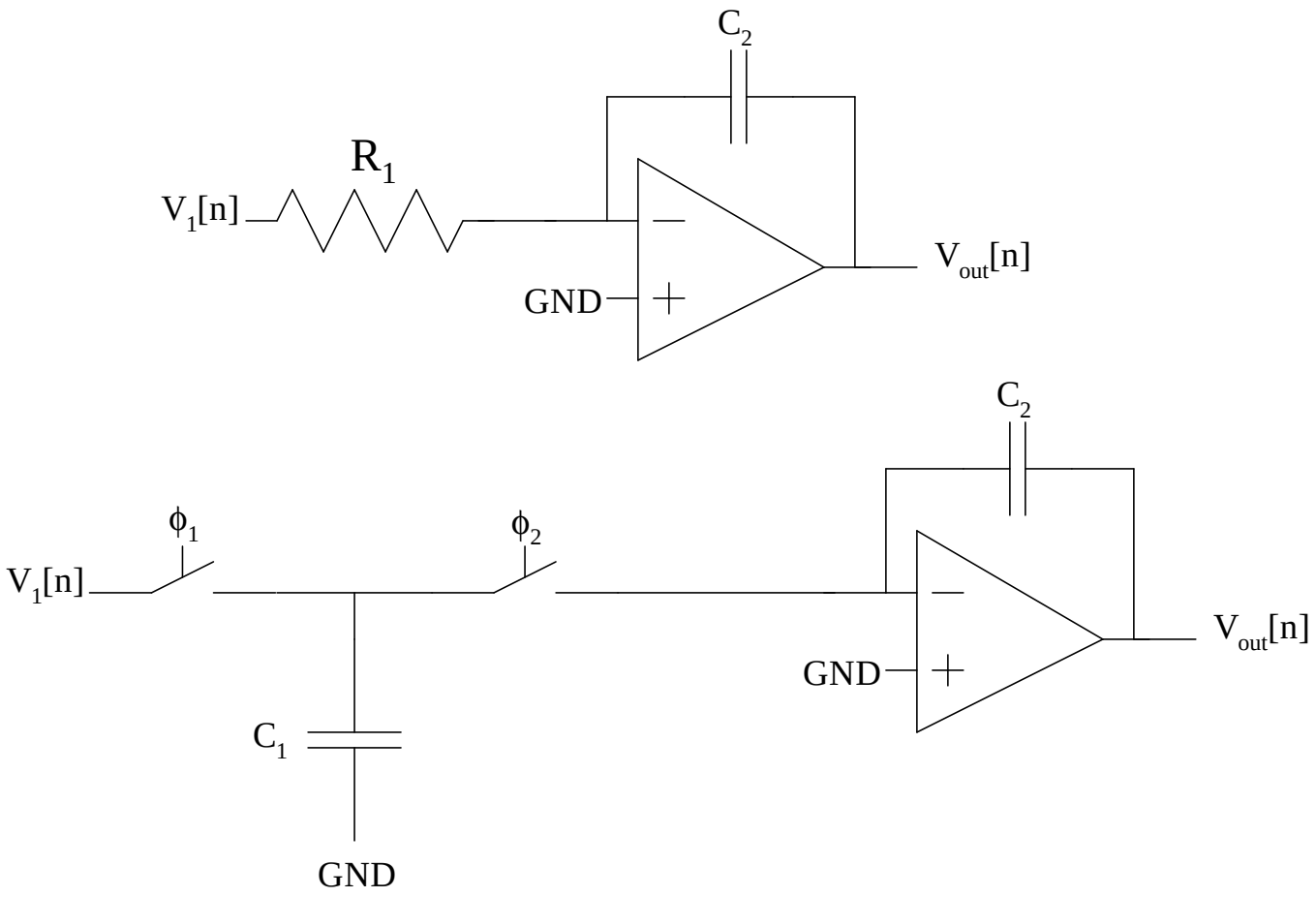
Rule of thumb: slow moving means
we oversample the Nyquist frequency of the input signal by a factor of 20 or more.

Basic Switch-Cap Integrator



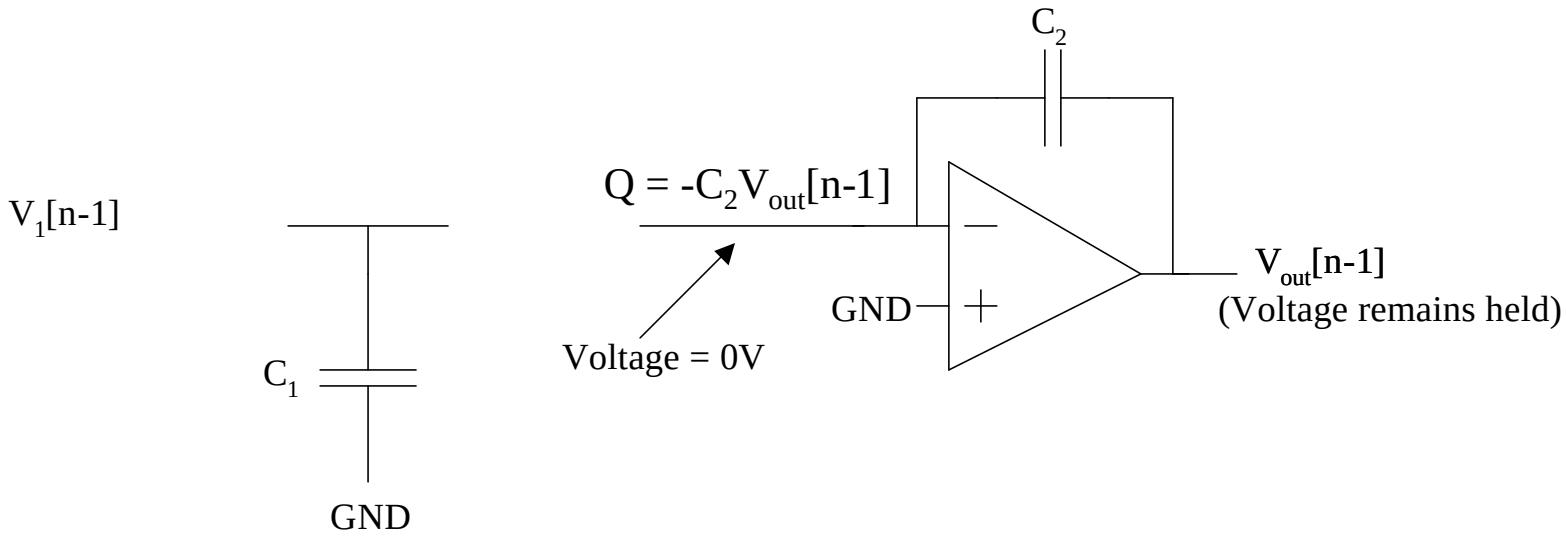
Basic Switch-Cap Integrator



- We will step through all four phases, to get the proper result.

Basic Switch-Cap Integrator

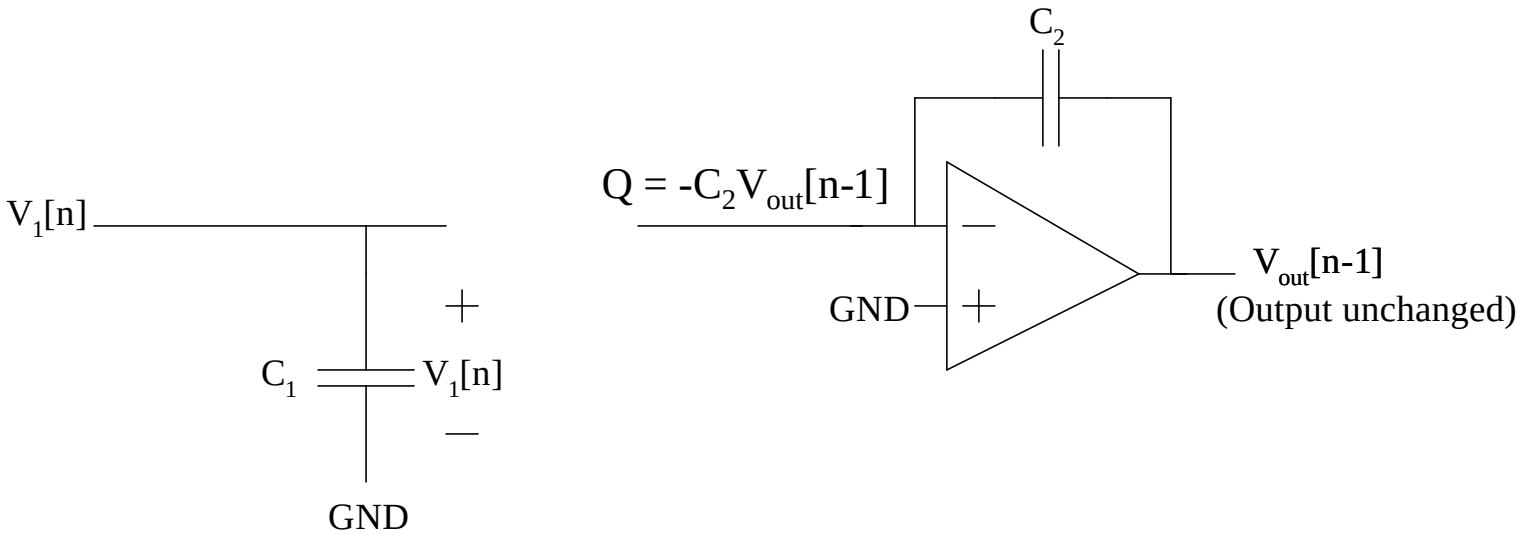
(4), [n-1] cycle



- This case is important to understand our starting point
  charge is stored on a capacitor ; therefore we need to know the initial state

Basic Switch-Cap Integrator

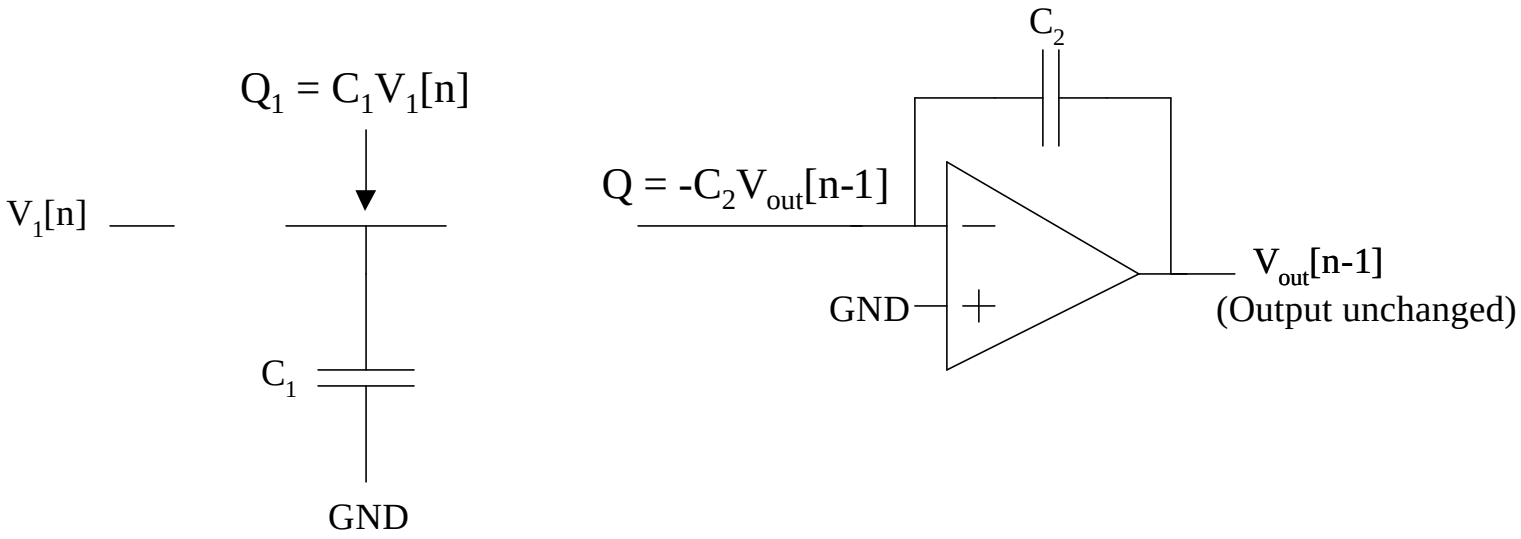
(1), [n] cycle: ϕ_1



- Charge up the capacitor with voltage $V_1[n]$

Basic Switch-Cap Integrator

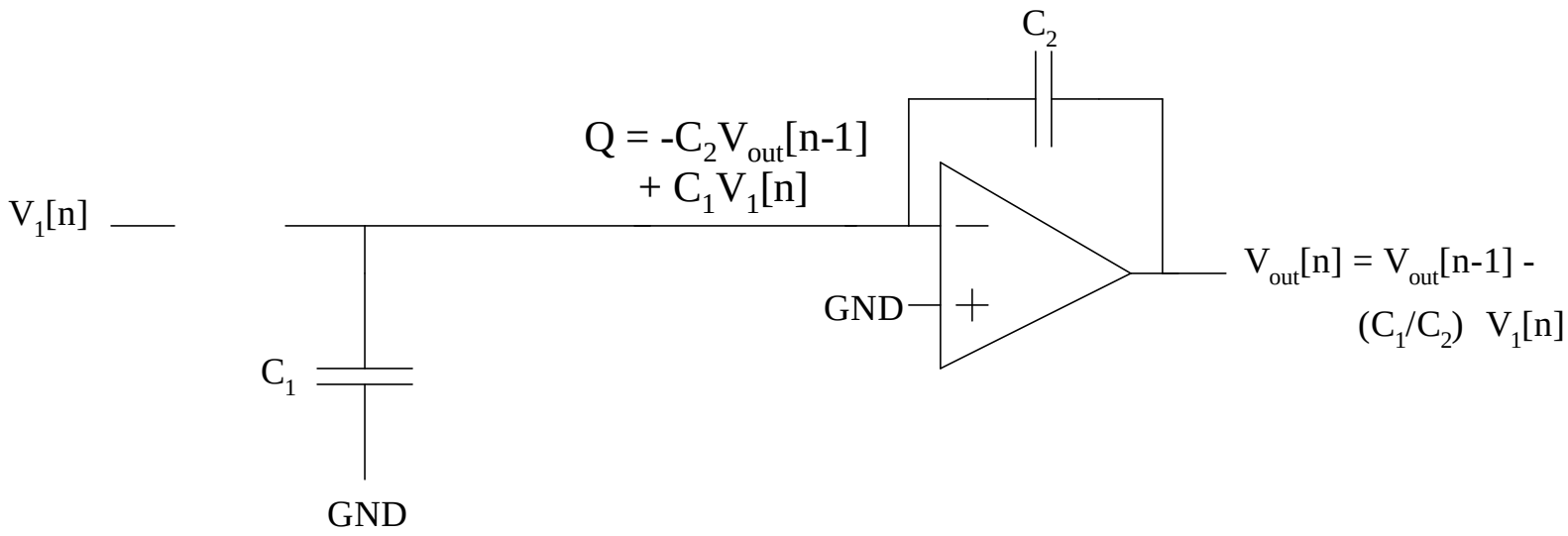
(2), [n] cycle



- We remove the capacitor from the input voltage.
- The voltage is stored across the capacitor

Basic Switch-Cap Integrator

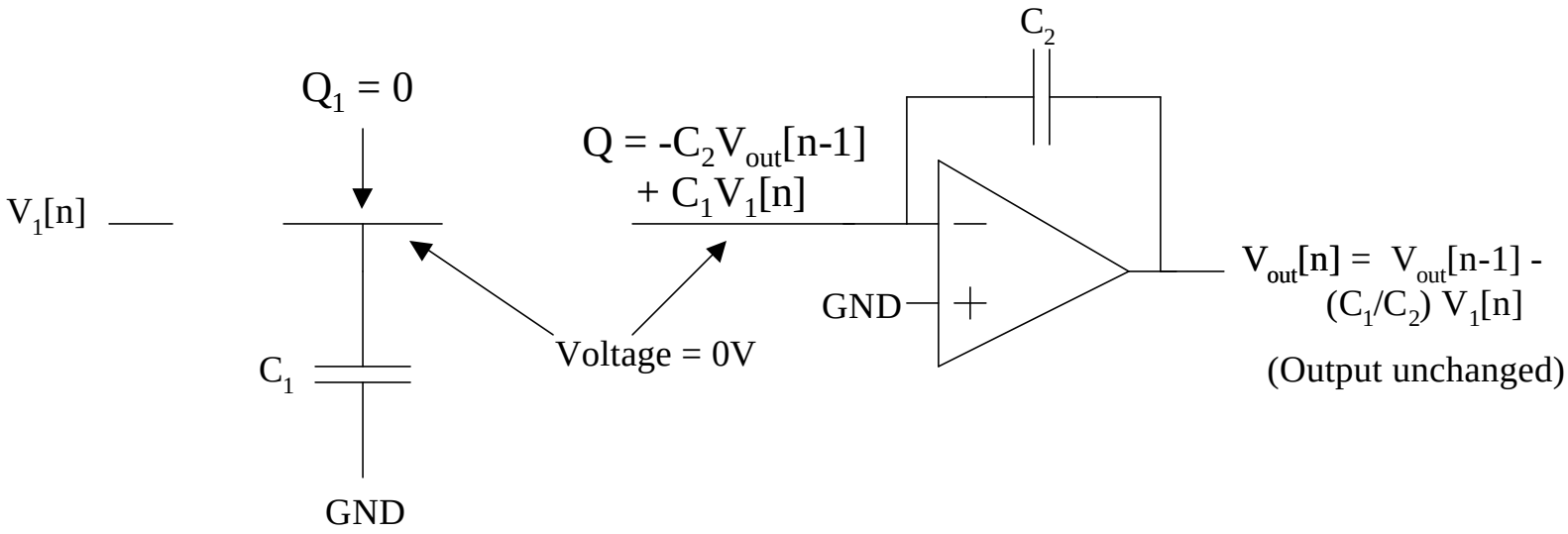
(3), [n] cycle: ϕ_2



- We connect the capacitor to the charge summing node
- The charge initially stored on the capacitor as well as the resulting charge from the second input ($V_2[n]$) contributes to the total charge

Basic Switch-Cap Integrator

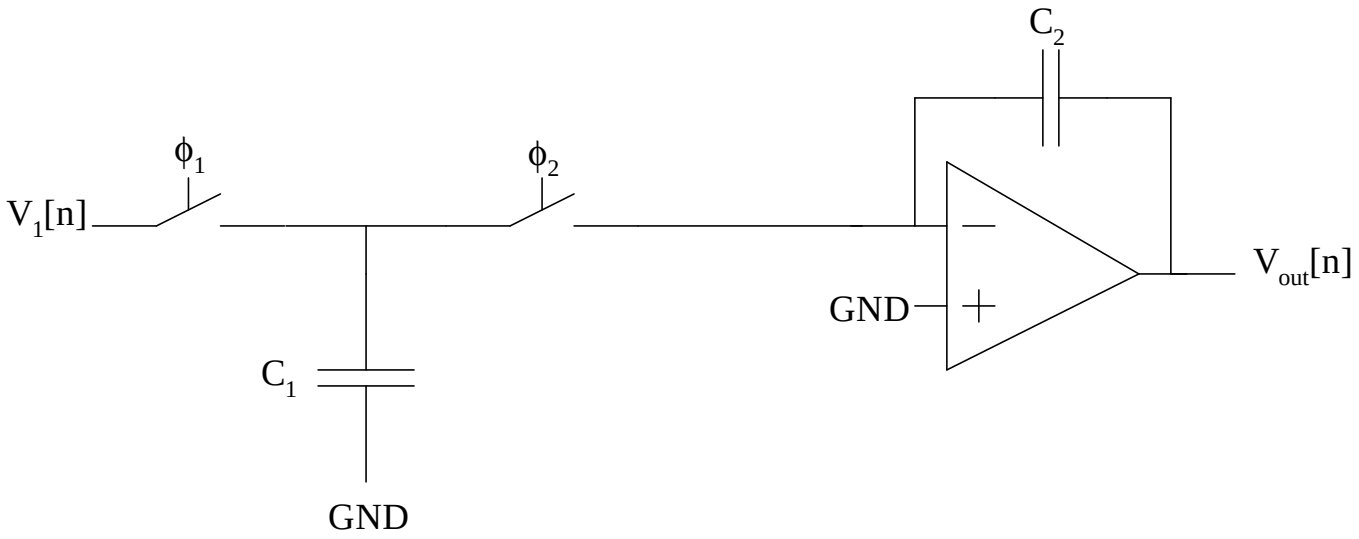
(4), [n] cycle



- We disconnect the capacitor from the charge summing node, and return to our initial case

$$V_{out}[n] = V_{out}[n-1] - (C_1/C_2)\, V_1[n]$$

Basic Switch-Cap Integrator



$$V_{out}[n] = V_{out}[n-1] - (C_1/C_2)\, V_1[n]$$

$$\frac{V_{out}(z)}{V_1(z)} = H(z) = -(C_1/C_2)\,\frac{1}{1 - z^{-1}}$$

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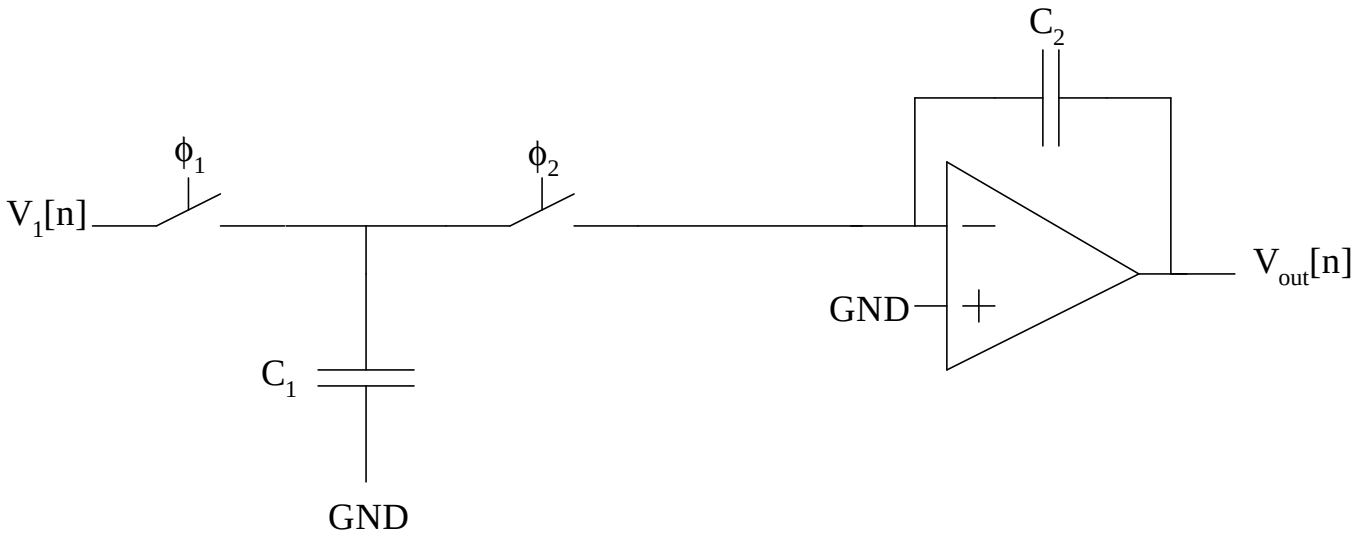

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$$H(j\omega) = -(C_1/C_2)\,\frac{1}{1 - e^{-j\omega T}}$$

$$\sim -(C_1/C_2)\ /\ j\omega T$$

assumes $\omega T << 1$; therefore
we need to sample much higher
(factor of 10 to 20)
over frequencies of interest.