Basic Sample and Hold Element

Prof. Paul Hasler
Georgia Institute of Technology
Sample and Hold Elements

Sample and Hold Block (S/H)
Sample and Hold Elements

Sample and Hold Block (S/H)

Input → Sample and Hold Block (S/H) → Output

Clock

Amplitude

Clock

Input

Time
Sample and Hold Elements

Sample and Hold Block (S/H)

Input → Sample and Hold Block (S/H) → Output

Clock → Sample and Hold Block (S/H)

Amplitude

Clock

Input

Output

Time
Sample and Hold Elements

Sample and Hold Block (S/H)

Input → Sample and Hold Block (S/H) → Output

Clock

Amplitude

Clock

Input → Output

Valid Output

Time
Sample and Hold Elements

Sample and Hold Block (S/H)

Input \rightarrow \text{Sample and Hold Block (S/H)} \rightarrow \text{Output}

Clock

Settling time \( (t_s) = \) time required to settle to the final held voltage to within an accuracy tolerance

Amplitude

Clock

Input

Output

Valid Output

Time

\( t_s \)
Sample and Hold Elements

Sample and Hold Block (S/H)

Clock

Input → Sample and Hold Block (S/H) → Output

Acquisition time \( t_a \) = time required to acquire the analog voltage

Amplitude

Clock (Hold) → (Sample) → (Hold)

Input

Output

Valid Output

Time

\( t_s \)
Sample and Hold Elements

Sample and Hold Block (S/H)

Input $\rightarrow$ Sample and Hold Block (S/H) $\rightarrow$ Output

Clock

$T_{\text{sample}} = t_a + t_s$

$F_{\text{sample(max)}} < \frac{1}{T_{\text{sample}}}$

Amplitude

Clock

(Hold) $\rightarrow$ (Sample) $\rightarrow$ (Hold)

Input $\rightarrow$ Output

$F_{\text{sample(max)}} < \frac{1}{T_{\text{sample}}}$

Valid Output

Input

Output

Time
Sample and Hold Elements

Sample and Hold Block (S/H)

- **Aperture time** = the time required for the sampling switch to open after the S/H command is initiated
- **Aperture jitter** = variation in the aperture time due to clock variations and noise

Amplitude

Clock

Input

Output

Time

• Aperture time = the time required for the sampling switch to open after the S/H command is initiated
• Aperture jitter = variation in the aperture time due to clock variations and noise

\[ t_a \]

\[ t_s \]
Basic Sample and Hold Element

\[ V_{\text{in}}(t) \rightarrow \text{CK} \rightarrow V_{\text{out}}(t) \]

\[ C_1 \]

\[ \text{GND} \]
Basic Sample and Hold Element
Basic Sample and Hold Element

\[ V_{\text{in}}(t) \rightarrow V_{\text{out}}(t) \]

\[ C_1 \]

\[ \text{GND} \]

\[ \text{CK} = 1 \ (V_{\text{dd}}) \]

\[ V_{\text{in}}(t) \rightarrow V_{\text{out}}(t) \]

\[ 1 \]

\[ C_1 \]

\[ \text{GND} \]
Basic Sample and Hold Element

\[
\begin{align*}
V_{in}(t) & \quad \text{CK} \quad V_{out}(t) \\
\quad & \quad C_1 \\
\quad & \quad \text{GND}
\end{align*}
\]

\[
\begin{align*}
V_{in}(t) & \quad 1 \quad V_{out}(t) \\
\quad & \quad C_1 \\
\quad & \quad \text{GND}
\end{align*}
\]

\[
\begin{align*}
\text{CK} = 1 \ (V_{dd})
\end{align*}
\]

\[
\begin{align*}
V_{in}(t) & \quad 1 \quad V_{out}(t) \\
\quad & \quad C_1 \\
\quad & \quad \text{GND}
\end{align*}
\]

\[
\begin{align*}
\text{CK} \quad \text{CK}
\end{align*}
\]
Basic Sample and Hold Element

When CK = 1 (Vdd):

\[ V_{in}(t) \rightarrow V_{out}(t) \]

When CK = 0 (Vdd):

\[ V_{in}(t) \rightarrow V_{out}(t) \]
Basic Sample and Hold Element

\[ V_{in}(t) \quad CK \quad V_{out}(t) \quad C_1 \quad GND \]

\[ V_{in}(t) \quad CK \quad V_{out}(t) \quad C_1 \quad GND \]

CK = 1 (Vdd)

\[ V_{in}(t) \quad V_{out}(t) \quad C_1 \quad GND \]

CK = 0 (Vdd)

\[ V_{in}(t) \quad V_{out}(t) \quad C_1 \quad GND \]
Acquisition and Hold Time

Acquisition Time

\[ V_{in}(t) \quad \text{CK} \quad V_{out}(t) \]
\[ \begin{array}{c} \text{GND} \\ \downarrow \end{array} \]
\[ R_{on} \quad V_{in}(t) \quad V_{out}(t) \]
\[ \begin{array}{c} \text{GND} \\ \end{array} \]

but \( R_{on} \) is not a constant….

Hold Time

\[ 0V \quad V_{in}(t) \]
\[ \begin{array}{c} \text{GND} \\ \downarrow \end{array} \]
\[ I_2 \quad I_1 \quad V_{out}(t) \]
\[ \begin{array}{c} \text{GND} \\ \text{GND} \end{array} \]

\( I_2(t) \): Leakage through the reversed-biased pn junction
Typically 1fA to 100fA (dark)

\( I_1(t) \): Leakage through the MOS transistor
Can be negligible with correct biasing

\[ C_1 \quad \text{Hold time (1mV drop) with } I_2(t) = 10fA \]
\[ \begin{array}{c|c}
10pF & 1s \\
1pF & 100ms \\
100fF & 10ms \\
10fF & 1ms
\end{array} \]
Basic S/H elements

Sample and Hold Block (S/H)

Input → Sample and Hold Block (S/H) → Output

Clock
Basic S/H elements

Sample and Hold Block (S/H)

Input → Sample and Hold Block (S/H) → Output

Clock

$V_{in}(t)$ → $V_{out}(t)$

$C_1$

GND
Basic S/H elements

Would use a buffer to drive loads that are not purely capacitive
S/H elements

Input \rightarrow \text{Sample and Hold Block (S/H)} \rightarrow \text{Output}

Clock

More accurate, but slower

$V_{\text{in}(t)}$ \rightarrow $\phi_1$ \rightarrow $\phi_2$ \rightarrow $V_{\text{out}[n]}$

$\phi_1$ and $\phi_2$ are non-overlapping clocks
Non-Overlapping Clocks

We will always be using non-overlapping clocks; therefore, we want a waveform like

\[ \phi_1, \phi_2 \]

We effectively have four phases.
Non-Overlapping Clocks

We will always be using non-overlapping clocks; therefore, we want a waveform like

\[
\begin{align*}
\phi_1 \\
\phi_2 \\
\end{align*}
\]

We effectively have four phases.

Would want \( t_d \) as small as possible for proper operation.

We will also assume that the input is held constant through the entire \([n]^{th}\) cycle.
Non-Overlapping Clocks

We will always be using non-overlapping clocks; therefore, we want a waveform like

\[ \phi_1 \]
\[ \phi_2 \]

We effectively have four phases.

\[ t_d \]

Would want \( t_d \) as small as possible for proper operation.

We will also assume that the input is held constant through the entire \([n]^{th}\) cycle.
S/H elements

Sample and Hold Block (S/H)

Input

Clock

Output

Initial Phase \((\phi_1, \phi_2 = 0)\)

\(V_{in}(t)\)

\(V_{out}[n-1]\)
S/H elements

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Clock

Phase I (φ₁ = 1, φ₂ = 0)

V_{in}(t) → \phi₁ → V_{out}(t) \sim V_{in}(t)
S/H elements

Phase II ($\phi_1, \phi_2 = 0$)

$V_{in}(t)$

$V_{out}[n]$
S/H elements

Sample and Hold Block (S/H)

Input → Sample and Hold Block (S/H) → Output

Clock

$V_{in}(t)$ are $\sim V_{in}(t)$; therefore ready for the next phase
**S/H elements**

Sample and Hold Block (S/H)

Input \[ \rightarrow \] Sample and Hold Block (S/H) \[ \rightarrow \] Output

Clock

\[ V_{in}(t) \]

\[ \phi_1 \]

\[ \phi_2 \]

\[ V_{out}[n] \]

\( \phi_1 \) and \( \phi_2 \) are non-overlapping clocks
S/H elements

• Basic S/H concepts
• Basic MOS switch issues
• Basic MOS S/H elements
• An additional S/H element