ADCs for High-Speed Applications

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ADCs for High-Speed Applications

ADC Concepts:
- quantization
- sampling

ADC Specifications:
- static specifications
- dynamic specifications

ADC Architectures:
- classical architectures
- “new” architectures

Summary
ADC Concepts

- continuous time
- continuous amplitude

- discrete time
- discrete values

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Quantization and Resolution

Quantization:
- continuous amplitudes represented with discrete levels

FS = Full Scale
LSB = Least Significant Bit

Resolution (1 LSB):
- smallest noticeable change

\[ V_{LSB} = \frac{V_{FS}}{2^N} \]

Converter Resolution = N
Quantization Noise & SNR

Quantization noise:
- quantization errors appear as noise with an RMS level of

\[ \sqrt{\frac{v^2}{qn}} = \frac{V_{LSB}}{\sqrt{12}} \]

Signal-to-Noise Ratio (SNR):
- full-scale sine wave \( V_{sig} = 2^N V_{LSB}/2\sqrt{2} \)

\[ SNR = 20\log\left(\frac{V_{sig}}{\sqrt{v^2_{qn}}}\right) = [6.02N + 1.76] \text{dB} \]

\[ SNR \approx 6N \text{dB} \]

Notes for quantization noise:
Quantization noise can be calculated by assuming the signal within any quantization step has a uniform distribution, as shown in the sketch to the right. The error for a particular sample will simply be the distance between \( x \) and the origin where \( -V_{LSB}/2 < x < V_{LSB}/2 \). The rms error or the quantization noise can then be calculated as:

\[ v_{qn} = \sqrt{\frac{1}{V_{LSB} - V_{LSB}/2} \int_{-V_{LSB}/2}^{V_{LSB}/2} x^2 dx} = \frac{V_{LSB}}{\sqrt{12}} \]
SNR and Resolution: the Practical Case

Quantization is not the only noise source:

\[
SNR = 20 \log \left( \frac{V_{\text{sig}}}{\sqrt{\frac{v_{\text{qn}}^2 + v_n^2}} N} \right)
\]

![Graph showing SNR vs. Noise (v_n) for Ideal and Real 12-bit and 10-bit scenarios with SNR levels at 74dB and 62dB.](image)

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Concepts & Specifications, page 6
$SNR$ & Effective Number of Bits

Measuring $SNR$:
- $f_{in} < f_s/2$
- noise bandwidth = $f_s/2$
- $SNR$ increases with the signal
- ideal $SNR$
  $$SNR_{max} = (6N + 1.76)\text{dB}$$

Effective Number of Bits:
- ideally $ENOB = N$
- circuit nonlinearities and noise reduce $ENOB$ to:
  $$ENOB = \frac{SNR_{max} - 1.76}{6.02}$$

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Notes for signal-to-noise:

The maximum SNR for an ideal N-bit ADC can be calculated by assuming the input is a sine wave and the only noise source is quantization noise. The largest peak-to-peak value of the sine wave is $2^NV_{\text{LSB}}$ which has an RMS value of $2^NV_{\text{LSB}}/2\sqrt{2}$. Knowing the quantization noise is $V_{\text{LSB}}/\sqrt{12}$, one can express the SNR as:

$$SNR = 20\log\left(\frac{2^NV_{\text{LSB}}/2\sqrt{2}}{V_{\text{LSB}}/\sqrt{12}}\right)$$

which reduces to:

$$SNR = 6.02N + 1.76 \ \text{dB}$$

Solving the above equation for $N$, yields the effective number of bits from the maximum SNR

$$ENOB = (SNR_{max} - 1.76)/6.02$$
Sampling, Nyquist and Aliasing

Signal spectrum:

Sampled spectrum with $f_s > 2f_{BW}$:

Sampled spectrum with $f_s < 2f_{BW}$:

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Aliasing in the Time Domain

- signals beyond $f_s/2$ are aliased to below $f_s/2$
- useful for down conversion from IF to baseband
Sampling & Anti-Aliasing Filtering (ADCs)

Nyquist Criterion \( f_s > 2f_{BW} \)

Ideal Case: \( f_s = 2f_{BW} \)

- Filter = ideal brick wall
- Attenuation sufficient to suppress out-of-band noise below 6NdB

Practical Case: digital audio

- Practical filter
- Audio signal

\( f_s = 44kHz \)

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1. Strictly, there should be NO signal energy at half the sampling frequency

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Concepts & Specifications, page 10
Oversampling & Anti-Aliasing Filters

Oversampling eases filtering requirements:

- simple analog filter

- high order digital filters can have sharp transitions & linear phase
Oversampling & Quantization Noise

Quantization noise is uniform between 0 and $f_s/2$

$f_s = 2f_{BW}$:

$f_s = 8(2f_{BW})$:

In-band $SNR$:

$$SNR = [6.02N + 1.76 + 10\log\left(\frac{f_s}{2f_{BW}}\right)] \text{dB}$$
ADC Concepts

Summary

Quantization determines resolution:
- smallest discernible step = 1 LSB
- more bits = more resolution
- $SNR \approx 6N\text{dB}$

Sampling rate determines useful bandwidth:
- $f_s > 2f_{BW}$ - Nyquist criterion
- $f_s \gg 2f_{BW}$ - eases analog filtering

\[
SNR = \left[ 6N + 1.76 + 10\log\left(\frac{f_s}{2f_{BW}}\right) \right]\text{dB}
\]
Specifying ADCs

DC Specifications:
- $f_s << f_{clk}$
- "optimal" specifications

Dynamic Specifications:
- $f_s \sim f_{clk}$
- indicates performance degradation for high signal frequencies
- "realistic" specifications
DC Specifications

Ideal output: \[ V_{OUT} = V_{REF} \left[ \frac{b_{n-1}}{2} + \cdots + \frac{b_0}{2^N} \right] \]

- MSB (most significant bit) = \( b_{n-1} \)
- LSB (least significant bit) = \( b_0 \)
- Full Scale input (or output) = \( V_{REF} \left[ \frac{2^N - 1}{2^N} \right] \approx V_{REF} \)
Ideal ADCs and DACs

- levels are uniformly spaced:

\[ 1\text{LSB} = \frac{V_{\text{REF}}}{2^N} \]

- slope = 45°, intercept = origin

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Gain and Offset Errors

3-bit ADC example:

Offset Error: difference between zero intercept and the origin
- expressed in LSBs

Gain Error: difference between real and ideal slopes
- often expressed in LSBs from ideal full scale
Linearity Errors

**Differential Non-Linearity (DNL):**
- difference between real & ideal step size

**Integral Non-Linearity (INL):**
- difference between step midpoint and line joining end points

**Missing Codes:**
- excessive DNL leads to missed codes in ADCs

**Non-Monotonicity:**
- excessive DNL leads to non-monotonic behavior in ADCs
Spurious Free Dynamic Range (SFDR)

- INL, DNL and finite slew rates cause distortion

SFDR:
- is a measure of harmonic distortion
- ideally SFDR > SNR

To Measure:
- noise bandwidth
  \[ \Delta f \ll \frac{f_s}{2} \]
- input sine wave
  \[ f_{in} \ll \frac{f_s}{2} \]
Signal-to-Noise and Distortion (SINAD)

SINAD:
- noise and distortion degrade an ADC’s performance

\[
SINAD = 20 \log \left( \frac{V_{sig}}{\sqrt{v_{n\text{ (total)}}^2 + THD^2}} \right)
\]

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Concepts & Specifications, page 20
ADC Bandwidth Specifications

Nyquist:
- bandwidth = $f_s/2$

Full Power BW ($f_{3dB}$):
- fundamental down 3dB
- typically $f_{3db} > f_s/2$

Resolution BW ($f_{RBW}$):
- SINAD down 3dB
  (1/2 bit = 3dB)
- ideally $f_{RBW} > f_s/2$

$f_{3dB}$ & $f_{RBW}$ are usually independent of $f_s/2$
Sampling Errors (Jitter)

Jitter:
- most systems assume the signal is sampled uniformly.
- clock noise leads to non-uniform sampling (i.e. jitter).

• leads to SNR degradation for high frequency inputs.

\[ 2\pi f_a T_j V_p < V_{LSB} \]

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Notes for jitter:

Jitter introduces uncertainty in the sampling instant that leads to uncertainty in the sampled value resulting in a degradation in the SNR. The effects of jitter depend on the slope of the signal at the sampling instant. A sine wave of frequency \( f_a \) with a peak value of \( V_p \) can be expressed as \( V_p \sin(2\pi f_a t) \). The slope of this wave form at any time is given by:

\[ \frac{\partial v}{\partial t} = 2\pi f_a V_p \cos(2\pi f_a t) \]

The worst case slope occurs at \( t = 0 \) and is given by \( 2\pi f_a V_p \). If the sampling clock has an rms jitter of \( T_j \) one can substitute for \( \partial t \) to solve for the worst case \( \partial v \):

\[ \partial v = 2\pi f_a V_p T_j \]

A nominal target for \( \partial v \) is to keep it below one LSB or

\[ 2\pi f_a V_p T_j < V_{LSB} \]
ADC Specification Summary

For true N-bit performance:

- \( \text{INL} < \pm \frac{1}{2} \text{LSB} \)
- \( \text{DNL} < \pm \frac{1}{2} \text{LSB} \)
- \( \text{ENOB} \sim N \)
- \( \text{SFDR} > 6N \text{dB} \)
- \( f_{RBW} > f_s / 2 \)