NYQUIST FREQUENCY ANALOG-DIGITAL CONVERTERS

The sampled nature of the ADC places a practical limit on the bandwidth of the input signal. If the sampling frequency is f_S, and f_B is the bandwidth of the input signal, then

$$f_B < 0.5f_S$$

which is simply the *Nyquist* relationship which states that to avoid aliasing, the sampling frequency must be greater than twice the highest signal frequency.

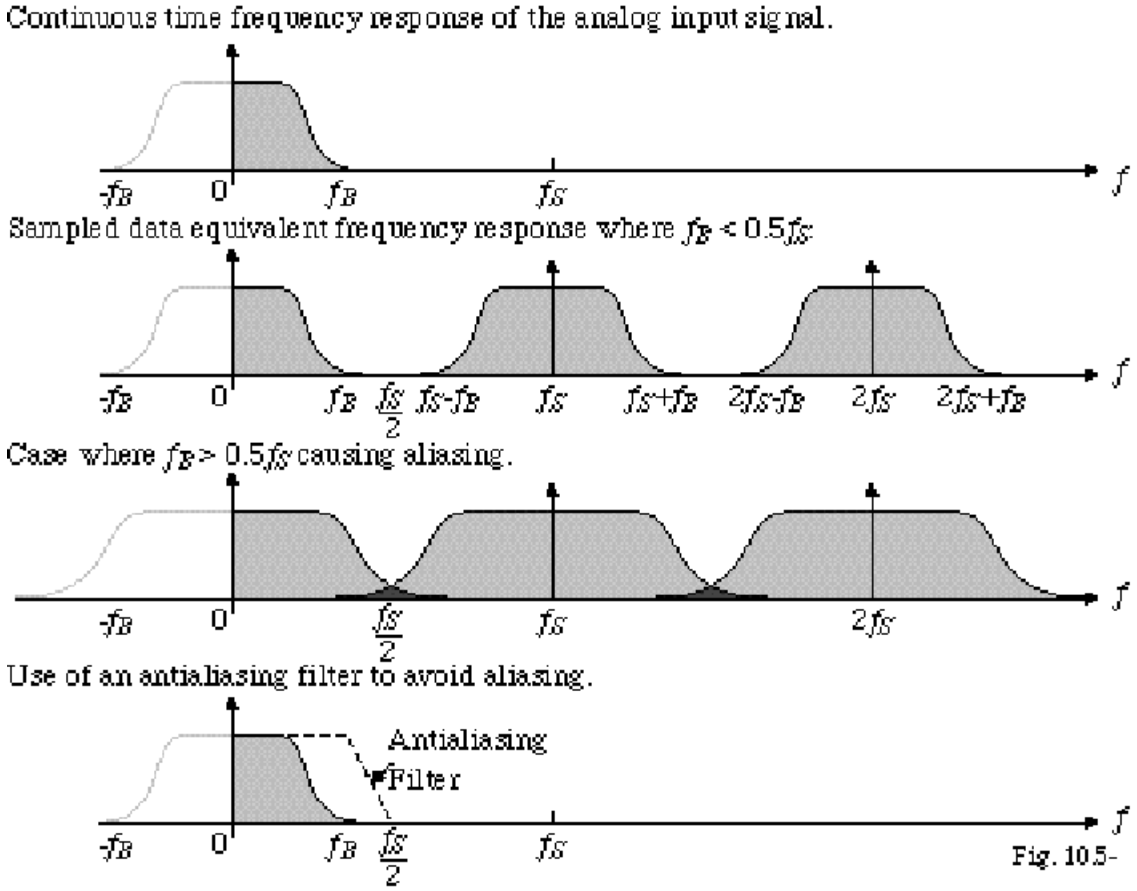


Fig. 10.5-

CLASSIFICATION OF ANALOG-DIGITAL CONVERTERS

Analog-digital converters can be classified by the relationship of f_B and $0.5f_S$ and by their conversion rate.

- *Nyquist ADCs* - ADCs that have f_B as close to $0.5f_S$ as possible.
- *Oversampling ADCs* - ADCs that have f_B much less than $0.5f_S$.

Table 10.5-1 - Classification of Analog-to-Digital Converter Architectures

Conversion Rate	Nyquist ADCs	Oversampled ADCs
Slow	Integrating (Serial)	Very high resolution >14 bits
Medium	Successive Approximation 1-bit Pipeline Algorithmic	Moderate resolution >10 bits
Fast	Flash Multiple-bit Pipeline Folding and interpolating	Low resolution > 6 bits

STATIC CHARACTERIZATION OF ANALOG-TO-DIGITAL CONVERTERS

DIGITAL OUTPUT CODES

Table 10.5-2 - Digital Output Codes used for ADCs

Decimal	Binary	Thermometer	Gray	Two's Complement
0	000	0000000	000	000
1	001	0000001	001	111
2	010	0000011	011	110
3	011	0000111	010	101
4	100	0001111	110	100
5	101	0011111	111	011
6	110	0111111	101	010
7	111	1111111	100	001

INPUT-OUTPUT CHARACTERISTICS

Ideal input-output characteristics of a 3-bit ADC

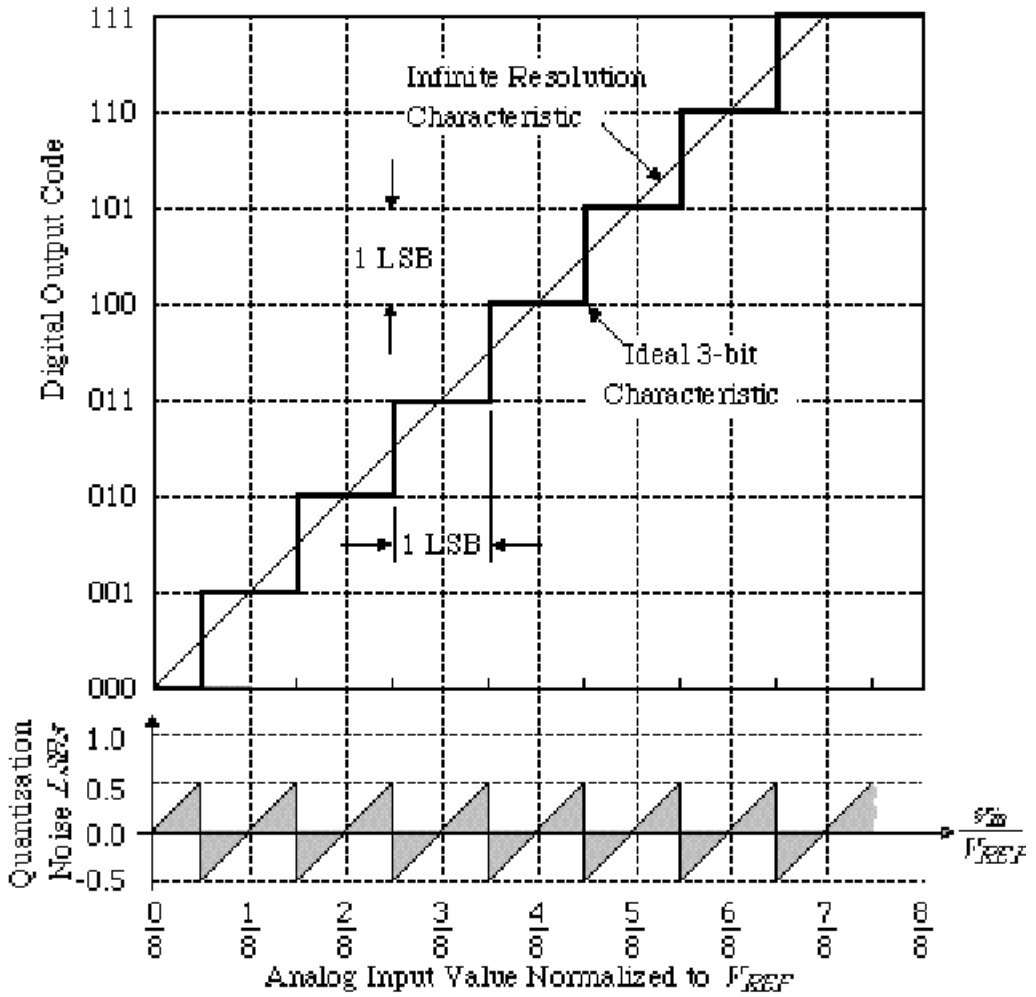


Figure 10.5-3 Ideal input-output characteristics of a 3-bit ADC.

DEFINITIONS

- The *dynamic range*, *signal-to-noise ratio (SNR)*, and the *effective number of bits (ENOB)* of the ADC are the same as for the DAC
- *Resolution* of the ADC is the smallest analog change that can be distinguished by an ADC.
- *Quantization Noise* is the ±0.5*LSB* uncertainty between the infinite resolution characteristic and the actual characteristic.
- *Offset Error* is the horizontal difference between the ideal finite resolution characteristic and actual finite resolution characteristic
- *Gain Error* is the horizontal difference between the ideal finite resolution characteristic and actual finite resolution characteristic which is *proportional* to the analog input voltage.

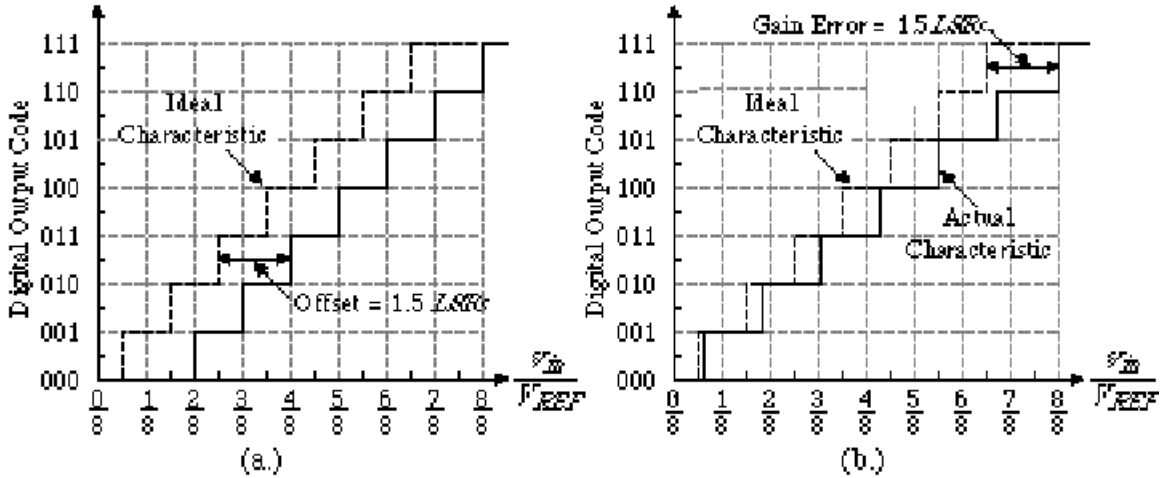


Figure 10.5-4 - (a.) Example of offset error for a 3-bit ADC. (b.) Example of gain error for a 3-bit ADC.

INTEGRAL AND DIFFERENTIAL NONLINEARITY

The integral and differential nonlinearity of the ADC are referenced to the vertical (digital) axis of the transfer characteristic.

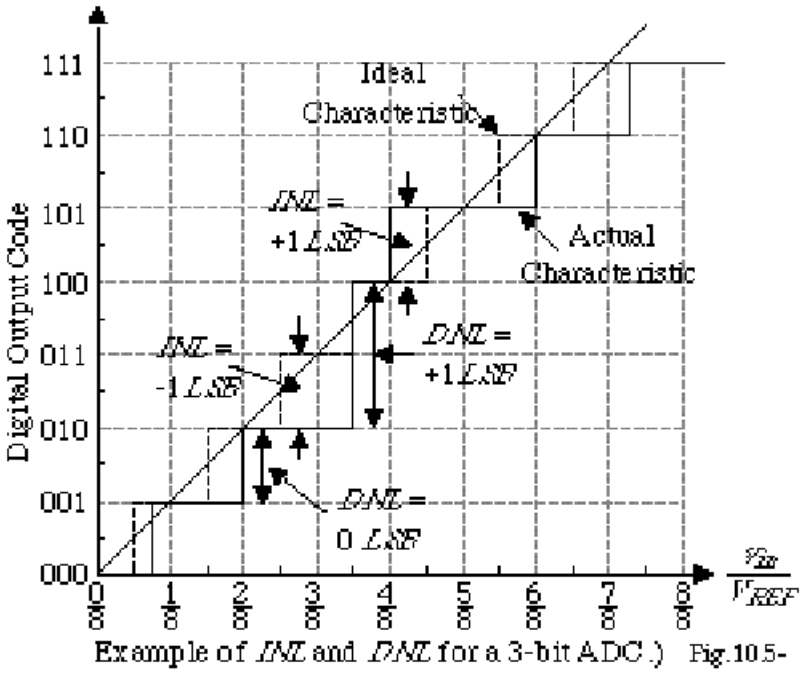
- *Integral Nonlinearity (INL)* is the maximum difference between the actual finite resolution characteristic and the ideal finite resolution characteristic measured vertically (% or *LSB*)
- *Differential Nonlinearity (DNL)* is a measure of the separation between adjacent levels measured at each vertical step (% or *LSB*).

$$DNL = (D_{cx} - 1)\ LSBs$$

where D_{cx} is the size of the actual vertical step in *LSBs*.

Note that *INL* and *DNL* of an analog-digital converter will be in terms of integers in contrast to the *INL* and *DNL* of the digital-analog converter. As the resolution of the ADC increases, this restriction becomes insignificant.

EXAMPLE OF *INL* and *DNL*



Example of *INL* and *DNL* for a 3-bit ADC.) Fig. 10.5-

MONOTONICITY

A *monotonic* ADC has all vertical jumps positive. Note that monotonicity can only be detected by *DNL*.

Example of a nonmonotonic ADC:

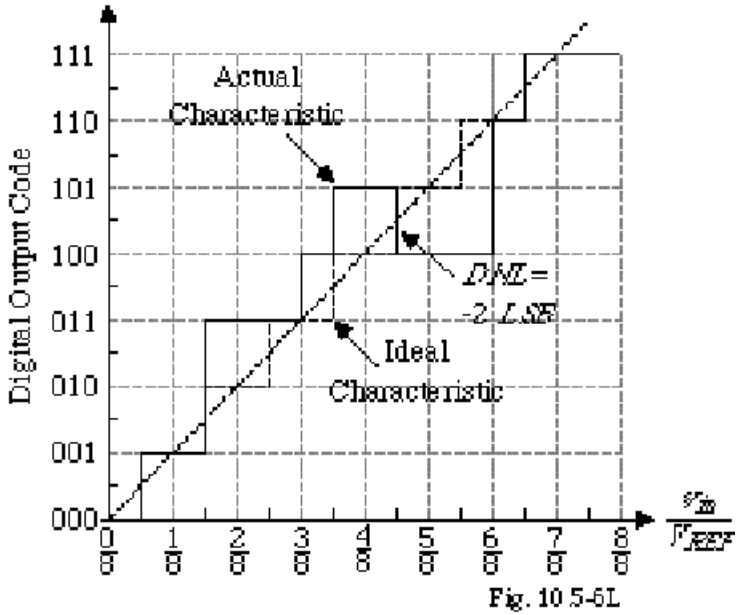


Fig. 10.5-6L

If a vertical jump is 2*LSB* or greater, missing output codes may result.

If a vertical jump is -1*LSB* or less, the ADC is not monotonic.

EXAMPLE 10.5-2

***INL* and *DNL* of a 3-bit ADC**

Find the *INL* and *DNL* for the 3-bit ADC shown on the previous slide.

Solution

With respect to the digital axis:

1.) The largest value of *INL* for this 3-bit ADC occurs between 3/16 to 5/16 or 7/16 to 9/16 and is 1*LSB*.

2.) The smallest value of *INL* occurs between 11/16 to 12/16 and is -2*LSB*.

3.) The largest value of *DNL* occurs at 3/16 or 6/8 and is +1*LSB*.

4.) The smallest value of *DNL* occurs at 9/16 and is -2*LSB* which is where the converter becomes nonmonotonic.

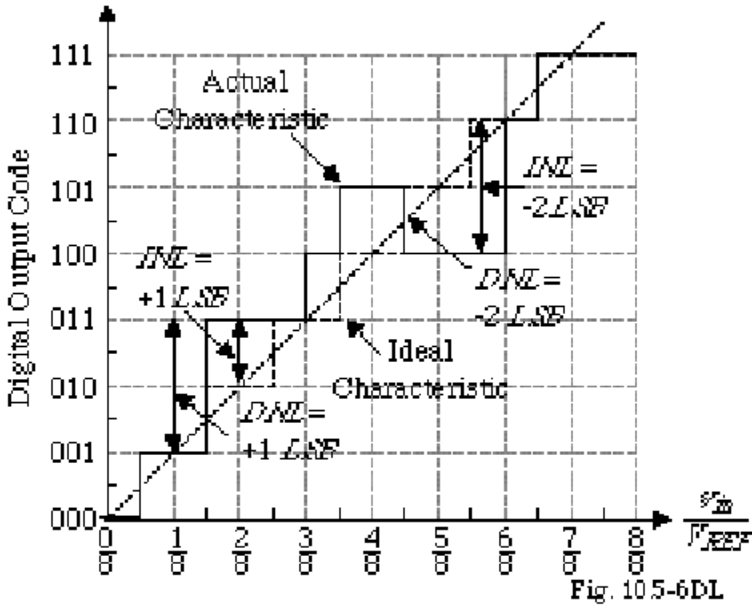


Fig. 10.5-6DL

DYNAMIC CHARACTERISTICS

The dynamic characteristics of ADCs are influenced by:

- Comparators
- Sample-hold circuits
- Circuit parasitics
- Logic propagation delay

COMPARATOR

The comparator is the quantizing unit of ADCs.

Open-loop model:

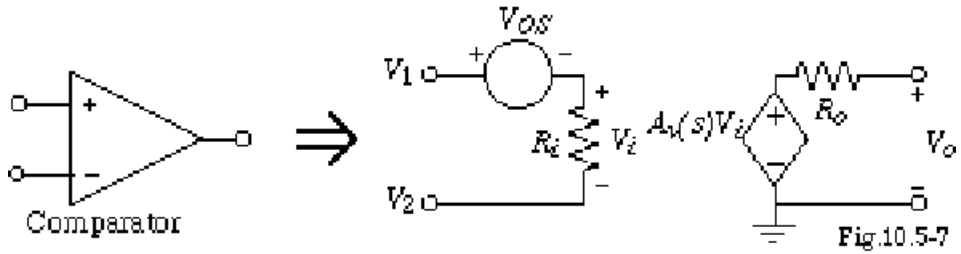


Fig.10.5-7

Nonideal aspects:

- Input offset voltage, V_{OS} (a static characteristic)
- Propagation time delay
  - Bandwidth (linear)

$$A_v(s) = \frac{A_v(0)}{\frac{s}{w_c} + 1} = \frac{A_v(0)}{st_c + 1}$$

  - Slew rate (nonlinear)

$$DT = \frac{C \cdot DV}{I} \quad (I \text{ is constant})$$

LINEAR PROPAGATION TIME DELAY (Small input changes)

If V_{OH} and V_{OL} are the maximum and minimum output voltages of the comparator, then minimum input to the comparator (resolution) is

$$v_{in}(\min) = \frac{V_{OH} - V_{OL}}{A_v(0)}$$

If the propagation time delay, t_p, is the time required to go from V_{OH} or from V_{OL} to $\frac{V_{OH}+V_{OL}}{2}$, then if v_{in}(min) is applied to the comparator, the t_P is,

$$\frac{V_{OH} - V_{OL}}{2} = A_v(0)\,[1 - e^{-t_p/t_c}]\; v_{in}(\min) = A_v(0)\,[1 - e^{-t_p/t_c}]\left(\frac{V_{OH} - V_{OL}}{A_v(0)}\right)$$

Therefore, t_p is

$$t_p(\max) = t_c\, ln(2) = 0.693 t_c$$

If v_{in} is greater than v_{in}(min), i.e. $v_{in} = kv_{in}(\min)$, then

$$t_p = t_c\, ln\left(\frac{2k}{2k - 1}\right)$$

Illustration of these results:

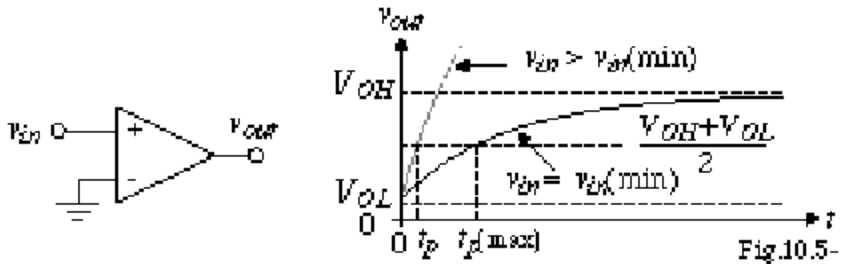


Fig.10.5-

NONLINEAR PROPAGATION TIME DELAY (Large input changes)

The output rises or falls with a constant rate as determined by the slew rate, *SR*.

$$\therefore \qquad t_p = DT = \frac{DV}{SR} = \frac{V_{OH} - V_{OL}}{2 \cdot SR}$$

(If the rate of the output voltage of the comparator never exceeds *SR* , then the propagation time delay is determined by the previous expression.)

EXAMPLE 10.5-2

Propagation Delay Time of a Comparator

Find the propagation delay time of an open loop comparator that has a dominant pole at 10^3 radians/sec, a dc gain of 10^4, a slew rate of 1V/μs, and a binary output voltage swing of 1V. Assume the applied input voltage is 10mV.

Solution

The input resolution for this comparator is $1V/10^4$ or 0.1mV. Therefore, the 10mV input is 100 times larger than $v_{in}(\min)$ giving a k of 100. Using the previous expression for this case, we get

$$t_p = \frac{1}{10^3} ln\left(\frac{2\cdot 100}{2\cdot 100-1}\right) = 10^{-3}\, ln\left(\frac{200}{199}\right) = 5.01\mu s$$

If the output is slew-rate limited, then

$$t_p = \frac{1}{2\cdot 1x10^6} = 0.5\mu s$$

Therefore, the propagation delay time for this case is the larger or 5.01μs.

Note that the maximum slope of the linear response is

$$\text{Max}\left(\frac{dv_{out}}{dt}\right) = \frac{d}{dt}\left(A_v(0)[1-e^{-t/t_c}](0.01V)\right) = \frac{A_v(0)}{t_c} e^{-t/t_c}(0.01V) = \frac{A_v(0)}{100t_c} = \frac{A_v(0)w_c}{100} = \frac{10^4\cdot 10^3}{100} = 0.1V/\mu s$$

Since the maximum rate of the linear response is less than the slew rate, the response is linear and the propagation time delay is 5.01μs.

APERATURE JITTER IN S/H CIRCUITS

Illustration:

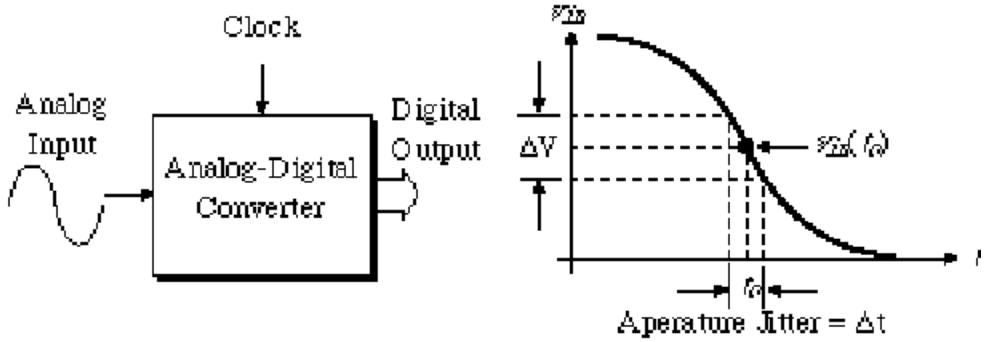


Figure 10.5-14 - Illustration of aperature jitter in an ADC.

If we assume that $v_{in}(t) = V_p sinwt$, then the maximum slope is equal to wV_p.

Therefore, the value of DV is given as

$$DV = \left|\frac{dv_{in}}{dt}\right| Dt = wV_p Dt \ .$$

The rms value of this noise is given as

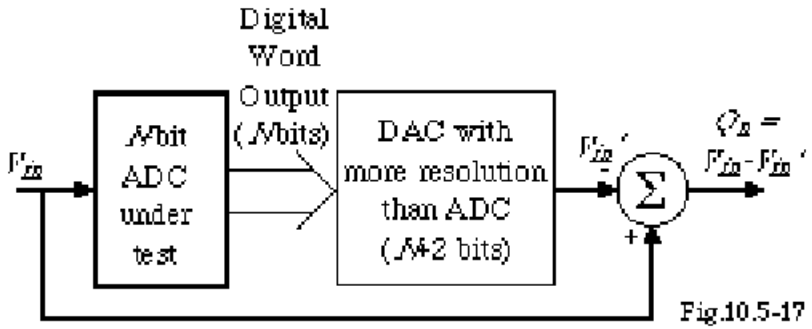
$$DV(\text{rms}) = \left|\frac{dv_{in}}{dt}\right| Dt = \frac{wV_p Dt}{2\sqrt{2}} \ .$$

The aperature jitter can lead to a limitation in the desired dynamic range of an ADC. For example, if the aperature jitter of the clock is 100ps, and the input signal is a full scale peak-to-peak sinusoid at 1MHz, the rms value of noise due to this aperature jitter is 111μV(rms) if the value of V_{REF} = 1V.

TESTING OF ADCs

INPUT-OUTPUT TEST FOR AN ADC

Test Setup:



The ideal value of Q_n should be within $\pm 0.5LSB$

Can measure:

- Offset error = constant shift above or below the 0 *LSB* line
- Gain error = contant increase or decrease of the sawtooth plot as V_{in} is increased
- *INL* and *DNL* (see following page)

ILLUSTRATION OF THE INPUT-OUTPUT TEST FOR A 4-BIT ADC

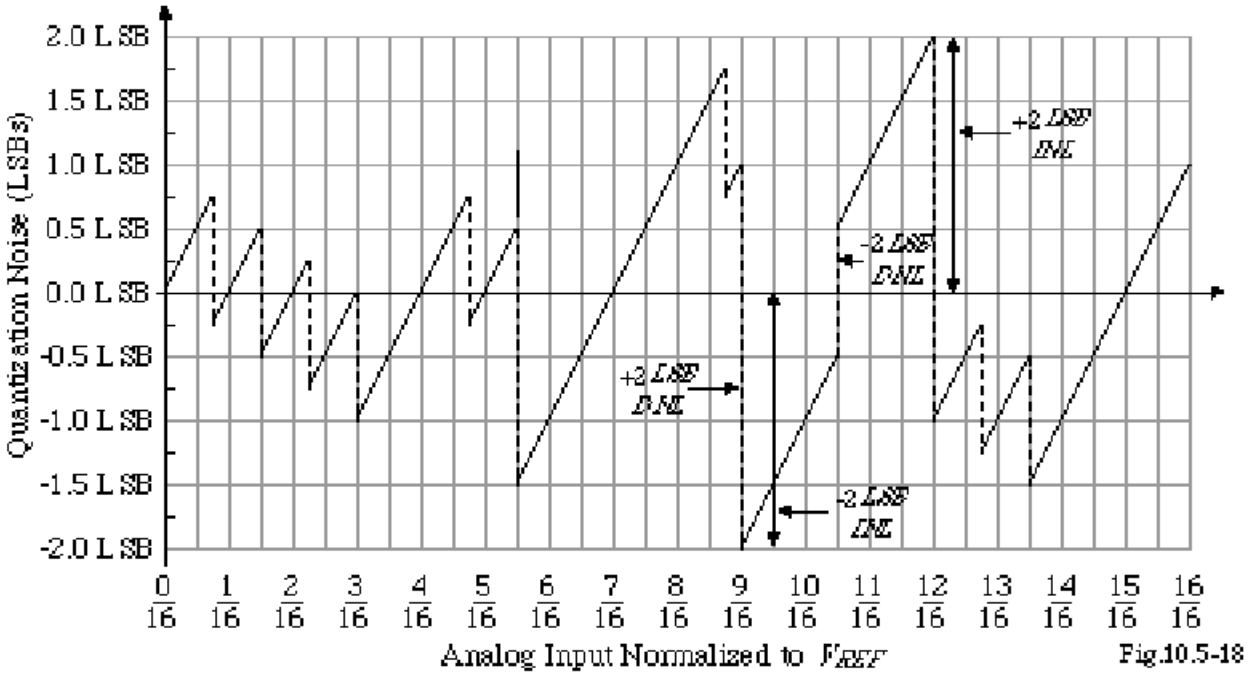


Fig.10.5-18

MEASUREMENT OF NONLINEARITY USING A PURE SINUSOID

This test applies a pure sinusoid to the input of the ADC. Any nonlinearity will appear as harmonics of the sinusoid. Nonlinear errors will occur when the dynamic range (*DR*) is less than 6*N* dB where *N* = number of bits.

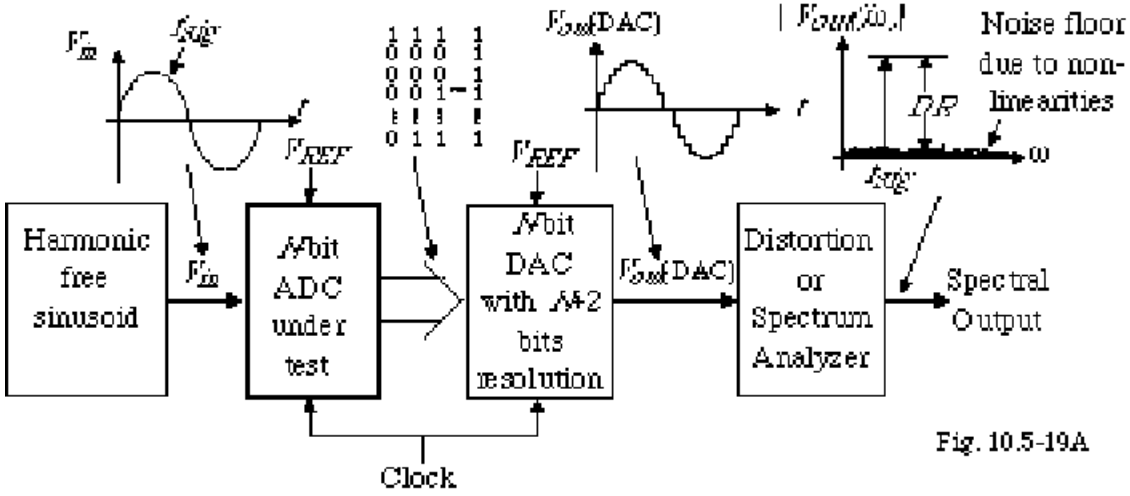


Fig. 10.5-19A

Comments:

- Input sinusoid must have less distortion that the required dynamic range
- DAC must have more accuracy than the ADC

FFT TEST FOR AN ADC

Test setup:

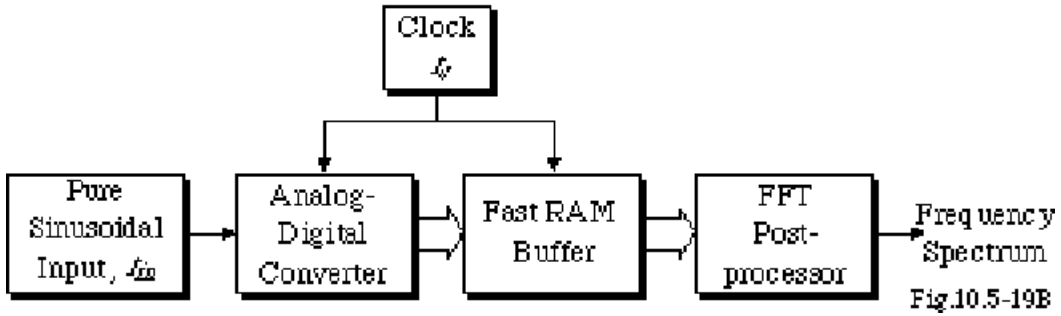


Fig.10.5-19B

Comments:

- Stores the digital output codes of the ADC in a RAM buffer
- After the measurement, a postprocessor uses the FFT to analyze the quantization noise and distortion components
- Need to use a window to eliminate measurement errors (Raised Cosine or 4-term Blackmann-Harris are often used)
- Requires a spectrally pure sinusoid

HISTOGRAM TEST FOR AN ADC

The number of occurances of each digital output code is plotted as a function of the digital output code.

Illustration:

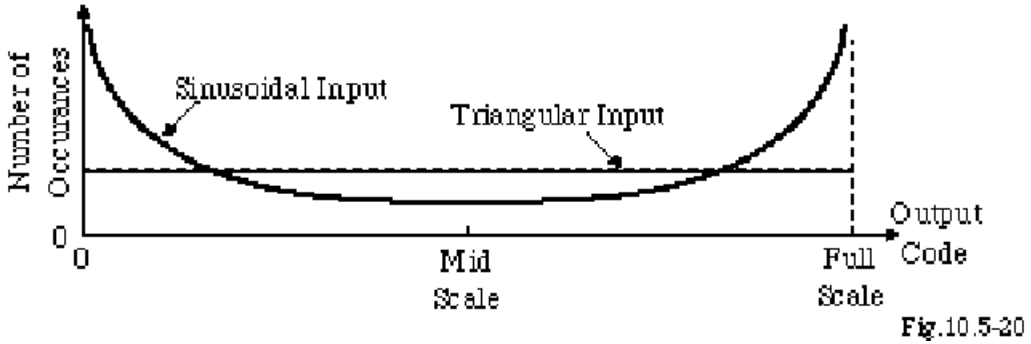


Fig.10.5-20

Comments:

- Emphasizes the time spent at a given level and can show *DNL* and missing codes
- *DNL*

$$DNL(i) = \frac{\text{Width of the bin as a fraction of full scale}}{\text{Ratio of the bin width to the ideal bin width}} - 1 = \frac{H(i)/N_t}{P(i)} - 1$$

where

$H(i)$ = number of counts in the ith bin

N_t = total number of samples

$P(i)$ = ratio of the bin width to the ideal bin width

- *INL* is found from the cumulative bin widths

COMPARISON OF THE TESTS FOR ANALOG-DIGITAL CONVERTERS

Other Tests

- Sinewave curve fitting (good for *ENOB*)
- Beat frequency test (good for a qualitative measure of dynamic performance)

Comparison

Test→ Error ↓	Histogram or Code Test	FFT Test	Sinewave Curve Fit Test	Beat Frequency Test
DNL	Yes (spikes)	Yes (Elevated noise floor)	Yes	Yes
Missing Codes	Yes (Bin counts with zero counts)	Yes (Elevated noise floor)	Yes	Yes
INL	Yes (Triangle input gives *INL* directly)	Yes (Harmonics in the baseband)	Yes	Yes
Aperature Uncertainty	No	Yes (Elevated noise floor)	Yes	No
Noise	No	Yes (Elevated noise floor)	Yes	No
Bandwidth Errors	No	No	No	Yes (Measures analog bandwidth)
Gain Errors	Yes (Peaks in distribution)	No	No	No
Offset Errors	Yes (Offset of distribution average)	No	No	No

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3.) J. Doernberg, H.S. Lee, and D.A. Hodges, "Full-Speed Testing of A/D Converters," *IEEE J. of Solid-State Circuits*, Vol. SC-19, No. 6, December 1984, pp. 820-827.

4.) "Dynamic performance testing of A to D converters," *Hewlett Packard Product Note 5180A-2*.

