Track & Hold: Architectures and Circuits
Sample-and-Hold Circuit

Block Diagram

Idealized Response

S/H circuit

S/H command

V_i → V_o

S/H: S H S H S H S H S H S

V_i

V_o

t
Performances of S & H

Realistic Transient Response:

Input & Output Voltage

$V_{in}$

$V_{out}$

Track Error

Pedestal

Voltage Drift

$C K$

$t_a$

$t_h$

$t$
S/H Circuit Waveforms and Performance Parameters

- **Droop**
- **V_i**
- **V_o**
- **Hold step**
- **Feedthrough**
- **Desired output**

- **t_{ac}**
- **t_{ap}**
- **t_s**
Design of Track and hold

Performance Definition

- **Acquisition Time**: the required time for the output transient after the sampling signal.

- **Hold Settling Time**: the time after the hold signal required for the output to settle within an acceptable error.

- **Pedestal Error**: due to the transition of sample to hold mode.

- **Voltage Drift**: the rate of discharge of the sampling capacitor during the hold mode.

- **Dynamic Range**: the ratio of the maximum and minimum input level, which can be sampled with a given resolution.
Performance Definition

- **Nonlinearity Error**: the maximum deviation of the $V_{\text{out}}/V_{\text{in}}$ characteristic from the straight line passed through the end points.

- **Gain Error**: the deviation of the slope of the straight line from unity.

Gain Error $= 1 - G$

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Track and hold

Performance Definition

- **Hold Mode Feedthrough**: the percentage of the input signal that appears at the output during the hold mode.

![Diagram of a track and hold circuit with parasitic capacitors](image-url)
Performance Definition

- **Aperture Error**: the random variation of the turn off time of the switch results in an uncertain sampling time.

**Maximum Allowable Aperture Error for 1/2 LSB**:

\[
\Delta t_{\text{max}} = \frac{1}{\pi f_{\text{in}} 2^{N+1}}
\]

Ideal sampling point
• Signal-to-Noise Ratio (SNR): the ratio of the signal power to the noise power at the output. The sources of noise are the input and output buffer, switch, and clock jitter.

• Signal to Noise + Distortion Ratio (SNDR): the ratio of signal power to the total noise and harmonic power at the output. The source of harmonics are the nonlinearity of the buffers and the switch.
Sample-and-Hold Basic Architectures

Fig. 1 An open-loop track and hold realized using MOS technology.

Fig. 2 An open-loop track and hold realized using a CMOS transmission gate.

Fig. 3 An open-loop track and hold realized using an n-channel switch along with a dummy switch for clock-feedthrough cancellation.

Analysis

\[ \Delta Q_{C_{hld}} = \frac{Q_{CH}}{2} = \frac{C_{OX}WLV_{eff-1}}{2} \]

where \( V_{eff-1} \) is given by

\[ V_{eff-1} = V_{GS1} - V_{in} = V_{DD} - V_{in} - V_{in} \]

\[ \Delta V' = \frac{\Delta Q_{C_{hld}}}{C_{hld}} = -\frac{C_{OX}WLV_{eff-1}}{2C_{hld}} = -\frac{C_{OX}WL(V_{DD} - V_{in} - V_{in})}{2C_{hld}} \]

\[ \Delta V' \approx -\frac{C_{OX}WL_{OV}(V_{DD} - V_{SS})}{C_{hld}} \]

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Input and Output Buffer:

The capacitor voltage during the hold mode can be affected by the current drawn by the following circuit. Therefore, the output voltage is buffered.
Unity Gain Buffer Circuit: BJT and CMOS implementations

Bipolar Technology

CMOS Technology

\[ V_{in} \rightarrow Q_1 \rightarrow Q_2 \rightarrow V_{out} \]

\[ V_{cc} \]

\[ R_c \]

\[ Q_3 \]

\[ I_{EE} \]

\[ I_F \]

\[ V_{in} \rightarrow M_1 \rightarrow V_{out} \]

\[ V_{DD} \]

\[ M_3 \]

\[ M_4 \]

\[ I_{SS} \]

\[ I_F \]
Track & Hold (T&H) Circuit

Simple Closed-Loop Architecture:

During the sampling time, the drain and source voltage of MOS switch are closed to ground. Thus the charge injection and clock feedthrough introduce an offset voltage at the output and is independent of the input voltage.

Disadvantage: Stability problems and low speed.
**T&H Circuit: Closed-Loop Architecture**

**Offset Voltage Cancellation:**

The charge injection and clock feedthrough can be cancel out by applying a replica of the offset voltage to the positive terminal of the second amplifier (common-mode voltage).
T&H Circuit: Switched Capacitor

Switched-Capacitor Architecture:

This architecture consists of sampling capacitor $C_S$, amplifier $G_m$, and MOS switches.

\[ \text{Hold Mode (CK}=0) \]

\[ \text{Track Mode (CK}=1) \]
Evolution of S/H Architectures

Fig A. Closed-loop sample-and-hold architecture.

Fig B. Including an opamp in a feedback loop of a sample and hold to increase the input impedance.

Fig C. Adding on additional switch to the S/H of Fig B to minimize slewing time.

Fig D. An improved configuration for an S/H as compared to that of Fig C.
Design of Track and hold

**T&H Circuit: Current-Mode**

**Current-Mode Architecture:**

Advantages: high-speed (over 100MHz) and low voltage (<1.2). The speed depends on the time constant given by:

\[ \tau = \frac{C_S}{g_{m1}} \]

\[ C_S = \frac{2}{3} C_{ox} (1 + A) W_1 \cdot L_1 \]

\[ g_{m1} = \mu C_{ox} \frac{W}{L} (V_{GS} - V_{Tn}) \]
Two Op Amps S/H Circuit

A1

A2

D1

D2

SW

R_F

C_H

V_i

V_o

S/H

Switch

driver
A 5 MHz track-and-hold circuit, using discrete components, with charge compensation to minimize the hold step.
Fig. The clock waveforms for $V_{in}$ and $\phi_{clk}$ used to illustrate how a finite slope for the sampling clock introduces sampling-time jitter.

Fig. Closed-loop sample-and-hold architecture with pedestal cancellation.
The open-loop architecture with Miller capacitance employs two different values of capacitance in the acquisition and hold modes to achieve high speed and small pedestal error. This is accomplished using a Miller amplifier that multiplies the effective value of the sampling capacitor by a large number when the SHA enters the hold mode.
Switched-Capacitor S/H Implementations

A switched-capacitor sample and hold and low-pass filter.

A switched-capacitor S/H.
MULTIPLEXED-INPUT ARCHITECTURES

Multiplexed-input architecture. (a) Basic (single-ended) circuit; (b) equivalent circuit in the hold mode.

Equivalent circuits of dual-loop multiplexed-input architecture. (b) Acquisition mode; (c) hold mode.

Fig. 15(a) Dual-loop multiplexed architecture.
T&H Circuit: Current-Mode

Closed-Loop Current-Mode Architecture:

This architecture needs stability and speed considerations. The distortion of $G_{m2}$ affects directly the output current [21].
T&H Circuit: Example

BiCMOS Track & Hold Amplifier (12-Bit & 50Msps):

This circuit consists of input buffer, hold section, and output buffer [3].

\[ C_S = 3 \text{pF} \]

\( C_{FF} \) is a feedforward compensation capacitor for the charge injection of \( Q_4 \).
Fig. 16 Recycling architecture.

Fig. 17 Equivalent circuits of recycling architecture.
(a) Sampling mode; (b) hold mode.
Integrating Amplifier S/H Circuit

Diagram of an integrating amplifier S/H circuit with components labeled and connections made clear.
Improved S/H Circuit

Buffer

S/H

SW driver

SW_1

SW_2

SW_3

R

C_H

V_i

+V

V_o

-
Sample and Hold based on a Switched Op Amp

Charge injection and clock feedthrough mechanism

\[ Q_{ch} = -WLC_{ox} (V_{GS} - V_T) \]

\[ \Delta V' = \frac{k \cdot Q_{ch}}{C_h} = -\frac{kWLC_{ox} (V_{GS} - V_T)}{C_h} \]

\[ \Delta V'' = -\frac{(V_{DD} - V_{SS})C_{para}}{C_{para} + C_h} \]
Channel charge in (top) triode and (bottom) saturation
Switched-Op-Amp-Based S/H Circuit

Simplified model of the pseudo-differential SOP-based S/H
Folded cascode switched op-amp in the unity-gain feedback configuration

\[ V_{\text{Nerr}} = -\frac{C_{\text{Npara}}}{C_h + C_{\text{Npara}}} V_{N_{\text{GS}}} \]

\[ V_{\text{Perr}} = -\frac{C_{\text{Ppara}}}{C_h + C_{\text{Ppara}}} V_{P_{\text{GS}}} \]
Simulation results for a complete cycle of sampled-and-held waveform

Simulation results of the spectrum of the sampled-and-held waveform
References