### Types of D/A Converters

<table>
<thead>
<tr>
<th>DAC Type</th>
<th>Advantage</th>
<th>Disadvantage</th>
</tr>
</thead>
<tbody>
<tr>
<td>Current Scaling</td>
<td>Fast, insensitive to switch parasitics</td>
<td>Large element spread, nonmonotonic</td>
</tr>
<tr>
<td>Voltage Scaling</td>
<td>Monotonic, equal resistors</td>
<td>Large area, sensitive to parasitic capacitance</td>
</tr>
<tr>
<td>Charge Scaling</td>
<td>Fast, good accuracy</td>
<td>Large element spread, nonmonotonic</td>
</tr>
</tbody>
</table>
Current Scaling D/As

The output voltage can be expressed as

\[ V_{\text{out}} = R_f (I_1 + I_2 + I_3 + \ldots + I_N) \]

where the currents \( I_1, I_2, I_3, \ldots \) are binary weighted currents.
D/As built from R-2R Ladders

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\[ V_{out} = R_f(I_1 + I_2 + I_3 + \ldots + I_N) \]

where the currents \( I_1, I_2, I_3, \ldots \) are binary weighted currents.

"The resistance seen to the right of any of the vertical 2R resistors is 2R."

Not monotonic
Current Scaling D/As

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\[ V_{\text{out}} = R_f(I_1 + I_2 + I_3 + \ldots + I_N) \]

where the currents \( I_1, I_2, I_3, \ldots \) are binary weighted currents.

Fast (no moving nodes) and not monotonic (mismatch)
Voltage Scaling D/As

- Guaranteed monotonic,
- Compatible with CMOS technology,
- Large area if \( N \) is large,
- Sensitive to parasitics,
- Requires a buffer,
- Large current can flow through the resistor string.
Charge Based D/A Converters

- No moving nodes
  - insensitive to parasitics
    (parasitic-insensitive switched capacitor circuitry)
  - fast

- Can not eliminate charge feedthrough

Based on capacitor matching (not monotonic)
Charge feedthrough and parasitic issues
Improving D/A Performance

Divide the total resolution $N$ into $k$ smaller sub-DACs.

- Smaller total area.
- More resolution (reduced largest to smallest component spread)

So how do we do this?

- Combination of similarly scaled subDACs
  - Divider approach (scale the analog output of the subDACs)
  - Subranging approach (scale the reference voltage of the subDACs)

- Combination of differently scaled subDACs
Subranging Converters

**m-MSB** bits → m-bit MSB DAC → \( V_{REF} \) → \( v_{OUT} \)

**k-LSB** bits → k-bit LSB DAC

**Current DAC**

\[ i_1 \sim \frac{b_8}{16} \]
\[ i_2 \sim \frac{b_7}{8} \]
\[ i_d = \frac{b_6}{4} \]

\[ i_0 = \frac{R}{i_d} \]

**Charge DAC**

\[ C_s = \frac{2C}{15} \]
\[ C + \frac{7C}{8} = \frac{15C}{8} \]
D/A Based on Two Charge Amps

- MSB subDAC is not dependent upon the accuracy of the scaling factor for the LSB subDAC.
- Insensitive to parasitics, fast
- Limited to op amp dynamics

Fig. 10.3-6
Combining Unique SubDACs

MSB: Charge Scaling  
(high # of bits)  
LSB: Voltage Scaling  
(monotonic)

LSB: Charge Scaling  
(high # of bits)  
MSB: Voltage Scaling  
(monotonic)
## Summary of D/A Converters

<table>
<thead>
<tr>
<th>DAC</th>
<th>Figure</th>
<th>Primary Advantage</th>
<th>Primary Disadvantage</th>
</tr>
</thead>
<tbody>
<tr>
<td>Current-scaling, binary weighted resistors</td>
<td>10.2-3</td>
<td>Fast, insensitive to parasitic capacitance</td>
<td>Large element spread, nonmonotonic</td>
</tr>
<tr>
<td>Current-scaling, R-2R ladder</td>
<td>10.2-4</td>
<td>Small element spread, increased accuracy</td>
<td>Nonmonotonic, limited to resistor accuracy</td>
</tr>
<tr>
<td>Current-scaling, active devices</td>
<td>10.2-5</td>
<td>Fast, insensitive to switch parasitics</td>
<td>Large element spread, large area</td>
</tr>
<tr>
<td>Voltage-scaling</td>
<td>10.2-7</td>
<td>Monotonic, equal resistors</td>
<td>Large area, sensitive to parasitic capacitance</td>
</tr>
<tr>
<td>Charge-scaling, binary weighted capacitors</td>
<td>10.2-10</td>
<td>Best accuracy</td>
<td>Large area, sensitive to parasitic capacitance</td>
</tr>
<tr>
<td>Binary weighted, charge amplifier</td>
<td>10.2-12</td>
<td>Best accuracy, fast</td>
<td>Large element spread, large area</td>
</tr>
<tr>
<td>Current-scaling subDACs using current division</td>
<td>10.3-3</td>
<td>Minimizes area, reduces element spread which enhances accuracy</td>
<td>Sensitive to parasitic capacitance, divider must have ±0.5LSB accuracy</td>
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<tr>
<td>Charge-scaling subDACs using charge division</td>
<td>10.3-4</td>
<td>Minimizes area, reduces element spread which enhances accuracy</td>
<td>Sensitive to parasitic capacitance, slower, divider must have ±0.5LSB accuracy</td>
</tr>
<tr>
<td>Binary weighted charge amplifier subDACs</td>
<td>10.3-6</td>
<td>Fast, minimizes area, reduces element spread which enhances accuracy</td>
<td>Requires more op amps, divider must have ±0.5LSB accuracy</td>
</tr>
<tr>
<td>Voltage-scaling (MSBs), charge-scaling (LSBs)</td>
<td>10.3-7</td>
<td>Monotonic in MSBs, minimum area, reduced element spread</td>
<td>Must trim or calibrate resistors for absolute accuracy</td>
</tr>
<tr>
<td>Charge-scaling (MSBs), voltage-scaling (LSBs)</td>
<td>10.3-8</td>
<td>Monotonic in LSBs, minimum area, reduced element spread</td>
<td>Must trim or calibrate resistors for absolute accuracy</td>
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<td>Serial, charge redistribution</td>
<td>10.4-1</td>
<td>Simple, minimum area</td>
<td>Slow, requires complex external circuits</td>
</tr>
<tr>
<td>Pipeline, algorithmic</td>
<td>10.4-3</td>
<td>Repeated blocks, output at each clock after (N) clocks</td>
<td>Large area for large number of bits</td>
</tr>
<tr>
<td>Serial, iterative algorithmic</td>
<td>10.4-4</td>
<td>Simple, one precise set of components</td>
<td>Slow, requires additional logic circuitry</td>
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