What are Comparators?

A 1-Bit Analog-Digital Converter

or

A 1-Bit Quantizer

Inputs Analog Signals and Outputs a Digital Signal

Noninverting Comparator

Inverting Comparator
Static Characteristics

Ideal Comparator

Real Comparator
Definitions

$V_{OH} =$ the high output of the comparator
$V_{OL} =$ the low level output of the comparator

$\text{Gain} = A_v = \lim_{\Delta V \to 0} \frac{V_{OH} - V_{OL}}{\Delta V}$ where $\Delta V$ is the input voltage change

$V_{IH} =$ smallest input voltage at which the output voltage is $V_{OH}$
$V_{IL} =$ largest input voltage at which the output voltage is $V_{OL}$

$V_{OS} =$ the input voltage necessary to make the output equal $\frac{V_{OH} + V_{OL}}{2}$ when $v_P = v_N$. 
Comparator Macromodel

\[ f_1(v_P' - v_N') = \begin{cases} 
V_{OH} \text{ for } (v_P' - v_N') > V_{IH} \\
A_v(v_P' - v_N') \text{ for } V_{IL} < (v_P' - v_N') < V_{IH} \\
V_{OL} \text{ for } (v_P' - v_N') < V_{IL}
\end{cases} \]
Propagation Delay

Propagation Delay = (Rise Time + Fall Time)/2
Propagation Delay

**Frequency Domain**

\[ A_v(s) = \frac{A_v(0)}{s/\omega_c + 1} = \frac{A_v(0)}{s\tau_c + 1} \]

\[ A_v(0) = \text{dc voltage gain of the comparator} \]

\[ \omega_c = \frac{1}{\tau_c} = \text{-3dB frequency of the comparator or the magnitude of the pole} \]

**Time Domain**

\[ v_o(t) = A_v(0) \left[ 1 - e^{-t/\tau_c} \right] V_{in} \]

\[ V_{in} = \text{the magnitude of the step input.} \]
Propagation Delay

\[
\frac{V_{OH} - V_{OL}}{2} = A_v(0) \left[ 1 - e^{-t_p/\tau_c} \right] V_{in} \quad \rightarrow \quad t_p = \tau_c \ln \left[ \frac{1}{1 - \frac{V_{OH} - V_{OL}}{2A_v(0)V_{in}}} \right]
\]

Define

\[
V_{in(\text{min})} = \frac{V_{OH} - V_{OL}}{A_v(0)} \quad k = \frac{V_{in}}{V_{in(\text{min})}}
\]

Propagation Delay

\[
t_p = \tau_c \ln \left[ \frac{2k}{2k-1} \right]
\]
Slew Rate

For large overdrives, the comparator is limited by Slew Rate

Slew Rate

- Analysis similar to an operational amplifier
- Depends on current charging/discharging a capacitor

\[
\text{Slew Rate} = \frac{dv}{dt} = \frac{I}{C}
\]

Propagation Delay when slew rate limited

\[
t_p = \Delta T = \frac{\Delta V}{SR} = \frac{V_{OH} - V_{OL}}{2 \cdot SR}
\]
Comparator Circuits

**Push-Pull Comparator**

![Push-Pull Comparator Diagram]

- better slew rate performance

**2-stage Comparator**

![2-stage Comparator Diagram]

- Does not require compensation. Why?

**Higher Gain Comparators**

![Higher Gain Comparators Diagram]

- M8-M11 form CMOS Inverters
Performance Metrics

Maximum Output Voltage

\[ V_{OH} = V_{DD} - (V_{DD} - V_{G6}(\text{min}) - |V_{TP}|) \left[ 1 - \sqrt{1 - \frac{8I_7}{\beta_6(V_{DD} - V_{G6}(\text{min}) - |V_{TP}|)^2}} \right] \]

Minimum Output Voltage

\[ V_{OL} = \tilde{V}_{SS} \]

Open Loop Gain

\[ A_V(0) = \left( \frac{g_{m1}}{g_{ds2} + g_{ds4}} \right) \left( \frac{g_{m6}}{g_{ds6} + g_{ds7}} \right) \]

Frequency Response

\[ A_V(s) = \frac{A_V(0)}{\left( \frac{s}{p_1 - 1} \right) \left( \frac{s}{p_2 - 1} \right)} \]

\[ p_1 = \frac{-(g_{ds2} + g_{ds4})}{C_I} \quad p_2 = \frac{-(g_{ds6} + g_{ds7})}{C_{II}} \]
Performance Metrics

Propagation Delay

\[ v_{out}(t) = A_v(0)V_{in}\left[1 + \frac{p_2e^{tp_1}}{p_1-p_2} - \frac{p_1e^{tp_2}}{p_1-p_2}\right] \]

Simplifying

\[ v_{out}(t_n) = A_v(0)V_{in}\left[1 - \frac{m}{m-1}e^{-t_n} + \frac{1}{m-1}e^{-mt_n}\right] \]

\[ m = \frac{p_2}{p_1} \neq 1 \quad \text{and} \quad t_n = -tp_1 \]

Linear Analysis

\[ t_{pn} \approx \sqrt{\frac{V_{OH} + V_{OL}}{mA_v(0)V_{in}}} = \sqrt{\frac{V_{in}(\text{min})}{mV_{in}}} = \frac{1}{\sqrt{mk}} \]

Comparator slews if a large input overdrive is applied
Autozeroing

Key Issues

- Stability during the autozero cycle
- Charge Injection during switching
Autozeroing

Note: Clocks need to be non-overlapping
Influence of Noise

Noise can result in false switching in the comparator
Hysteresis

- The trip point is altered as a function of the input
- Can be achieved externally or internally
Hysteresis – External Feedback

**Upper Trip Point**

\[ V_{REF} = \left( \frac{R_1}{R_1+R_2} \right) V_{OL} + \left( \frac{R_2}{R_1+R_2} \right) V_{TRP^+} \]

\[ V_{TRP^+} = \left( \frac{R_1+R_2}{R_2} \right) V_{REF} - \frac{R_1}{R_2} V_{OL} \]

**Lower Trip Point**

\[ V_{REF} = \left( \frac{R_1}{R_1+R_2} \right) V_{OH} + \left( \frac{R_2}{R_1+R_2} \right) V_{TRP^-} \]

\[ V_{TRP^-} = \left( \frac{R_1+R_2}{R_2} \right) V_{REF} - \frac{R_1}{R_2} V_{OH} \]
Hysteresis – External Feedback

Upper Trip Point

\[ v_{IN} = V_{TRP^+} = \left( \frac{R_1}{R_1 + R_2} \right) V_{OH} + \left( \frac{R_2}{R_1 + R_2} \right) V_{REF} \]

Lower Trip Point

\[ v_{IN} = V_{TRP^-} = \left( \frac{R_1}{R_1 + R_2} \right) V_{OL} + \left( \frac{R_2}{R_1 + R_2} \right) V_{REF} \]
Hysteresis – Internal Feedback
Hysteresis – Internal Feedback

Trip point occurs when current through M2 equals M6

Any further increase will turn on M4/M7 setting the positive feedback in motion
Hysteresis – Internal Feedback

Trip point occurs when current through M1 equals M7

Any further increase will turn on M3/M6 setting the positive feedback in motion
Schmitt Trigger

Assume $V_{in}$ low and $V_{out}$ high

Transistors M1/M2/M6 are off
Transistors M3/M4/M5 are on

As $V_{in}$ is increased M1 turns on
$I(M1)$ initially supplied by M3

When M2 turns on it decreases $V_{out}$
that turns off M3 and further turns on M2 $\rightarrow$ Positive feedback

Trip point occurs at the point of turn on of M2
Switch Capacitor Comparator

$\phi_1$ autozeros the comparator and $\phi_2$ performs the comparison
Regenerative Comparators

Use positive feedback to achieve signal comparison

The inputs are initially applied to the outputs of the latch.

\[ V_{o1}' = \text{initial input applied to } v_{o1} \]
\[ V_{o2}' = \text{initial input applied to } v_{o2} \]
Regenerative Comparators

\[ g_{m1}V_{o2} + G_1V_{o1} + sC_1 \left( V_{o1} - \frac{V_{o1}'}{s} \right) = g_{m1}V_{o2} + G_1V_{o1} + sC_1V_{o1} - C_1V_{o1}' = 0 \]

\[ g_{m2}V_{o1} + G_2V_{o2} + sC_2 \left( V_{o2} - \frac{V_{o2}'}{s} \right) = g_{m2}V_{o1} + G_2V_{o2} + sC_2V_{o2} - C_2V_{o2}' = 0 \]

Defining the output, \( \Delta V_o \), and input, \( \Delta V_i \), as

\[ \Delta V_o = V_{o2} - V_{o1} \quad \text{and} \quad \Delta V_i = V_{o2}' - V_{o1}' \]
Regenerative Comparators

Solving

\[ \Delta V_o = \frac{\tau \Delta V_i}{s\tau + (1 - g_m R)} = \frac{\tau \Delta V_i}{s\tau} \frac{1}{1 - g_m R + 1} = \frac{\tau' \Delta V_i}{s\tau' + 1} \]

\[ \tau' = \frac{\tau}{1 - g_m R} \]

Taking Inverse LT

\[ \Delta V_{out}(t) = e^{t/\tau_L} \Delta V_i \]

\[ \tau_L = |\tau'| \approx \frac{\tau}{g_m R} \]

The response is rapid towards the end
Comparator using a Latch

M1/M2 act as resistors degenerating M3/M4
High Speed Comparators

- Amplifiers have a step response with a negative argument in the exponent
- Latches have a step response with a positive argument in the exponent

Use a pre-amp to quickly build up the signal and pass it on to a latch!

Judicious use of both amplifier and latch to achieve high speeds
High Speed Comparators

Cascade of stages

Initial stages are responsible for signal buildup

Latter stages make a quick transition to binary levels
Summary

 Comparator Types

- High Gain Open Loop Comparators
- Improvements include autozeroing/hysteresis
  - Charge Injection Key Limitation
- Discrete Time Comparators
- Regenerative Comparators
- High Speed Comparators
  - Pre-amp (High GB) + Latch + Output stage