Sample and Hold Elements

Input ➔ Sample and Hold Block (S/H) ➔ Output

Clock
Sample and Hold Elements

Sample and Hold Block (S/H)

Input → Sample and Hold Block (S/H) → Output

Clock

Amplitude

Clock

Input

(Sample)

(Hold)

(Hold)

Time
Sample and Hold Elements

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Clock

Amplitude

Clock

Input

Output

Time
Sample and Hold Elements

Sample and Hold Block (S/H)

Input → Sample and Hold Block (S/H) → Output

Clock

Amplitude

Clock

Input

Output

Valid Output

Time
Sample and Hold Elements

Sample and Hold Block (S/H)

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Clock

Amplitude

Settling time \((t_s)\) = time required to settle to the final held voltage to within an accuracy tolerance

Valid Output

Time

\(t_s\)

Input

Output

(Hold)

(Sample)

(Hold)
Sample and Hold Elements

Sample and Hold Block (S/H)

Input → Sample and Hold Block (S/H) → Output

Clock

Valid Output

Acquisition time \( t_a \) =

time required to acquire the analog voltage

Amplitude

Clock

Input

Output

\( t_a \)

\( t_s \)

Time
Sample and Hold Elements

Sample and Hold Block (S/H)

Input $\rightarrow$ Sample and Hold Block (S/H) $\rightarrow$ Output

Clock

Amplitude

Clock

Input $\rightarrow$ Output

Valid Output

Time

$T_{\text{sample}} = t_a + t_s$

$F_{\text{sample}}(\text{max}) < \frac{1}{T_{\text{sample}}}$
Sample and Hold Elements

Sample and Hold Block (S/H)

- **Aperture time** = the time required for the sampling switch to open after the S/H command is initiated
- **Aperture jitter** = variation in the aperture time due to clock variations and noise

Clock

Amplitude

Input

Output

Time

\[ t_a \]

\[ t_s \]
Basic Sample and Hold Element

\[ V_{\text{in}}(t) \quad \text{CK} \quad V_{\text{out}}(t) \quad C_1 \quad \text{GND} \]
Basic Sample and Hold Element
Basic Sample and Hold Element

\[
\begin{align*}
&CK \quad V_{in}(t) \quad V_{out}(t) \\
&C_1 \quad GND
\end{align*}
\]

\[
\begin{align*}
&\text{CK} = 1 \ (Vdd) \\
&V_{in}(t) \quad 1 \quad V_{out}(t) \\
&C_1 \quad GND
\end{align*}
\]
Basic Sample and Hold Element

\[ \text{CK} = 1 \ (Vdd) \]
Basic Sample and Hold Element

\[ \text{CK} = 1 \text{ (Vdd)} \]

\[ \text{CK} = 0 \text{ (Vdd)} \]
Basic Sample and Hold Element

CK = 1 (Vdd)

CK = 0 (Vdd)
Acquisition and Hold Time

**Acquisition Time**

- **CK**
- \( V_{\text{in}}(t) \) — \( V_{\text{out}}(t) \)
- \( C_1 \)
- **GND**

\[ V_{\text{in}}(t) \quad \text{R}_{\text{on}} \quad V_{\text{out}}(t) \quad \text{GND} \]

\( V_{\text{in}}(t) \) through \( R_{\text{on}} \) to \( V_{\text{out}}(t) \)

\( V_{\text{in}}(t) \) to \( C_1 \) with \( \text{GND} \)

but \( R_{\text{on}} \) is not a constant....

**Hold Time**

- **0V**
- \( V_{\text{in}}(t) \)
- \( I_1 \)
- \( I_2 \)
- **GND**
- \( V_{\text{out}}(t) \)

\[ V_{\text{in}}(t) \quad \downarrow \quad I_1 \quad I_2 \quad \text{GND} \quad \text{GND} \quad V_{\text{out}}(t) \]

\( I_2(t) \): Leakage through the reversed-biased pn junction
Typically 1fA to 100fA (dark)

\( I_1(t) \): Leakage through the MOS transistor
Can be negligible with correct biasing

<table>
<thead>
<tr>
<th>( C_2 )</th>
<th>Hold time (1mV drop) with ( I_2(t) = 10fA )</th>
</tr>
</thead>
<tbody>
<tr>
<td>10pF</td>
<td>1s</td>
</tr>
<tr>
<td>1pF</td>
<td>100ms</td>
</tr>
<tr>
<td>100fF</td>
<td>10ms</td>
</tr>
<tr>
<td>10fF</td>
<td>1ms</td>
</tr>
</tbody>
</table>
Basic S/H elements

Sample and Hold Block (S/H)

Input → Sample and Hold Block (S/H) → Output

Clock
Basic S/H elements

Sample and Hold Block (S/H)

Input → Sample and Hold Block (S/H) → Output

Clock

$V_{in}(t)$ → $V_{out}(t)$

$C_1$

GND
Basic S/H elements

Would use a buffer to drive loads that are not purely capacitive
S/H elements

Sample and Hold Block (S/H)

Clock

Input

Output

$V_{in}(t)$

$V_{out}[n]$

$\phi_1$ and $\phi_2$ are non-overlapping clocks

More accurate, but slower
Non-Overlapping Clocks

We will always be using non-overlapping clocks; therefore, we want a waveform like

We effectively have four phases.
Non-Overlapping Clocks

We will always be using non-overlapping clocks; therefore, we want a waveform like

\[ \phi_1 \quad \phi_2 \]

We effectively have four phases.

Would want \( t_d \) as small as possible for proper operation

We will also assume that the input is held constant through the entire \([n]^{th}\) cycle
Non-Overlapping Clocks

We will always be using non-overlapping clocks; therefore, we want a waveform like

\[ \phi_1 \quad \phi_2 \]

We effectively have four phases.

Would want \( t_d \) as small as possible for proper operation.

We will also assume that the input is held constant through the entire \([n]^{th}\) cycle.

Circuit to generate waveform

\[ \text{N-stages of delay (sets } t_d) \]

Clock in \( \phi_1 \quad \phi_2 \)
**S/H elements**

**Sample and Hold Block (S/H)**

**Input** → **Sample and Hold Block (S/H)** → **Output**

Clock

**Initial Phase** ($\phi_1, \phi_2 = 0$)

$V_{in}(t)$

$V_{out}[n-1]$
S/H elements

Phase I ($\phi_1 = 1, \phi_2 = 0$)
S/H elements

Phase II \((\phi_1, \phi_2 = 0)\)
S/H elements

Sample and Hold Block (S/H)

Input \rightarrow \text{Sample and Hold Block (S/H)} \rightarrow \text{Output}

Clock

\[ V_{\text{in}}(t) \]

are \( \sim V_{\text{in}}(t) \); therefore ready for the next phase
S/H elements

$V_{\text{out}}[n]$ and $\phi_2$ are non-overlapping clocks

$V_{\text{in}}(t)$

$\phi_1$ and $\phi_2$ are non-overlapping clocks