Measurement and Analysis of Charge Injection in MOS Analog Switches

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Abstract — **Charge injection in MOS switches has been analyzed. The analysis has been extended to the general case including signal-source resistance and capacitance. Universal plots of percentage channel charge injected are presented. Normalized variables are used to facilitate usage of the plots. The effects of gate voltage falling rate, signal-source level, substrate doping, substrate bias, switch dimensions, as well as the source and holding capacitances are all included in the plots. A small-geometry switch, slow switching rate, and small source resistance can reduce the charge injection effect. On-chip test circuitry with a unity-gain operational amplifier, which reduces the disturbance imposed by measurement equipment to a minimum, is found to be an excellent monitor of the switch charge injection. The theoretical results agree with the experimental data.**

I. Introduction

In A monolithic sample and hold, a signal is stored on a capacitor. The accuracy of sample-and-hold circuits is disturbed by charge injected when the sampling switch turns off. The majority of sample-and-hold circuits are implemented using MOS technologies because the high input impedance of MOS devices performs excellent holding function. When the switch connecting the signal-source node and the data-storage node is turned on, the sampling function is performed. When the switch is turned off, the data stored in the storage node will be held until the next operation step occurs. However, an MOS switch is not an ideal switch. A finite amount of mobile carriers are stored in the channel when an MOS transistor conducts. When the transistor turns off, the channel charge exits through the source, the drain, and the substrate electrodes. The charge transferred to the data node during the switch turning-off period superposes an error component to the sampled voltage. In addition to the charge from the intrinsic channel, the charge associated with the feedthrough effect of the gate-to-diffusion overlap capacitance also enlarges the error voltage after the switch turns off [1]. This charge injection problem was identified in the early stage of switched-capacitor circuit development. Various compensation schemes [2],[3] have been used to reduce the switch-induced error voltage. As the design of higher precision sample-and-hold circuits progresses, the need for effective test patterns to accurately monitor the switch charge injection becomes increasingly important. In 5-V technologies, the resolution in a 10-bit analog-to-digital (A/D) converter is 4.88 mV, while the resolution in a 16-bit A/D converter is only 76 μV. The error voltage caused by the switch charge injection is usually in the millivolt range. The fully differential circuit approach [3] cancels the switch charge injection to the first order. Precise characterization and detailed analysis of the switch charge injection is of prime interest in designing high-performance integrated circuits.

There have been some attempts to model the switch charge injection. MacQuigg [4] made a qualitative observation and did SPICE simulation on a simplified case. Sheu and Hu [1] developed an analytical model corresponding to infinite source capacitance. A two-transistor source follower was used by Wilson *et al.* [5] with an attempt to improve the measurement accuracy. In this paper, analysis on the general case of switch charge injection is described in Section II. Analytical models of special cases are also presented. A better test structure for monitoring switch charge injection is proposed in Section III. Experimental results are presented in Section IV. A conclusion is given in Section V.

II. Analysis

We assume that the charge pumping phenomenon due to the capture of channel charge by the interface traps is insignificant and all the channel charge exits through the source and drain electrodes when the transistor turns off. The turn-off of an MOS switch consists of two distinct phases. During the first phase, the gate voltage is higher than the transistor threshold voltage. There is a conduction channel that extends from the source to the drain of the transistor. As the gate voltage decreases, mobile carriers exit through both the drain end and the source end and the channel conduction decreases. During the second phase, the gate voltage is below the transistor threshold voltage and the conduction channel does not exist any more. The coupling between the gate and the data-holding node is merely through the gate-to-diffusion overlap capacitance. In our analysis, attention is focused on the switch charge

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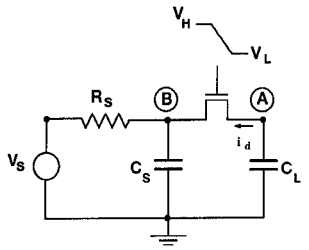

Fig. 1. Circuit for analysis of switch charge injection.

injection due to the first phase of the switch turn-off. The circuit schematic corresponding to the general case of switch charge injection is shown in Fig. 1. Capacitance C_L is the lumped capacitance at the data-holding node. Resistance R_S could be the output resistance of an operational amplifier, while capacitance C_S could be the lumped capacitance associated with the amplifier output node.

Let C_G represent the total gate capacitance, including both the channel capacitance and gate-to-source/gate-to-drain overlap capacitances:

$$C_G = WLC_0 + C_{0vs} + C_{0vd}. \tag{1}$$

By following the derivation presented in [1], Kirchkoff's current law at node A and node B requires

$$C_L \frac{dv_L}{dt} = -i_d + \frac{C_G}{2}\frac{d(V_G - v_L)}{dt} \tag{2}$$

and

$$\frac{v_S}{R_S} + C_S\frac{dv_S}{dt} = i_d + \frac{C_G}{2}\frac{d(V_G - v_S)}{dt} \tag{3}$$

where v_L and v_S are the error voltages at the data-holding node and the signal-source node, respectively. Gate voltage is assumed to decrease linearly with time from the ON value V_H:

$$V_G = V_H - Ut \tag{4}$$

where U is the falling rate. When the transistor is operated in the strong inversion region

$$i_d = \beta(V_{HT} - U)(v_L - v_S) \tag{5}$$

where

$$\beta = \mu C_0 \frac{W}{L}$$

and

$$V_{HT} = V_H - V_S - V_{TE}. \tag{6}$$

Here V_{TE} is the transistor effective threshold voltage including the body effect. For small-geometry transistors, narrow- and short-channel effects should be considered in determining the V_{TE} value. Under the condition $|dV_G/dt| \gg |dv_L/dt|$ and $|dv_S/dt|$, (2) and (3) simplify to

$$C_L\frac{dv_L}{dt} = -\beta(V_{HT} - Ut)(v_L - v_S) - \frac{C_G}{2}U \tag{7}$$

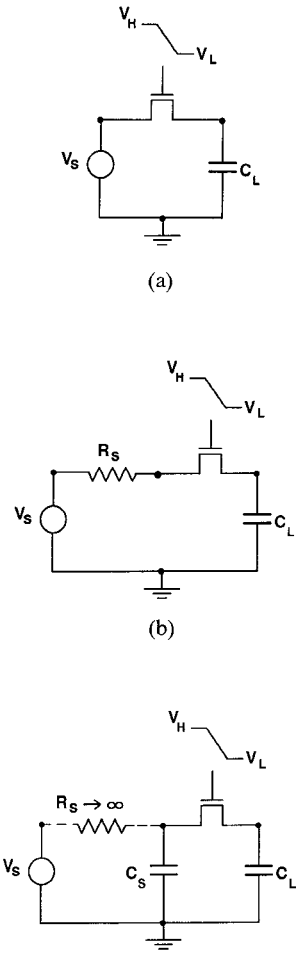

Fig. 2. Special cases of switch charge injection. (a) No source resistance and capacitance. (b) No source capacitance. (c) Infinitely large source resistance.

and

$$\frac{v_S}{R_S} + C_S\frac{dv_S}{dt} = \beta(V_{HT} - Ut)(v_L - v_S) + \frac{C_G}{2}U. \tag{8}$$

No closed-form solution to this set of equations can be found. Numerical integration can be employed to find the results. Analytical solutions to special cases are given below.

Fig. 2(a) shows the case with only a voltage source at the signal-source node. Since $C_S \gg C_L$, v_S can be approximated as zero and the governing equation reduces to

$$C_L\frac{dv_L}{dt} = -\beta(V_{HT} - Ut)v_L - \frac{C_G}{2}U. \tag{9}$$

When the gate voltage reaches the threshold condition, the error voltage at the data-holding node is

$$v_L = -\sqrt{\frac{\pi UC_L}{2\beta}}\left(\frac{C_G}{2C_L}\right)\operatorname{erf}\left(\sqrt{\frac{\beta}{2UC_L}}V_{HT}\right). \tag{10}$$

Another special case is when the source capacitance is negligibly small, as is shown in Fig. 2(b). The governing

equations reduce to

$$C_L\frac{dv_L}{dt} = -\beta(V_{HT}-Ut)(v_L-v_S)-\frac{C_G}{2}U \quad (11)$$

and

$$\frac{v_S}{R_S} = \beta(V_{HT}-Ut)(v_L-v_S)+\frac{C_G}{2}U. \quad (12)$$

When the gate voltage reaches the threshold condition, (5) breaks down and the error voltage at the data-holding node is

$$v_L = -\frac{UC_G}{2C_L}\exp\left(-\frac{V_{HT}}{UC_LR_S}\right)\cdot\int_0^{V_{HT}/U}[\beta R_S(V_{HT}-U\xi)+1]^{1/C_L\beta R_S^2U}\cdot\exp\left(\frac{\xi}{C_LR_S}\right)\left(2-\frac{1}{1+\beta R_S(V_{HT}-U\xi)}\right)d\xi. \quad (13)$$

If the time constant R_SC_S is much larger than the switch turn-off time, then the channel charge will be shared between C_S and C_L, as is shown in Fig. 2(c). For the case of a symmetrical transistor and $C_S = C_L$, half of the channel charge will be deposited to each capacitor. Otherwise the following equations can be used to find out the results:

$$C_L\frac{dv_L}{dt} = -\beta(V_{HT}-Ut)(v_L-v_S)-\frac{C_G}{2}U \quad (14)$$

and

$$C_S\frac{dv_S}{dt} = \beta(V_{HT}-Ut)(v_L-v_S)+\frac{C_G}{2}U. \quad (15)$$

We now multiply (15) by the ratio C_L/C_S, and then subtract the result from (14), to obtain

$$C_L\frac{d(v_L-v_S)}{dt} = -\beta(V_{HT}-Ut)\left[1+\frac{C_L}{C_S}\right](v_L-v_S) - \frac{UC_G}{2}\left(1-\frac{C_L}{C_S}\right). \quad (16)$$

When the gate voltage reaches the threshold condition, the amount of voltage difference between the data-holding node and the signal-source node is

$$v_L - v_S = -\sqrt{\frac{\pi UC_L}{2\beta(1+C_L/C_S)}}\left(\frac{C_G(1-C_L/C_S)}{2C_L}\right)\cdot\operatorname{erf}\left(\sqrt{\frac{\beta(1+C_L/C_S)}{2UC_L}}V_{HT}\right). \quad (17)$$

Fig. 3 shows the calculated percentage of channel charge injected to the data-holding node when the source resistance is infinitely large. Similar plots were obtained by numerical integration after some special transformation of the problem [6]. The dimensionless quantity $V_{HT}\sqrt{\beta/UC_L}$ has been identified as the driving force of the switch charge injection effect. It has the same functional dependence as the argument of the error function in (10). A family of curves corresponding to various C_S/C_L ratios have been plotted. When the switch turns off, the channel charge exits to the signal-source node and the data-holding node under capacitive coupling and resistive conduction. In the fast switching-off conditions, the transistor conduction channel disappears very quickly. There is not enough time for the charge at the signal-source side and the charge at the data-holding side to communicate. Hence, the percentage of charge injected into the data-holding node approaches 50 percent independent of the C_S/C_L ratio. In the slow switching-off conditions, the communication between the charge at the signal-source side and the charge at the data-holding side is so strong that it tends to make the final voltages at both sides equal. This allows the majority of channel charge to go to the node with larger capacitance.

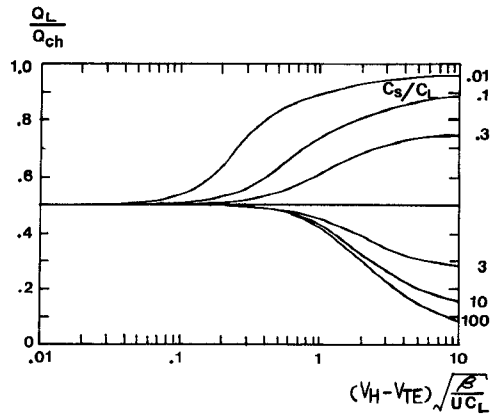

Fig. 3. Percentage of channel charge injected to the data-holding node. Source resistance is assumed to be infinitely large. A family of curves corresponding to various C_S/C_L ratios has been plotted.

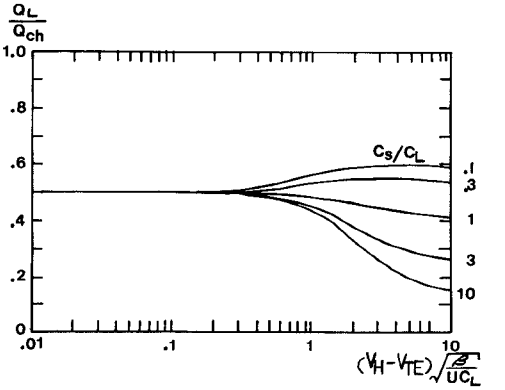

Fig. 4. Percentage of channel charge injected to the data-holding node with $V_{HT}/UR_SC_S = 1$.

Another important factor in switch charge injection is the relative magnitude of the falling rate compared with the signal time constant R_SC_S. The curves corresponding to two different V_{HT}/UR_SC_S values are shown in Figs. 4 and 5. Source resistance effectively offers a leakage path

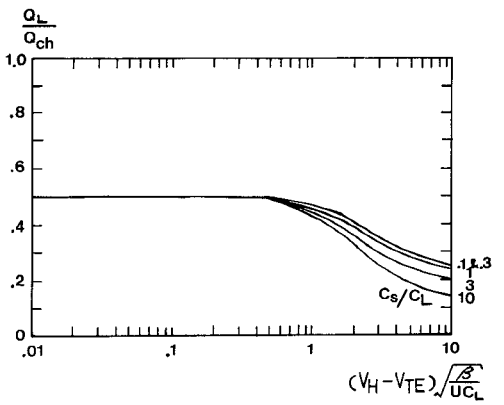

Fig. 5. Percentage of channel charge injected to the data-holding node with $V_{HT}/UR_SC_S = 5$.

for the channel charge during the switch turn-off period. Hence, a small source resistance will greatly reduce the amount of charge injected to the data-holding node.

III. Measurement

The holding capacitor is usually chosen around or above 1 pF to minimize the thermal noise voltage. Direct measurement of switch charge injection using single transistors has severe limitations. The stray capacitance of the equipment probe alters the capacitance at the interested node. When the gate voltage falling rate is high, the probe capacitance and inductance greatly perturbs measurement accuracy. On-chip circuitry can be used to circumvent the problem. It offers good buffering between the interested node and the measurement equipment. The insertion of a two-transistor source follower between the interested node and the external probe, as used by Wilson *et al.* [5], achieves the buffering function to the first order. However, a two-transistor source follower has nonlinear voltage characteristics and limited driving capability. Fig. 6 shows the two-transistor source-follower test configuration.

The unity-gain operational amplifier is found to be a better monitor of the switch charge injection. The output of the amplifier precisely tracks the input voltage. The amplifier possesses an excellent driving capability to interface with the measurement equipment. The unity-gain op-amp test configuration is shown in Fig. 7.

The circuit schematic of the operational amplifier used in the studies is shown in Fig. 8. The operational amplifier is a conventional two-stage design with a source-follower output stage [7]. It is similar to the amplifier used in the on-chip capacitance measurement of MOS transistors in some respects [8]. This circuit configuration provides good common-mode range, output swing, voltage gain, and common-mode rejection ratio. Transistors $M1-M3$ are p-channel current sources. The input stage consists of $M5-M8$. They are a p-channel differential pair with n-channel active loads and double-to-single-ended conversion. Transistors $M11$ and $M12$ are the dummy biasing string for the tracking compensation scheme and also offer dc bias to the output stage. Transistors $M4$ and $M10$ form

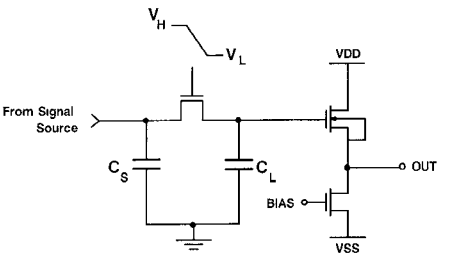

Fig. 6. A two-stage source-follower measurement approach.

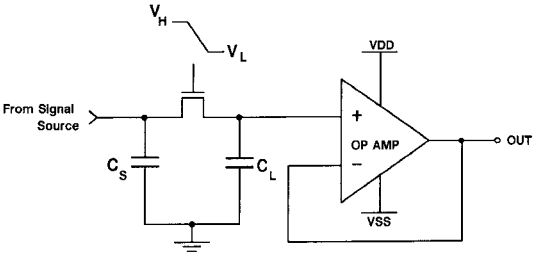

Fig. 7. A unity-gain operational-amplifier measurement approach.

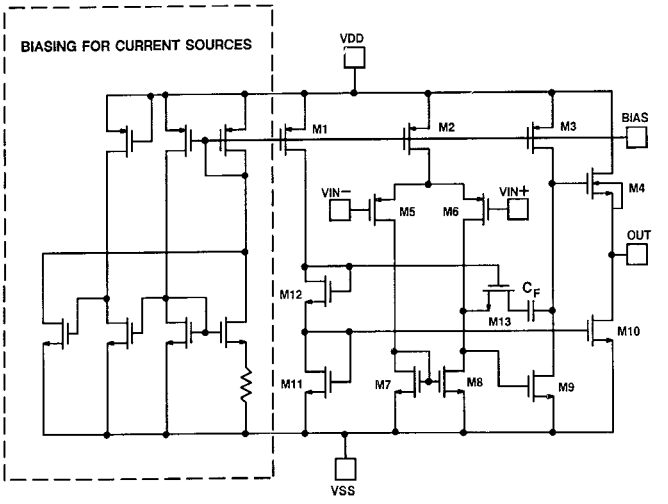

Fig. 8. Schematic of an operational amplifier suitable for charge injection monitoring.

a class-A output stage. A pole-splitting capacitor is used to compensate for the frequency response. If a fabrication process is primarily used for digital circuits and high-quality capacitors are not readily available, a thin-gate transistor can be connected to supply the necessary capacitance. Since the input-referred noise is inversely proportional to the size of the input devices, large-geometry transistors with $W/L = 99\ \mu m/6\ \mu m$ are used to keep the input-referred noise small. Notice that the substrate and source terminals of the output transistor $M4$ are connected together to eliminate the body effect. This configuration improves the amplifier output range. If an n-well process is used instead of a p-well process, then the output transistors would be changed to p-channel transistors because the transistor inside a well can have its substrate and source tied together. The bias of the current sources can be derived in two ways. A dedicated biasing circuit can be used. The other alternative is to apply an external bias to the pad BIAS. The latter approach turns out to be a good

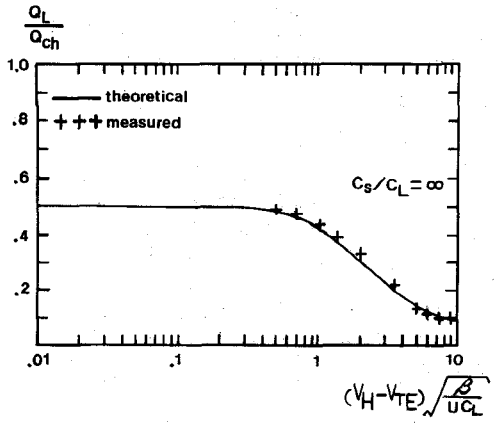

Fig. 9. Comparison of measured and theoretical charge injection results for the special case of Fig. 2(a). The gate voltage falling rate was varied in the experiments.

choice in the application because it reduces the size of the whole test pattern without sacrificing any measurement accuracy. The dotted portion in Fig. 8 denotes the optional biasing block for the current sources.

IV. Experimental Results

The transistors used in the experiments were fabricated using a 3-μm CMOS process. The transistor gate-oxide thickness is 50.0 nm, substrate doping is 10^{16} cm^{-3}, and zero-bias threshold voltage is 0.9 V. Percentage charge injection was measured against the gate voltage falling rate ranging from 1.25×10^{6} to 5×10^{8} V/s. Fig. 9 shows the measured data and theoretical results. Good agreement between the theoretical results and experimental data is found.

V. Conclusion

Charge injection in MOS switches has been analyzed. The analysis has been extended to the general case which includes signal-source resistance and capacitance. This extension makes the results useful for the various conditions encountered in integrated-circuit applications. Plots of the percentage charge injection corresponding to various normalized parameters are presented. The source resistance effectively offers a leakage path for the channel charge during the switch turn-off period. On-chip test circuitry with a unity-gain operational amplifier, which reduces the disturbance imposed by the measurement equipment to a minimum, is found to be an excellent monitor of switch charge injection.

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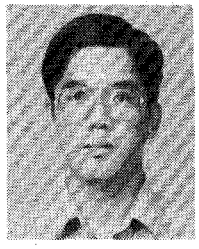

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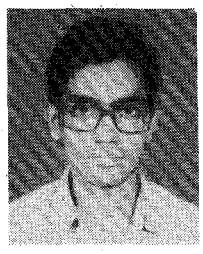

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