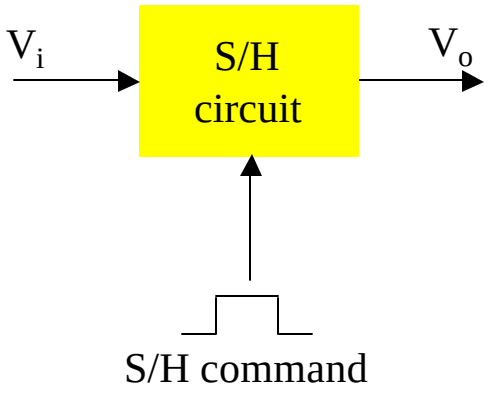
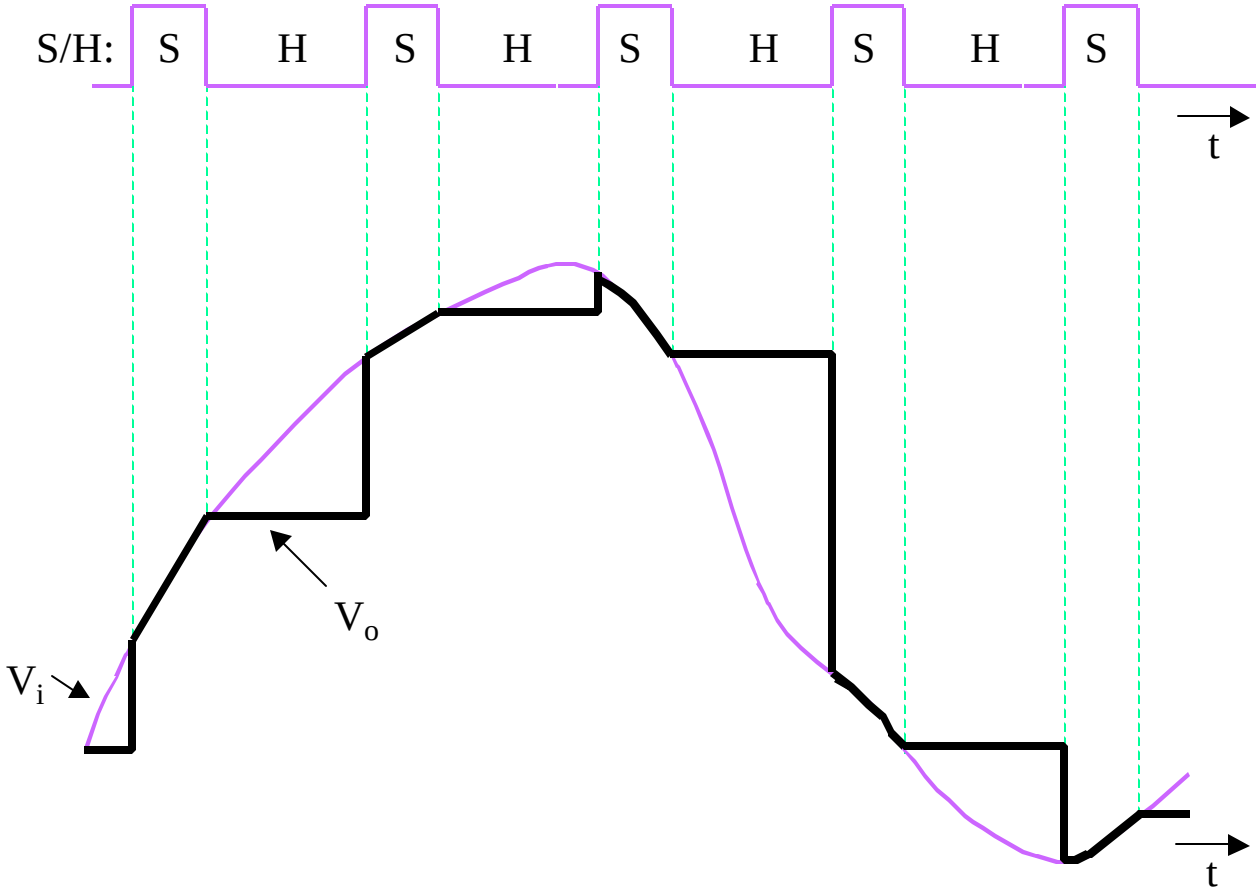
Track & Hold: Architectures and Circuits

Analog and Mixed-Signal Center, TAMU

Sample-and-Hold Circuit



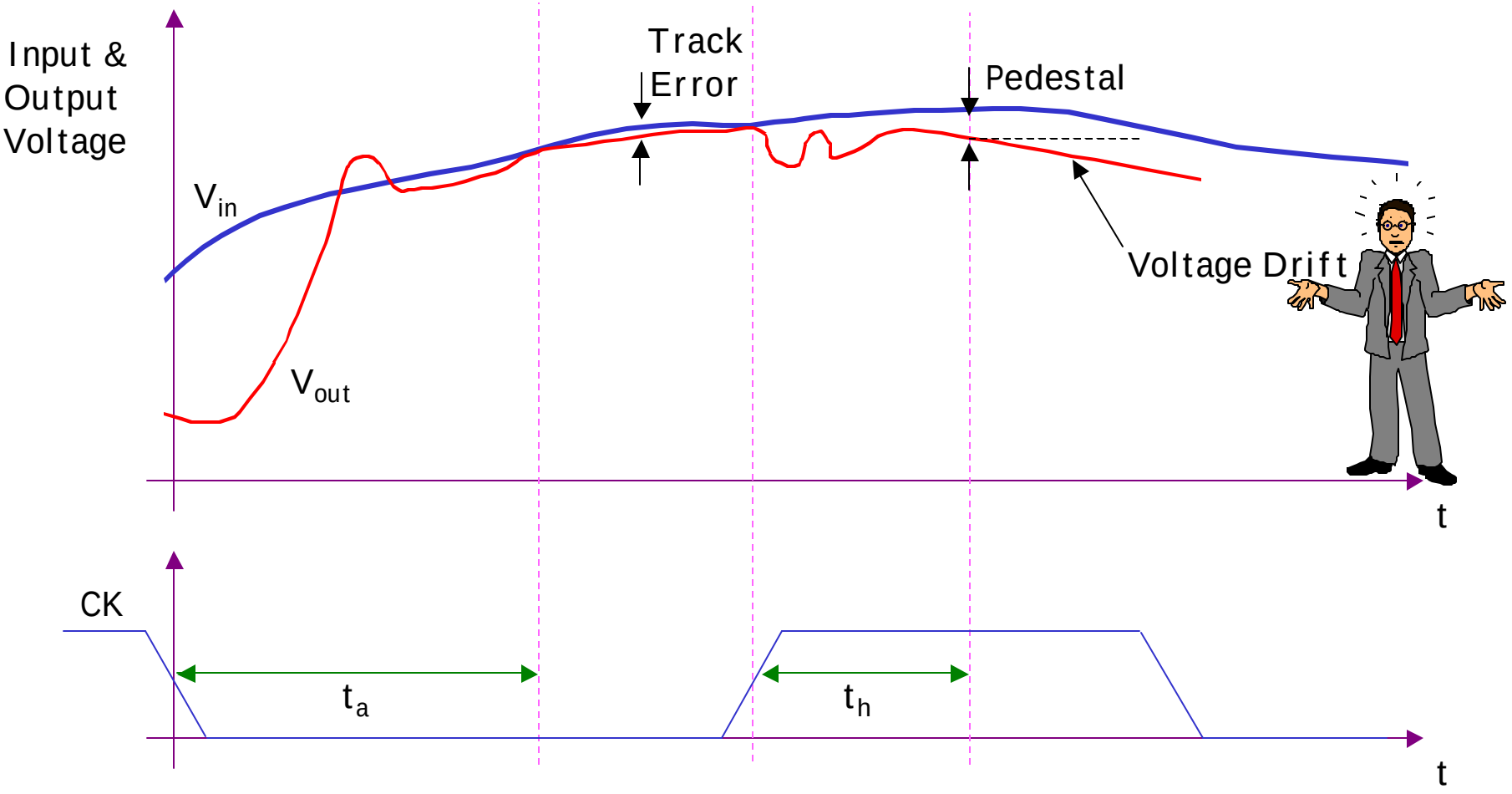
Block Diagram



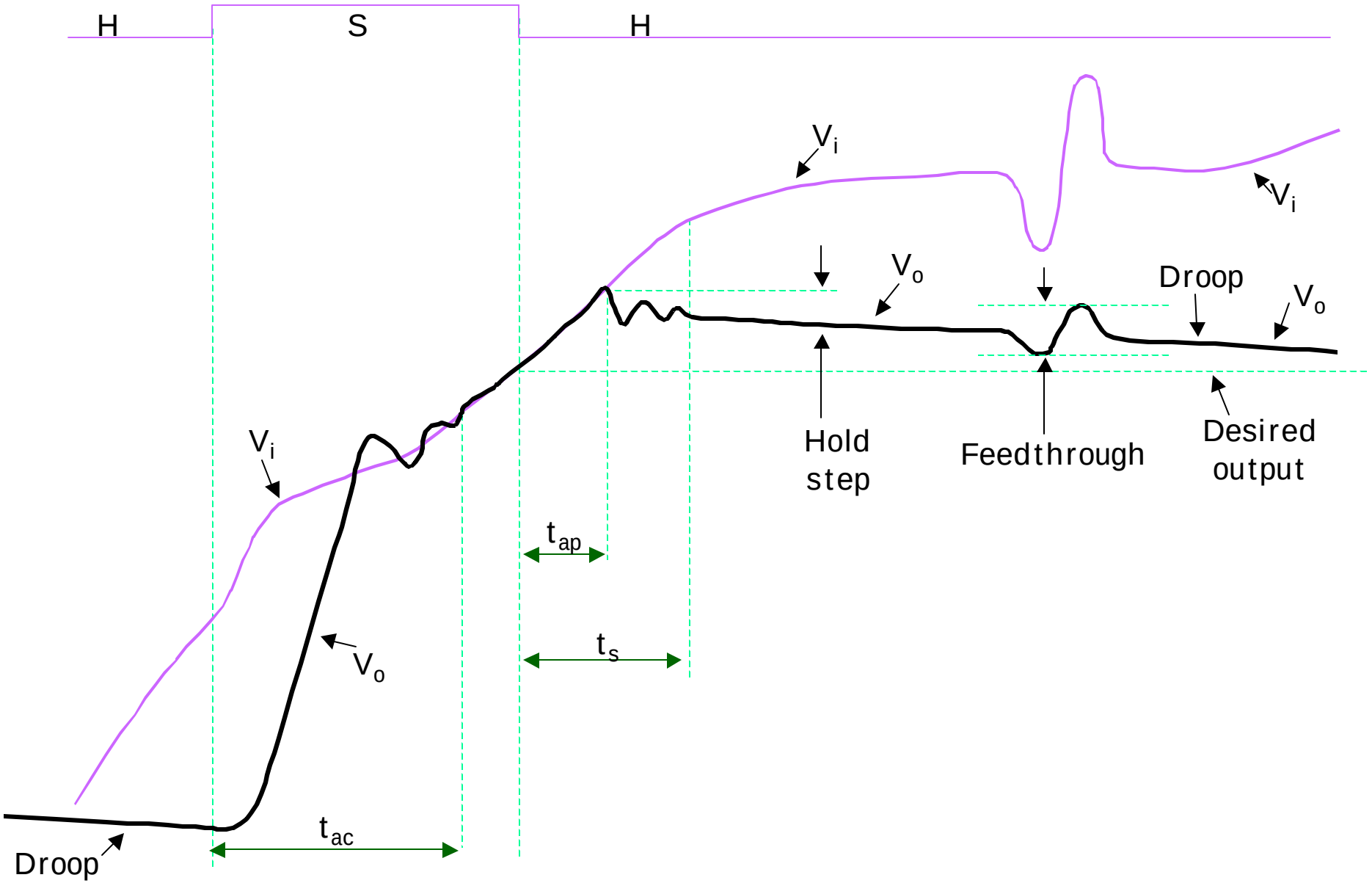
Idealized Response

Performances of S & H

Realistic Transient Response:



S/H Circuit Waveforms and Performance Parameters



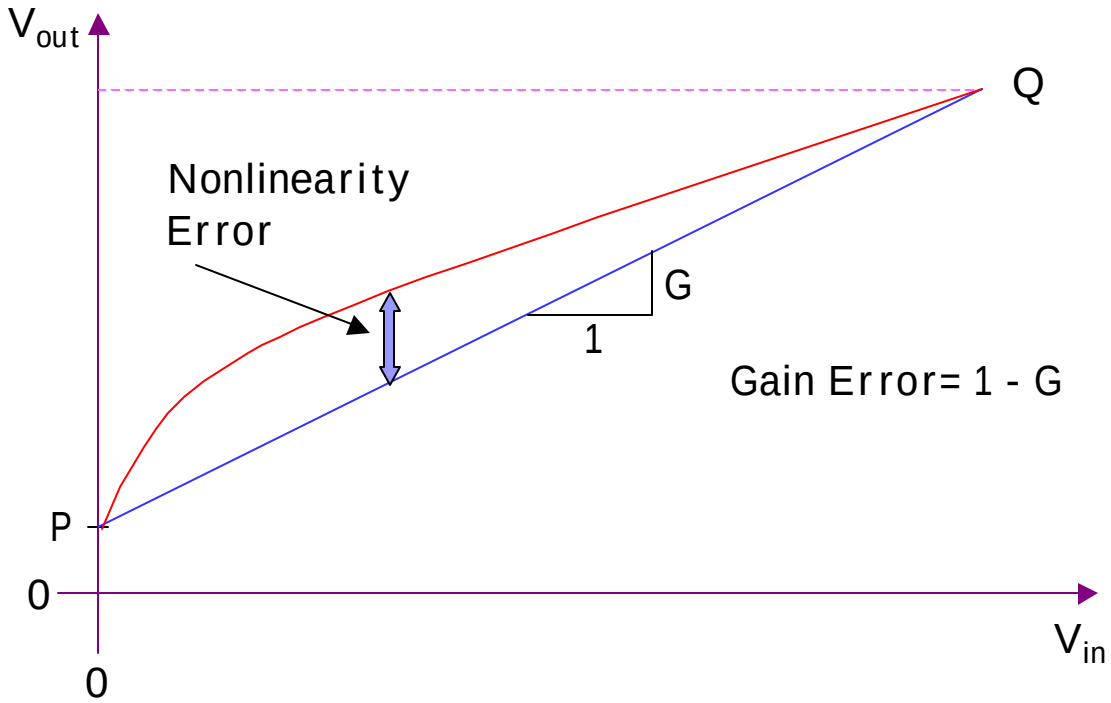
Performance Definition

- **Acquisition Time: the required time for the output transient after the sampling signal.**
- **Hold Settling Time: the time after the hold signal required for the output to settle within an acceptable error.**
- **Pedestal Error: due to the transition of sample to hold mode.**
- **Voltage Drift: the rate of discharge of the sampling capacitor during the hold mode.**
- **Dynamic Range: the ratio of the maximum and minimum input level, which can be sampled with a given resolution.**

Performance Definition

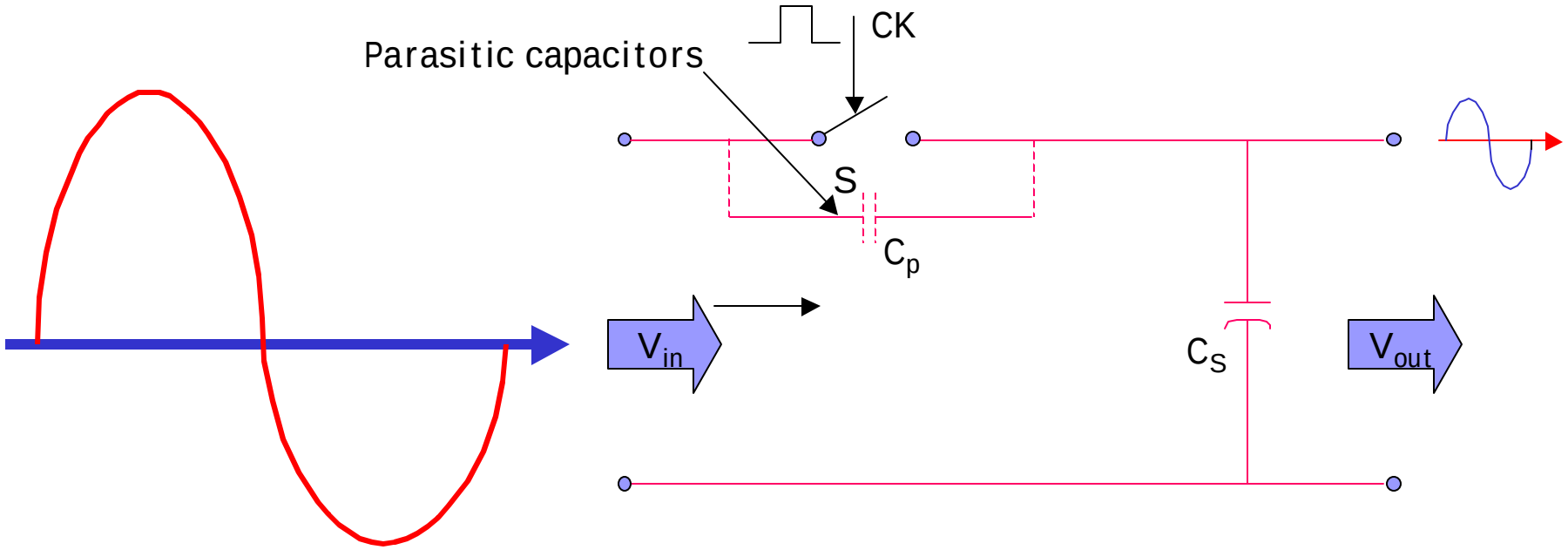
- **Nonlinearity Error: the maximum deviation of the V_{out}/V_{in} characteristic from the straight line passed through the end points.**

- **Gain Error: the deviation of the slope of the straight line from unity.**



Performance Definition

- **Hold Mode Feedthrough: the percentage of the input signal that appears at the output during the hold mode.**

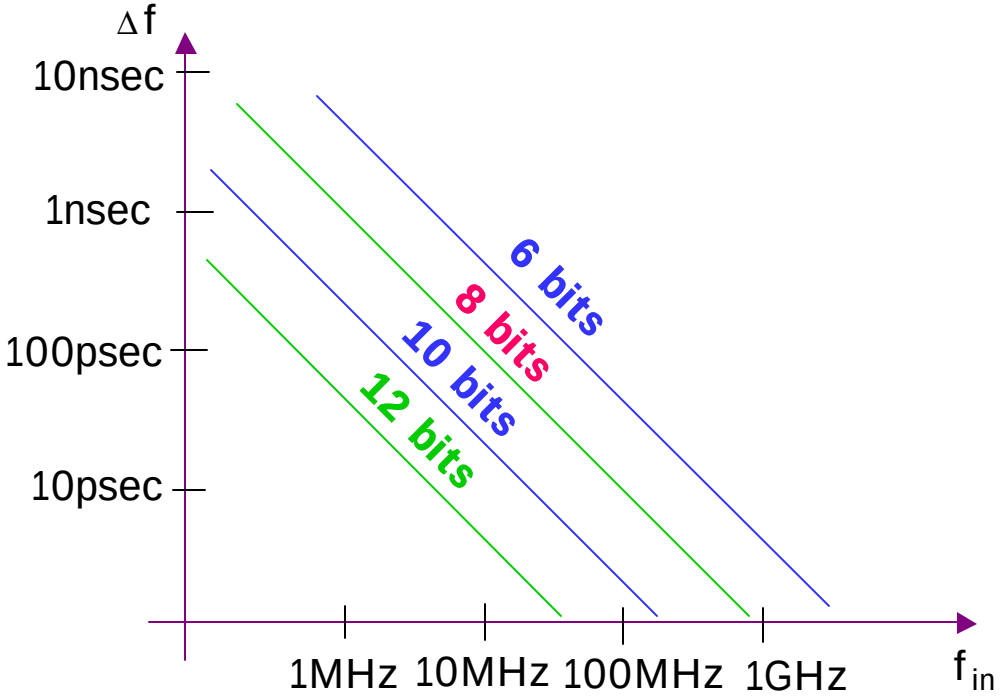


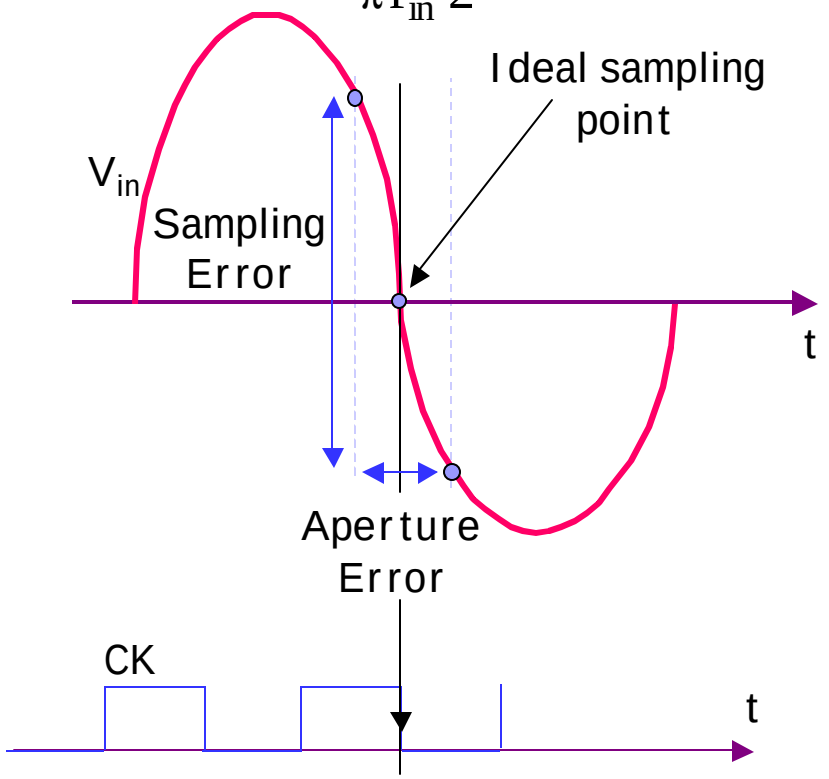
Performance Definition

- **Aperture Error: the random variation of the turn off time of the switch results in an uncertain sampling time.**

Maximum Allowable Aperture Error for 1/2 LSB:

$$\Delta t_{max} = \frac{1}{\pi f_{in} 2^{N+1}}$$

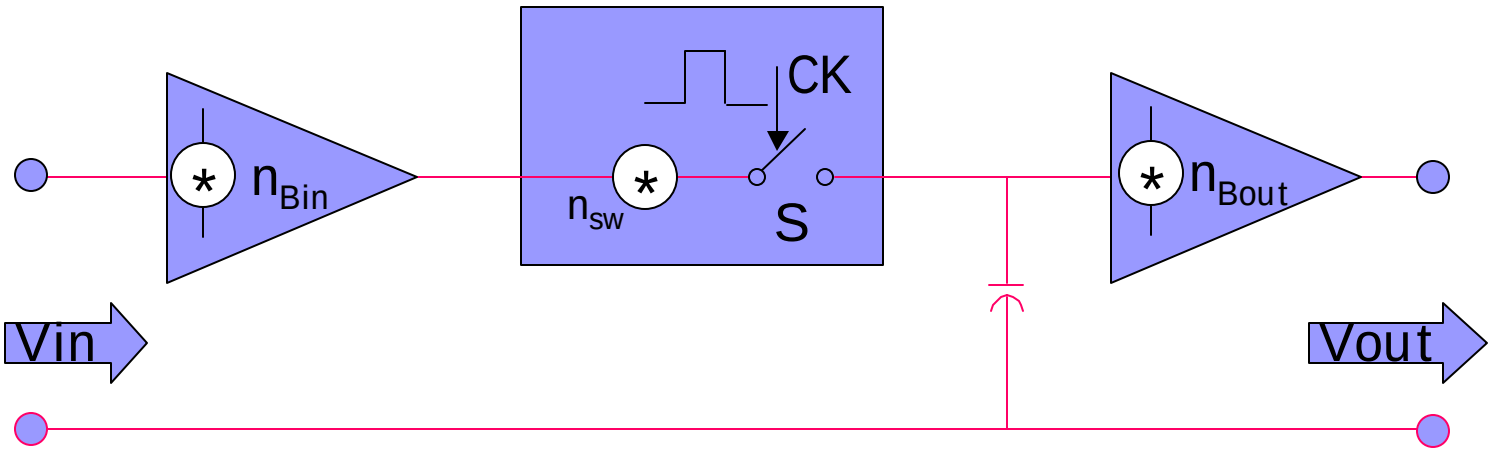




Performance Definition

- **Signal-to-Noise Ratio (SNR): the ration of the signal power to the noise power at the output. The sources of noise are the input and output buffer, switch, and clock jitter.**

- **Signal to Noise + Distortion Ratio (SNDR): the ration of signal power to the total noise and harmonic power at the output. The source of harmonics are the nonlinearity of the buffers and the switch.**



Sample-and-Hold Basic Architectures

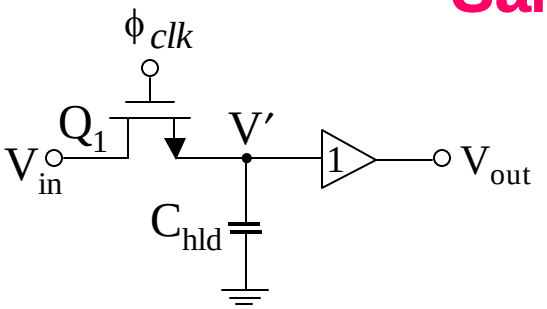


Fig. 1 An open-loop track and hold realized using MOS technology.

Analysis

$$\Delta Q_{C_{hld}} = \frac{Q_{CH}}{2} = \frac{C_{OX}WLV_{eff-1}}{2}$$

where V_{eff-1} is given by

$$V_{eff-1} = V_{GS1} - V_{tn} = V_{DD} - V_{tn} - V_{in}$$

$$\Delta V' = \frac{\Delta Q_{C-hld}}{C_{hld}} = -\frac{C_{OX}WLV_{eff-1}}{2C_{hld}} = -\frac{C_{OX}WL(V_{DD} - V_{tn} - V_{in})}{2C_{hld}}$$

$$\Delta V' \cong -\frac{C_{OX}WL_{OV}(V_{DD} - V_{SS})}{C_{hld}}$$

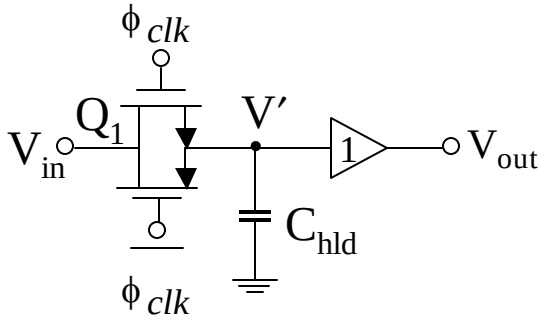


Fig. 2 An open-loop track and hold realized using a CMOS transmission gate.

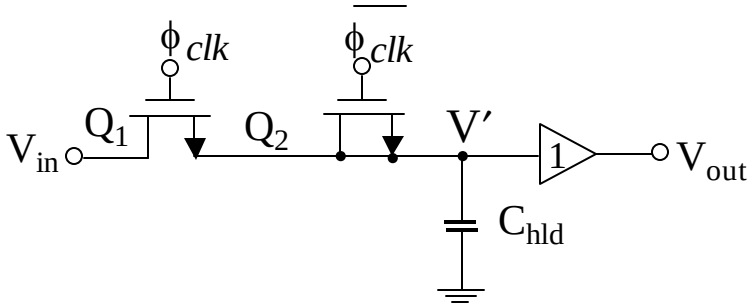
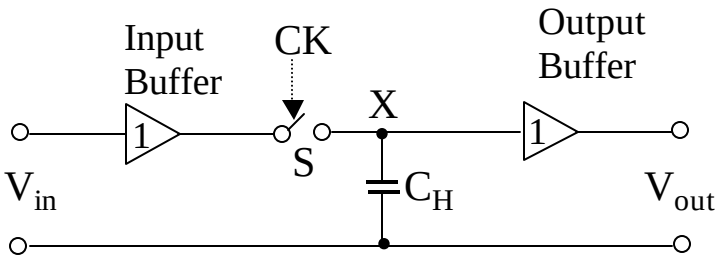


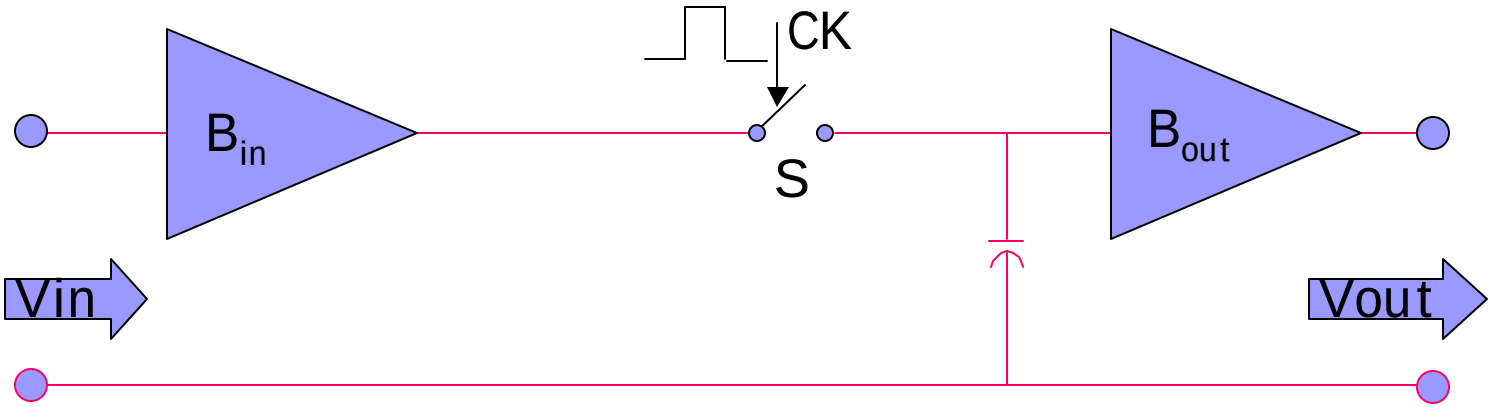
Fig. 3 An open-loop track and hold realized using an n-channel switch along with a dummy switch for clock-feedthrough cancellation.



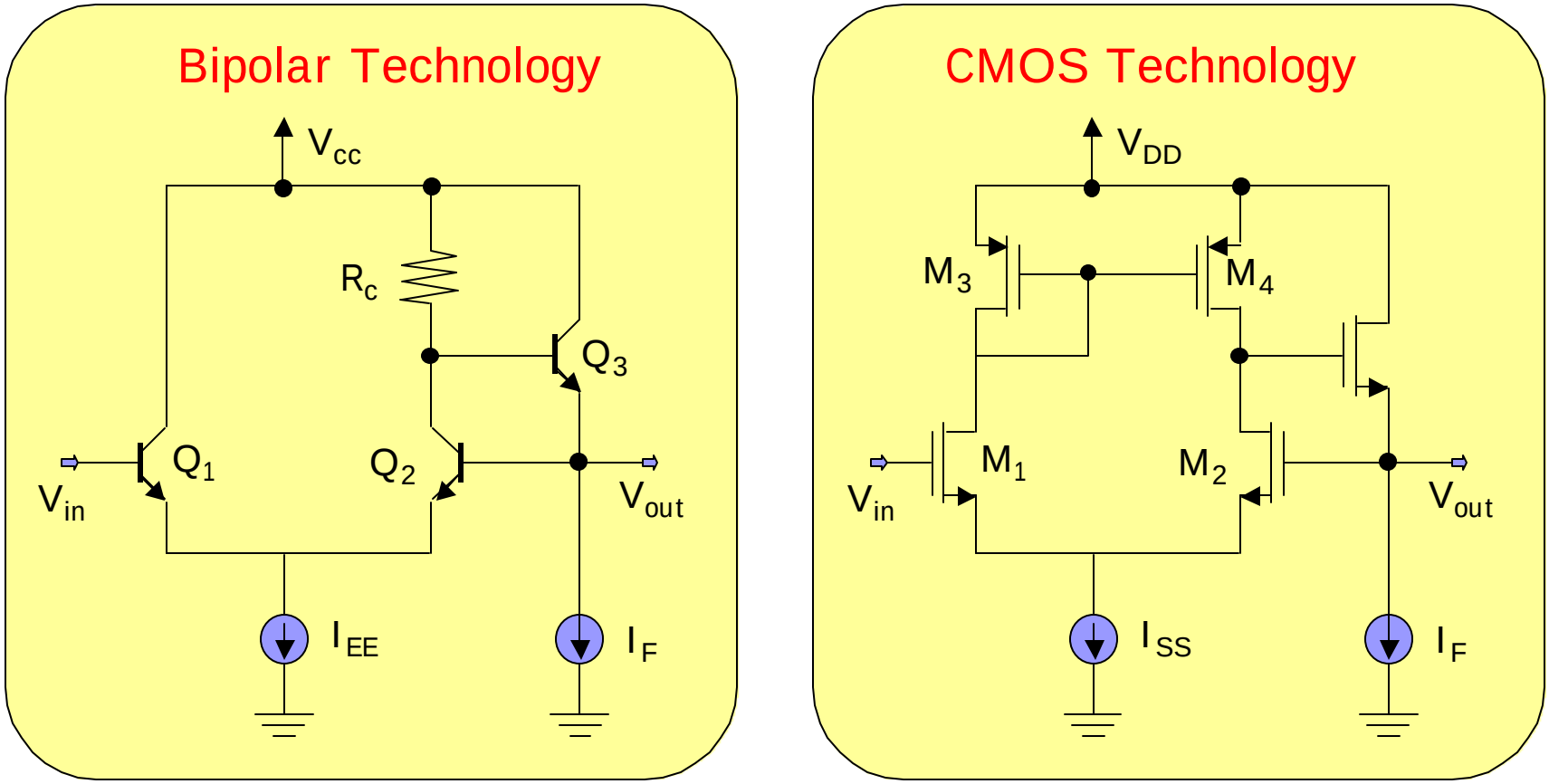
Buffered Sample & Hold Circuit

- Input and Output Buffer:

The capacitor voltage during the hold mode can be affected by the current drawn by the following circuit. Therefore, the output voltage is buffered.



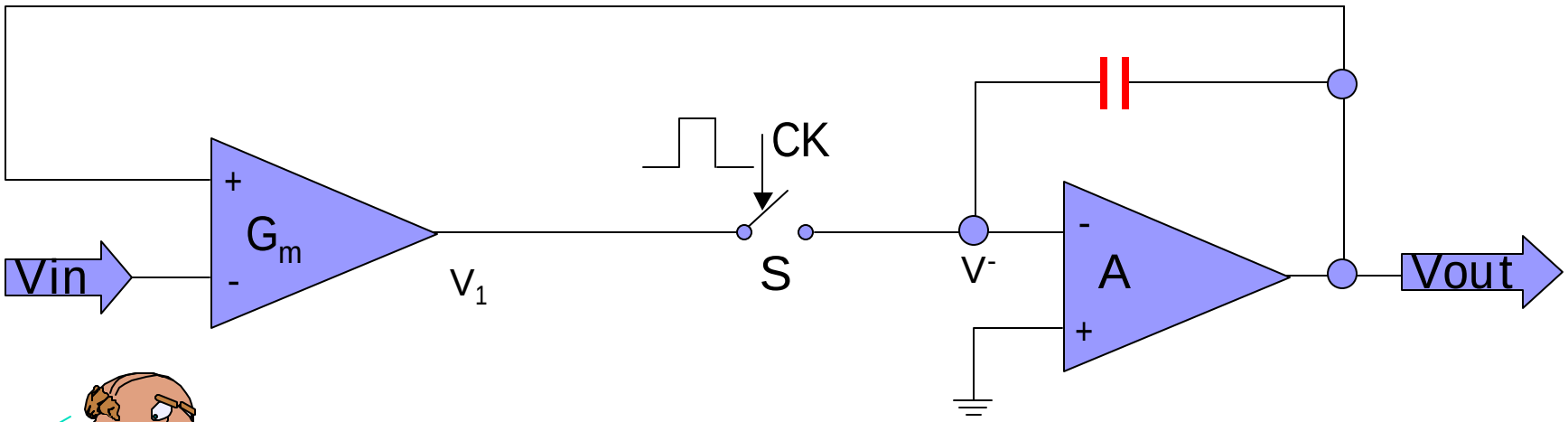
Unity Gain Buffer Circuit: BJT and CMOS implementations

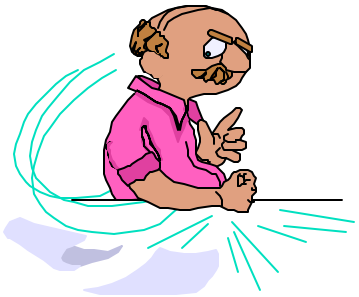


Track & Hold (T&H) Circuit

Simple Closed-Loop Architecture:

During the sampling time, the drain and source voltage of MOS switch are closed to ground. Thus the charge injection and clock feedthrough introduce an offset voltage at the output and is independent of the input voltage.



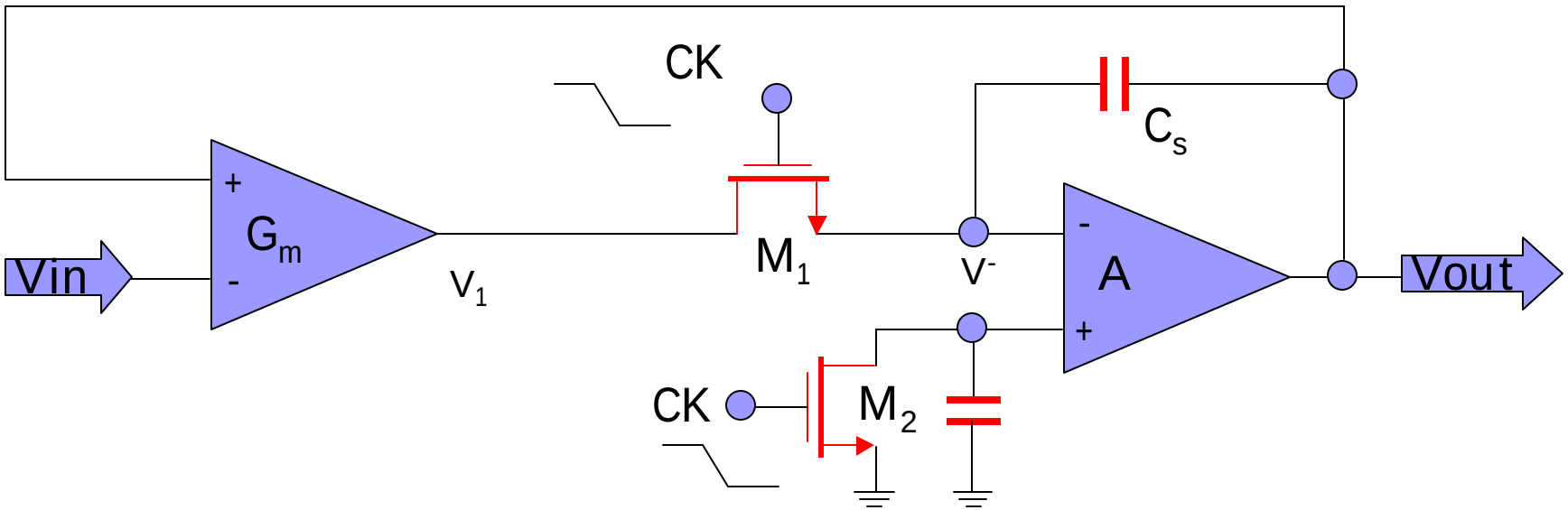


Disadvantage: stability problems and low speed.

T&H Circuit: Closed-Loop Architecture

Offset Voltage Cancellation:

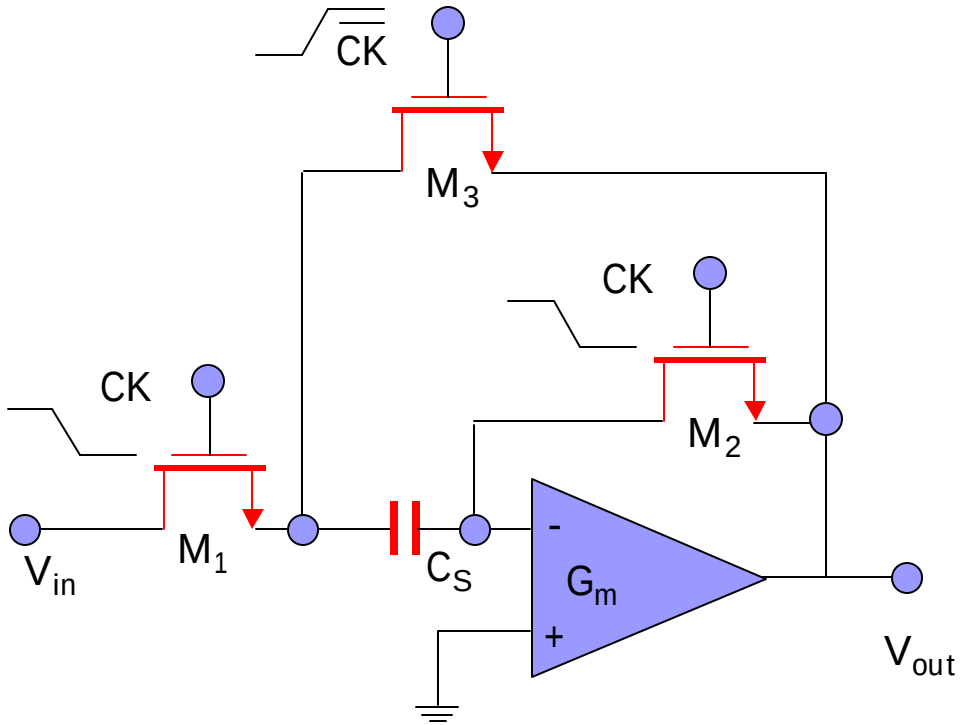
The charge injection and clock feedthrough can be cancel out by applying a replica of the offset voltage to the positive terminal of the second amplifier (common-mode voltage).

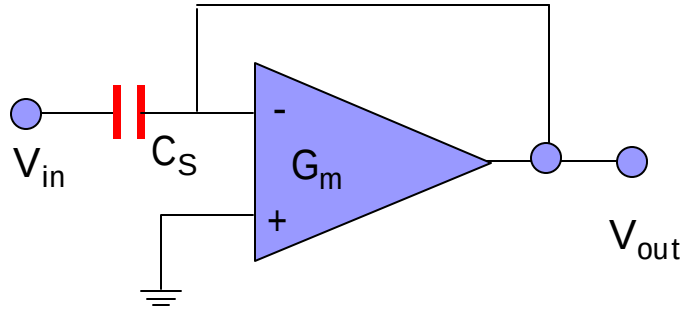


T&H Circuit: Switched Capacitor

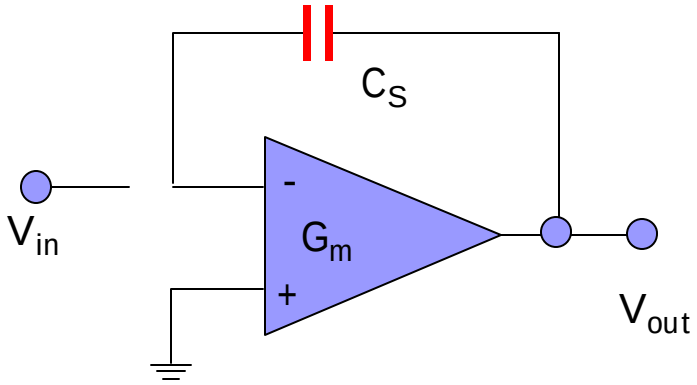
Switched-Capacitor Architecture:

This architecture consists of sampling capacitor C_S, amplifier G_m, and MOS switches.





Track Mode (CK=1)



Hold Mode (CK=0)

Evolution of S/H Architectures

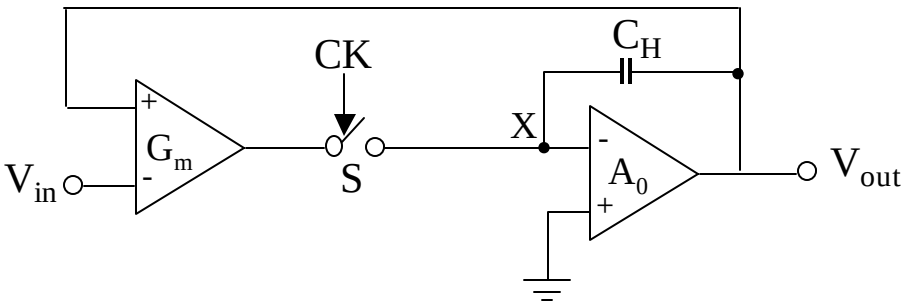


Fig A. Closed-loop sample-and-hold architecture.

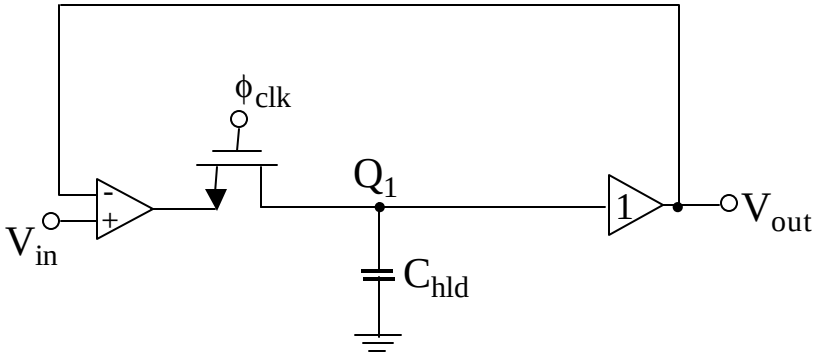
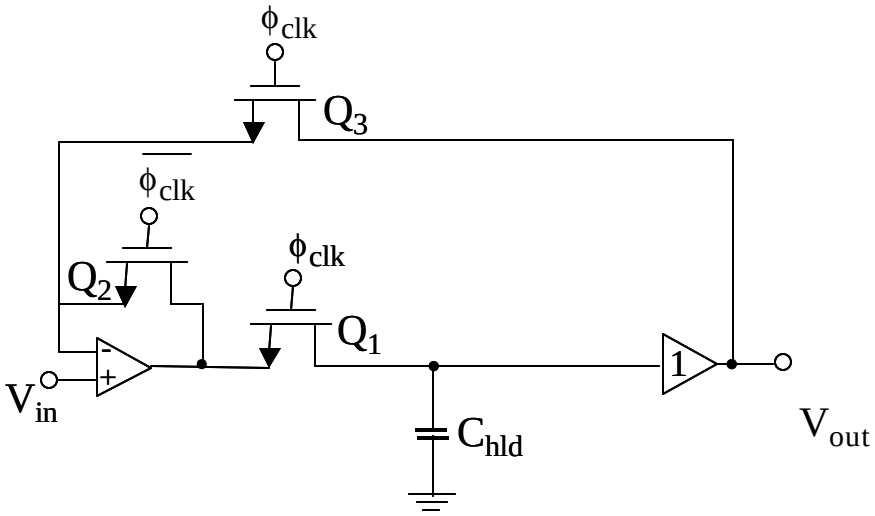


Fig B. Including an opamp in a feedback loop of a sample and hold to increase the input impedance.



C. Adding on additional switch to the S/H of Fig B to minimize slewing time.

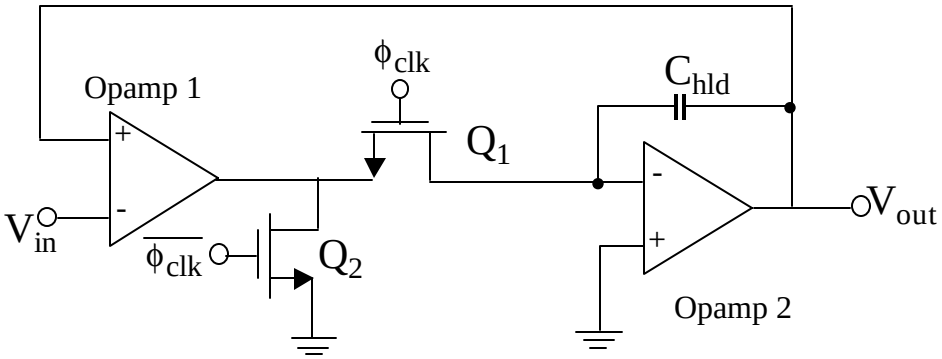
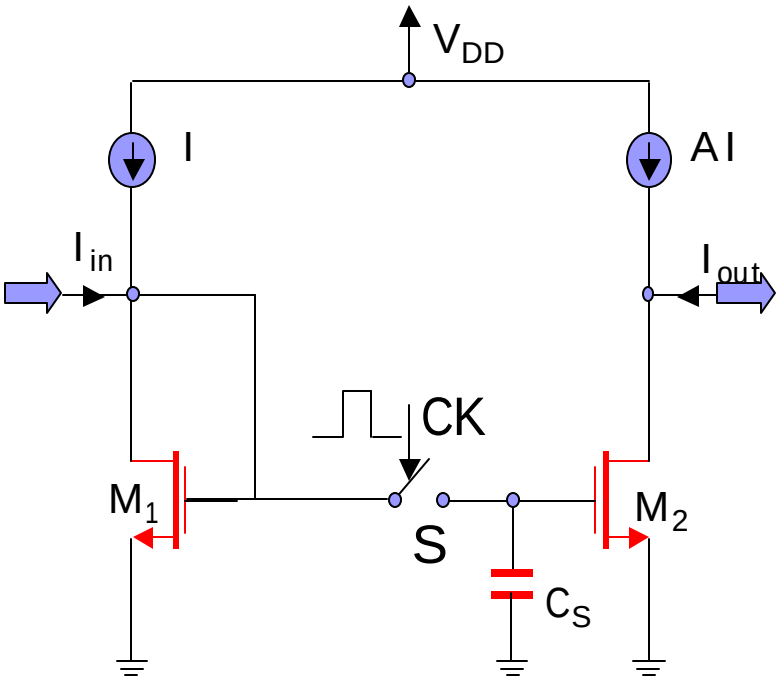


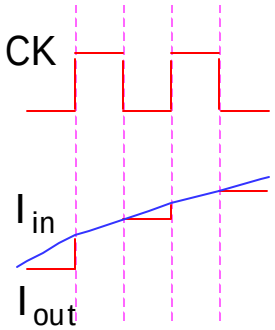
Fig D An improved configuration for an S/H as compared to that of Fig C

T&H Circuit: Current-Mode

Current-Mode Architecture:

Advantages: high-speed (over 100MHz) and low voltage (<1.2).
The speed depends on the time constant given by:



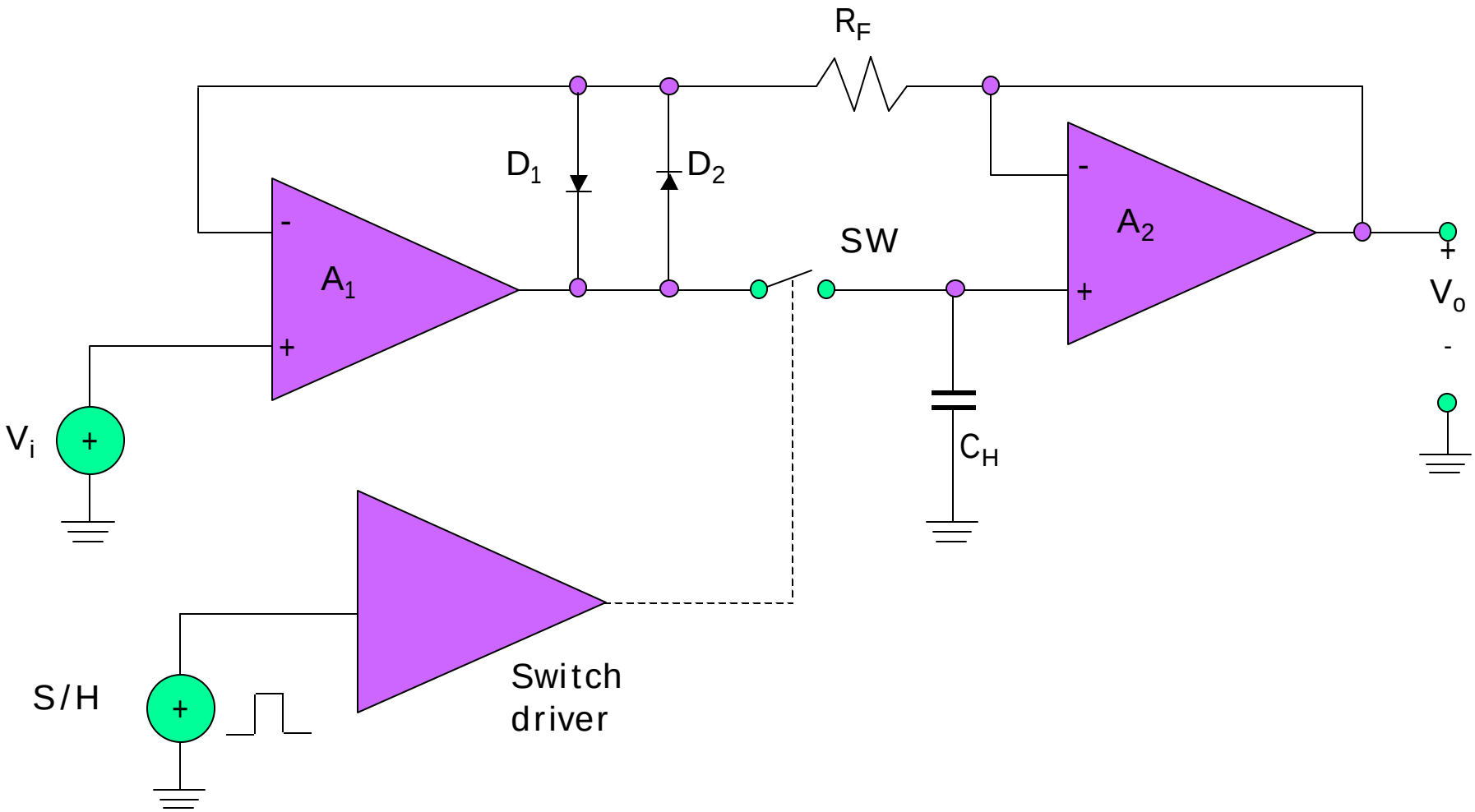


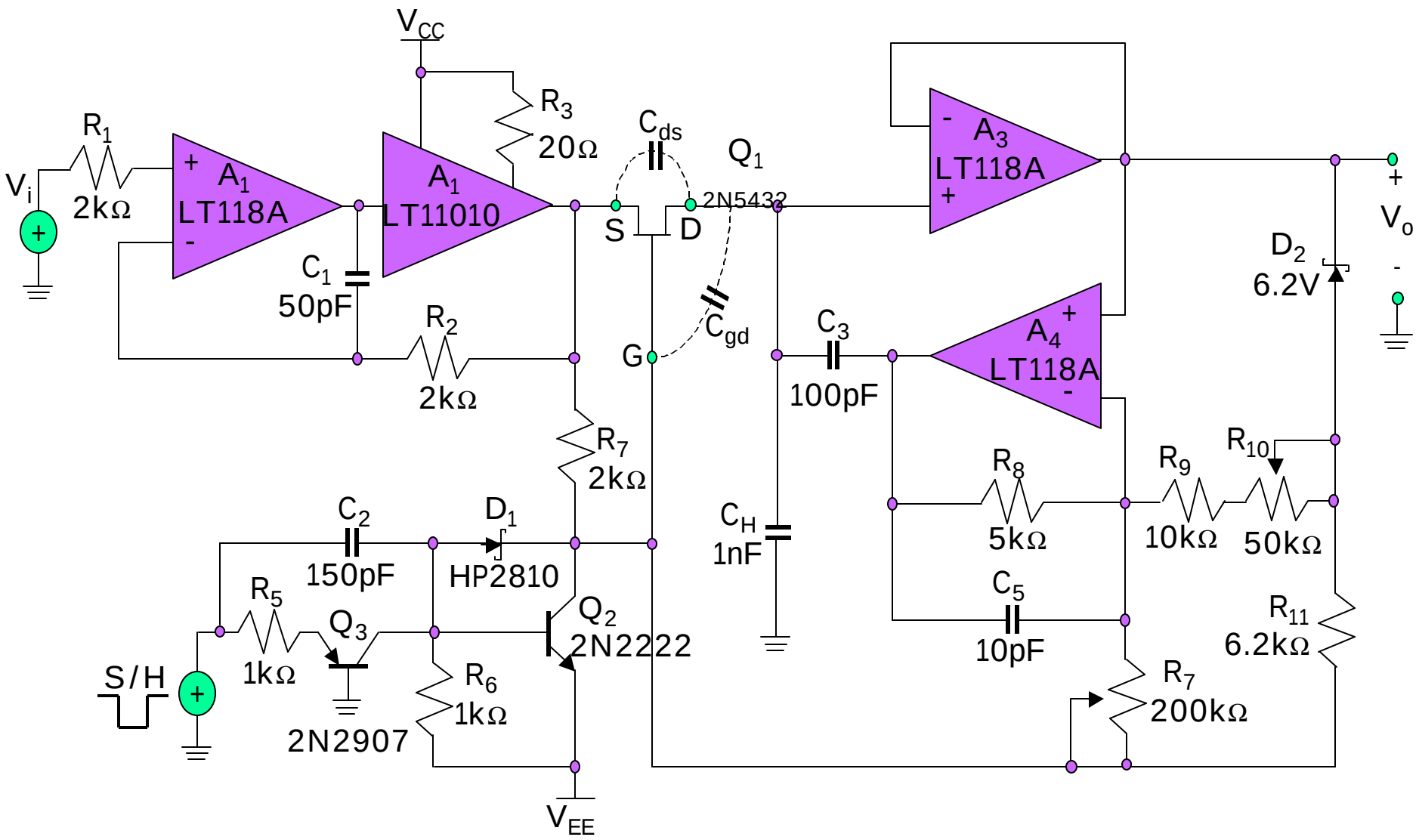
$$\tau = \frac{C_S}{g_{m1}}$$

$$C_S = \frac{2}{3} C_{ox} (1 + A) W_1 \bullet L_1$$

$$g_{m1} = \mu C_{ox} \frac{W}{L} (V_{GS} - V_{Tn})$$

Two Op Amps S/H Circuit





A 5 MHz track-and-hold circuit, using discrete components, with charge compensation to minimize the hold step.

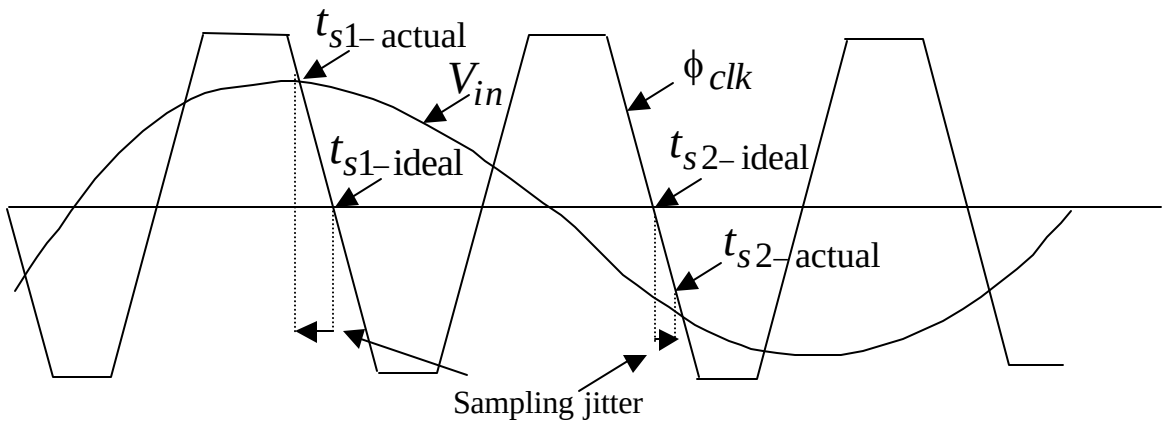


Fig. The clock waveforms for V_{in} and ϕ_{clk} used to illustrate how a finite slope for the sampling clock introduces sampling-time jitter.

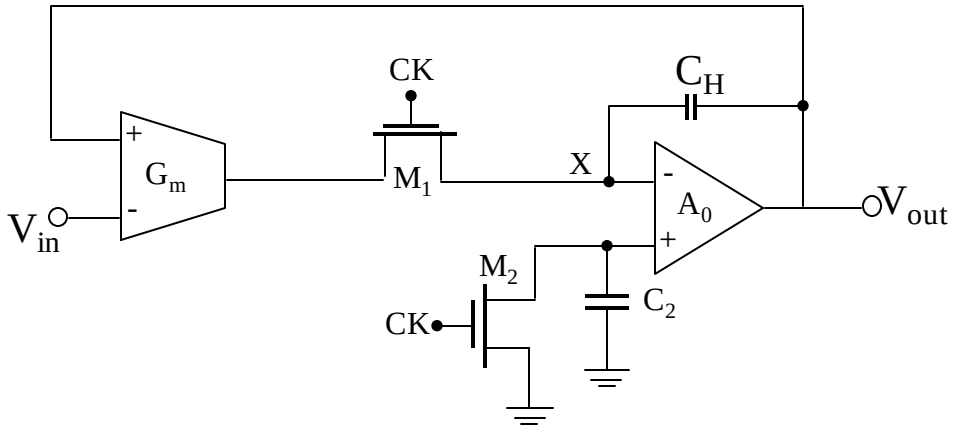


Fig. Closed-loop sample-and-hold architecture with pedestal cancellation.

S/H Open Loop Architecture with Miller Capacitance

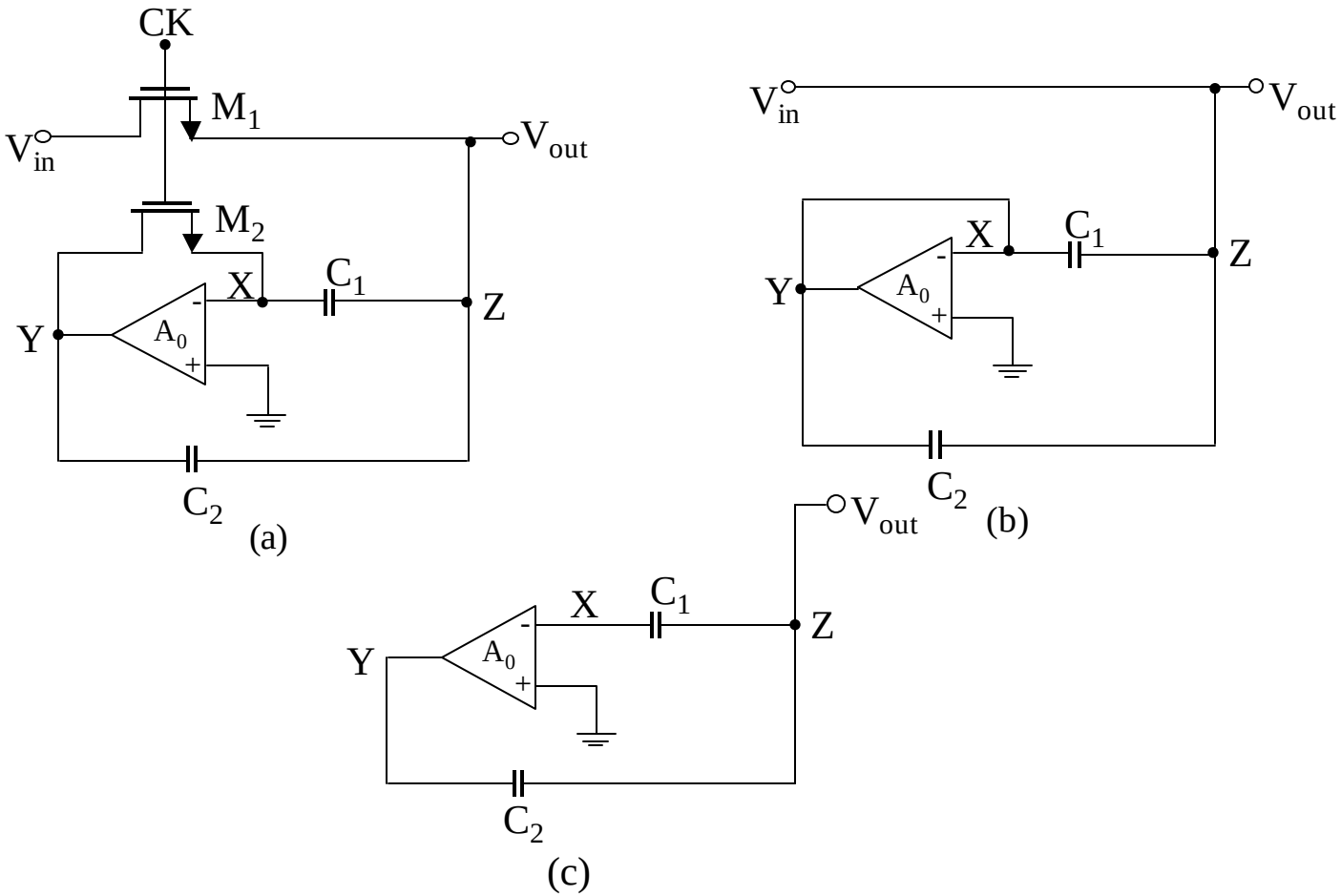
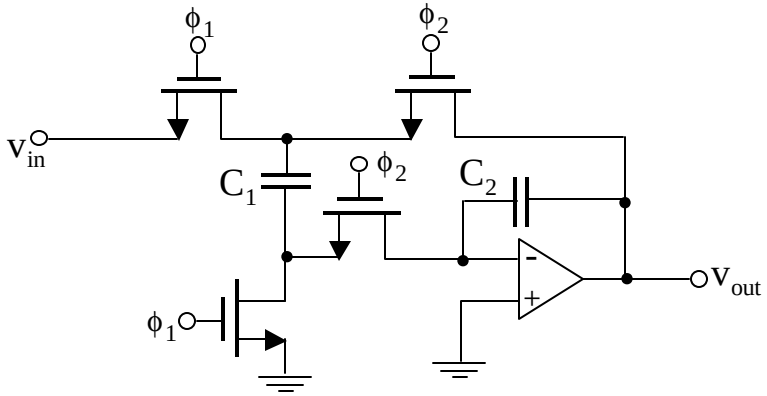


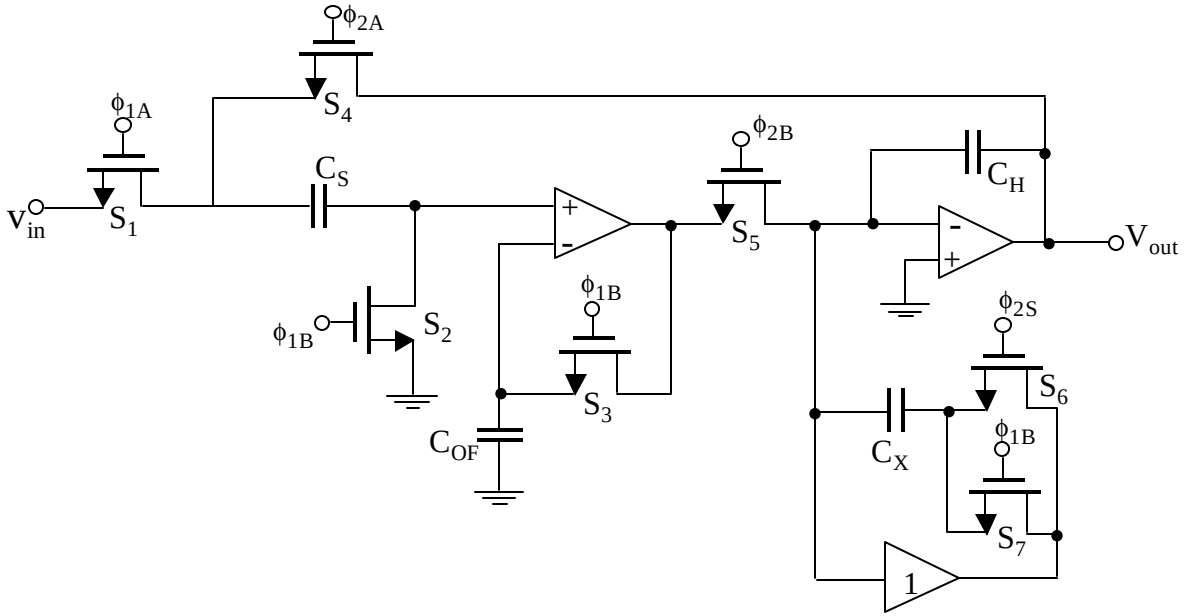
Fig. Open-loop architecture with Miller capacitance. (a) Basic circuit; (b) equivalent circuit in the acquisition mode; (c) equivalent circuit in the hold mode.

The open-loop architecture with Miller capacitance employs two different values of capacitance in the acquisition and hold modes to achieve high speed and small pedestal error. This is accomplished using a Miller amplifier that multiplies the effective value of the sampling capacitor by a large number when the SHA enters the hold mode.

Switched-Capacitor S/H Implementations

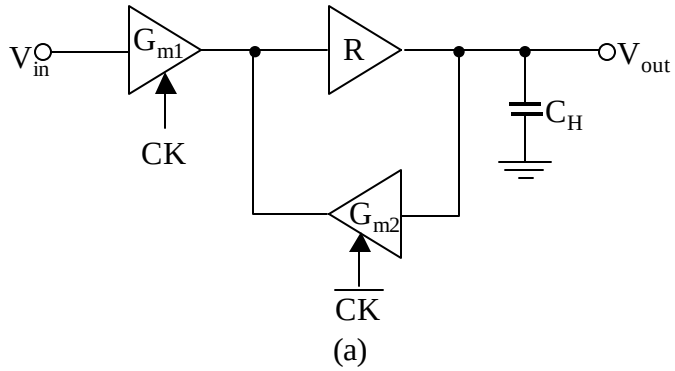


A switched-capacitor sample and hole and low-pass filter.

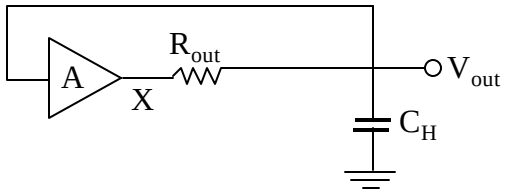


A switched-capacitor S/H.

MULTIPLEXED-INPUT ARCHITECTURES



(a)



Multiplexed-input architecture. (a) Basic (single-ended) circuit; (b) equivalent circuit in the hold mode.

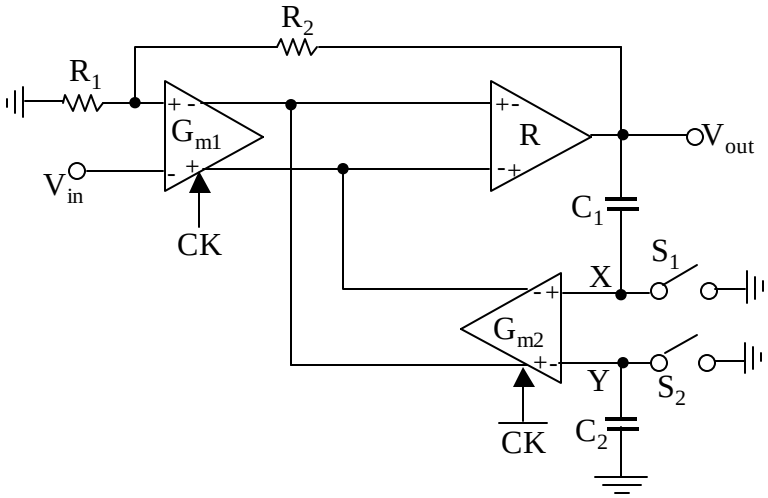
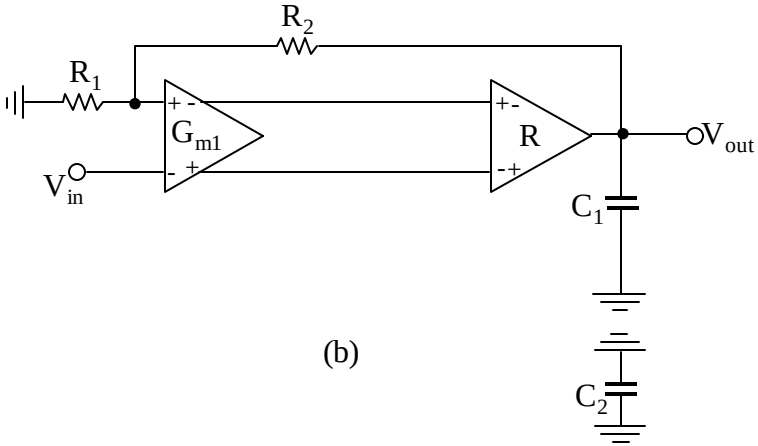
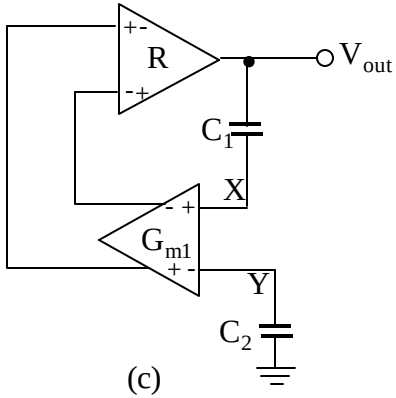


Fig. 15(a) Dual-loop multiplexed architecture.



(b)



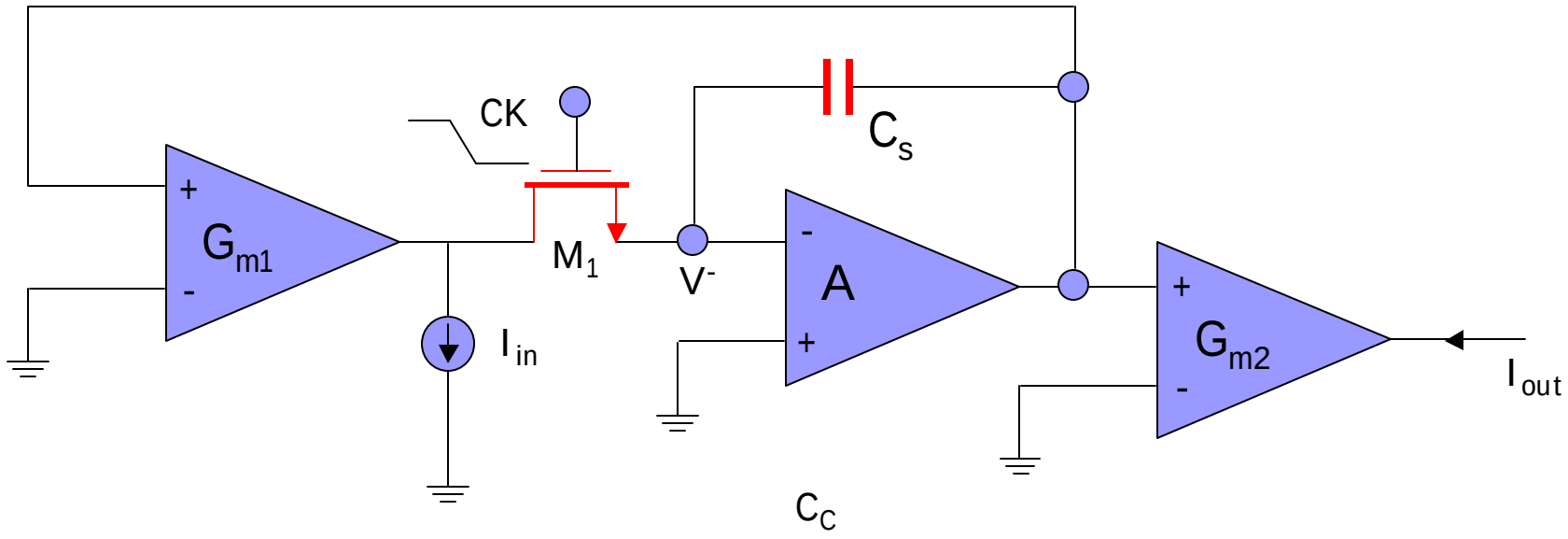
(c)

Equivalent circuits of dual-loop multiplexed-input architecture. (b) Acquisition mode; (c) hold mode.

T&H Circuit: Current-Mode

Closed-Loop Current-Mode Architecture:

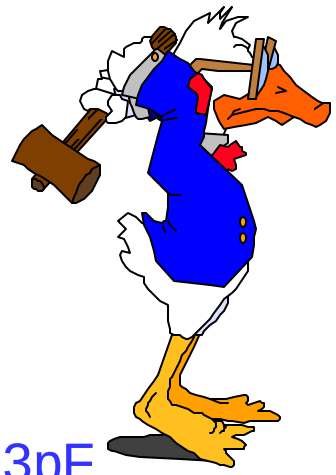
This architecture needs stability and speed considerations.
The distortion of G_{m2} affects directly the output current [21].



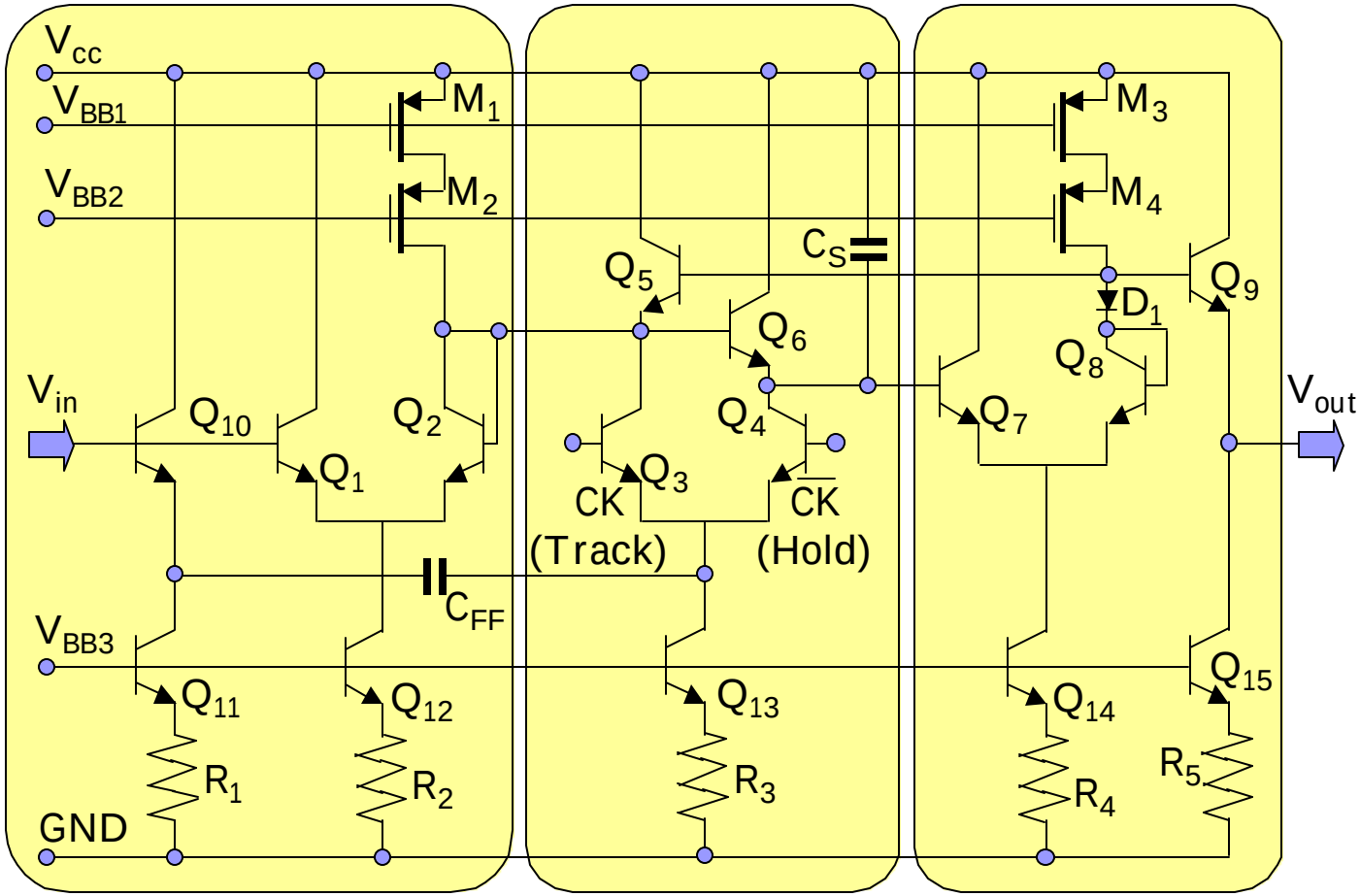
T&H Circuit: Example

BiCMOS Track & Hold Amplifier (12-Bit & 50Msps):

This circuit consists of input buffer, hold section, and output buffer [3].



C_S=3pF
C_{FF} is a feed-forward compensation capacitor for the charge injection of Q_4



RECYCLING S/H ARCHITECTURE

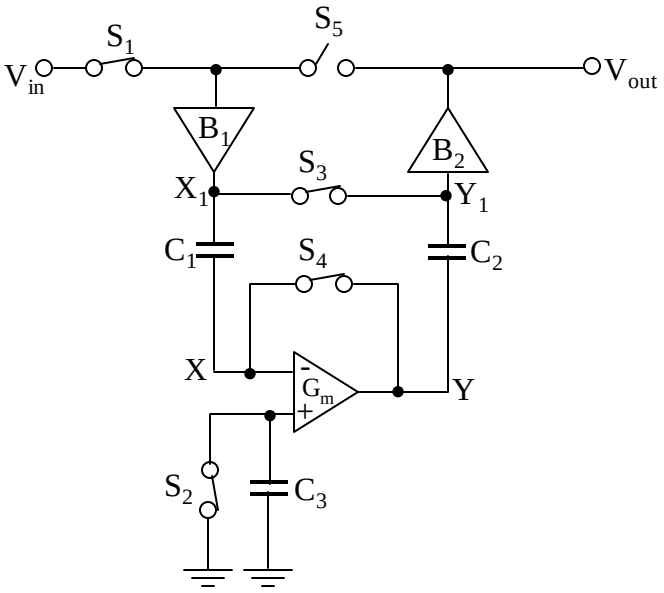


Fig. 16 Recycling architecture.

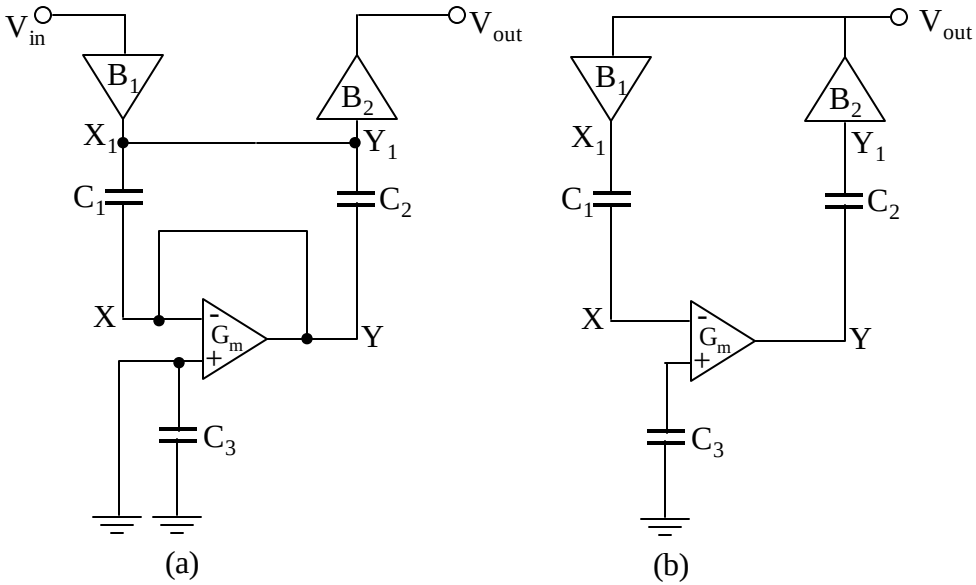
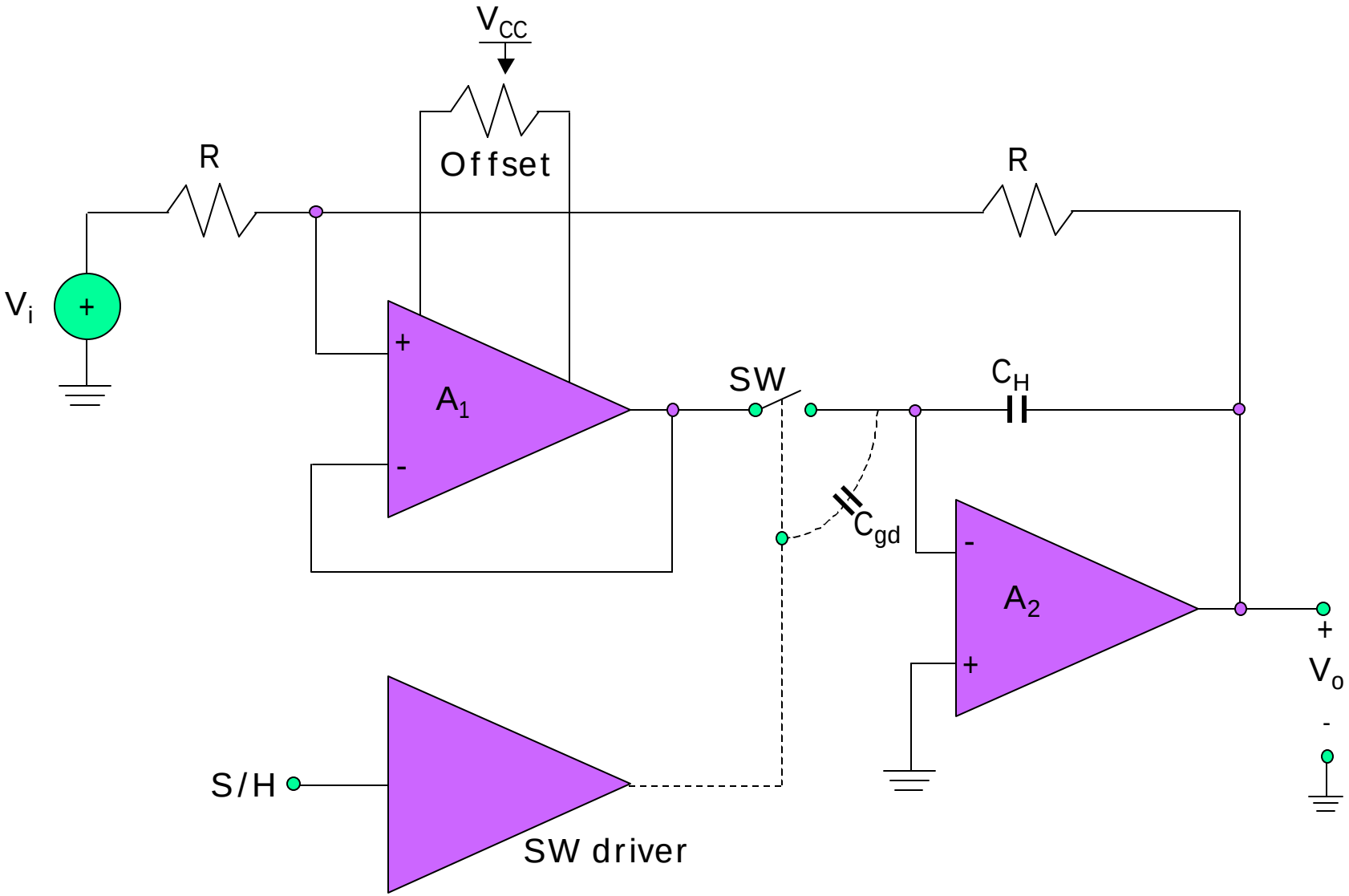
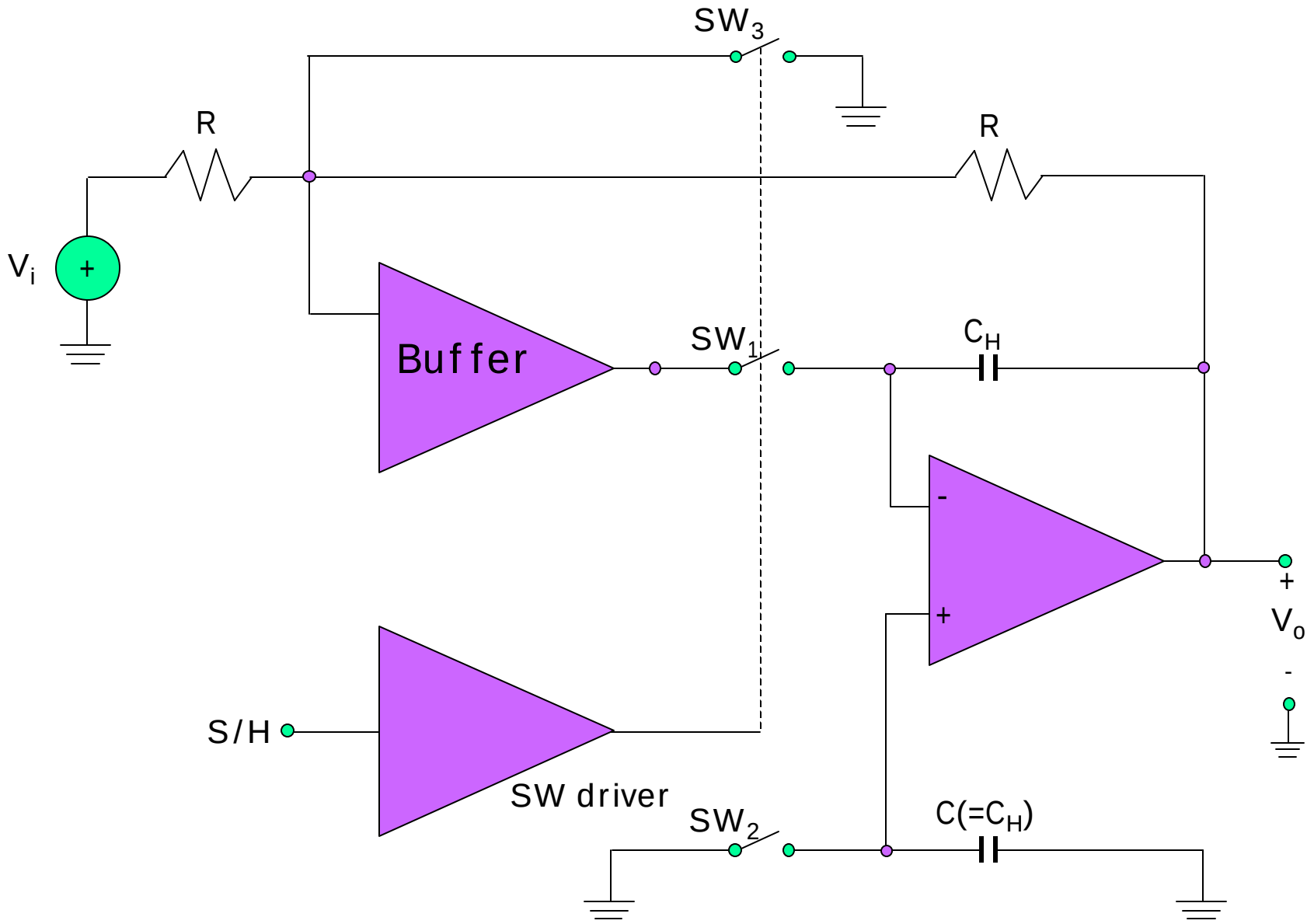


Fig. 17 Equivalent circuits of recycling architecture. (a) Sampling mode; (b) hold mode.

Integratating Amplifier S/H Circuit



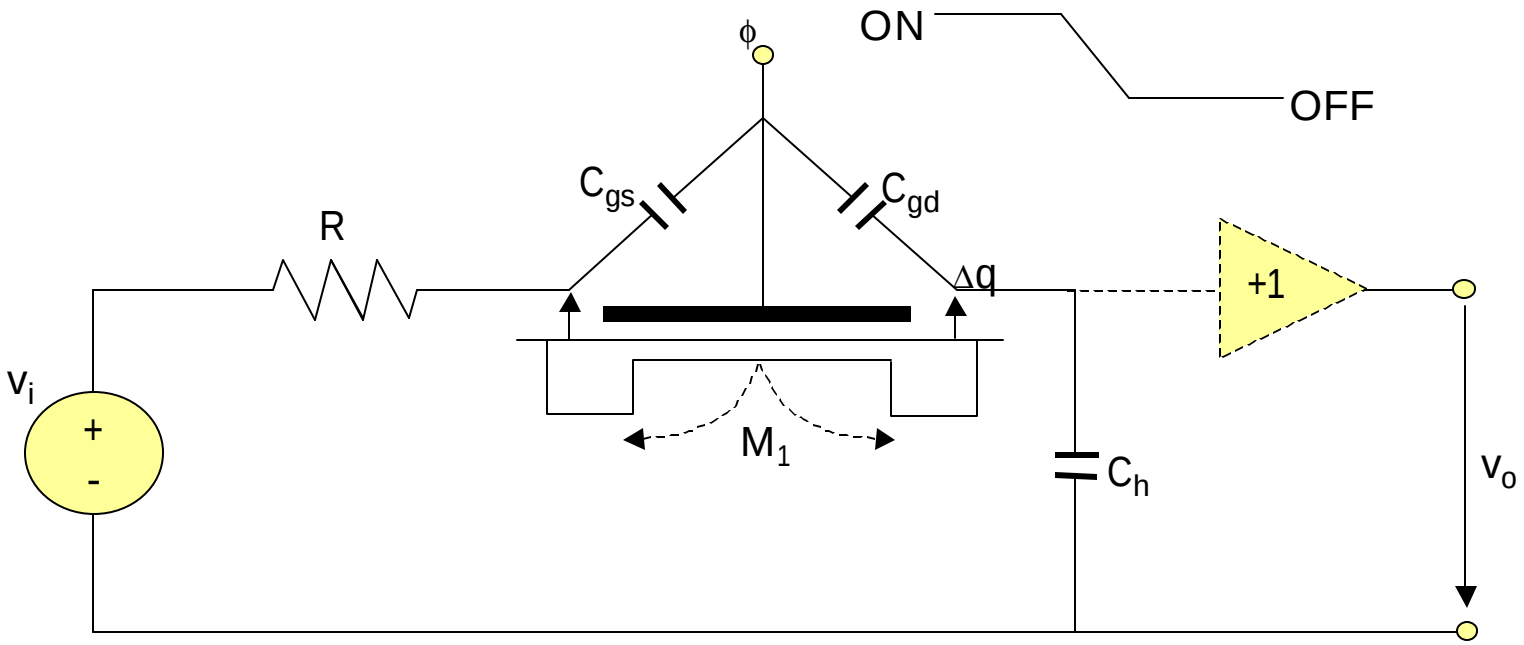
Improved S/H Circuit



Sample and Hold based on a Switched Op Amp

L.Dai and R. Harjani," CMOS Switched-Op-Amp Based Sample and Hold Circuit, IEEE JSSC, January 2000, pp 109-113

Charge injection and clock feedthrough mechanism

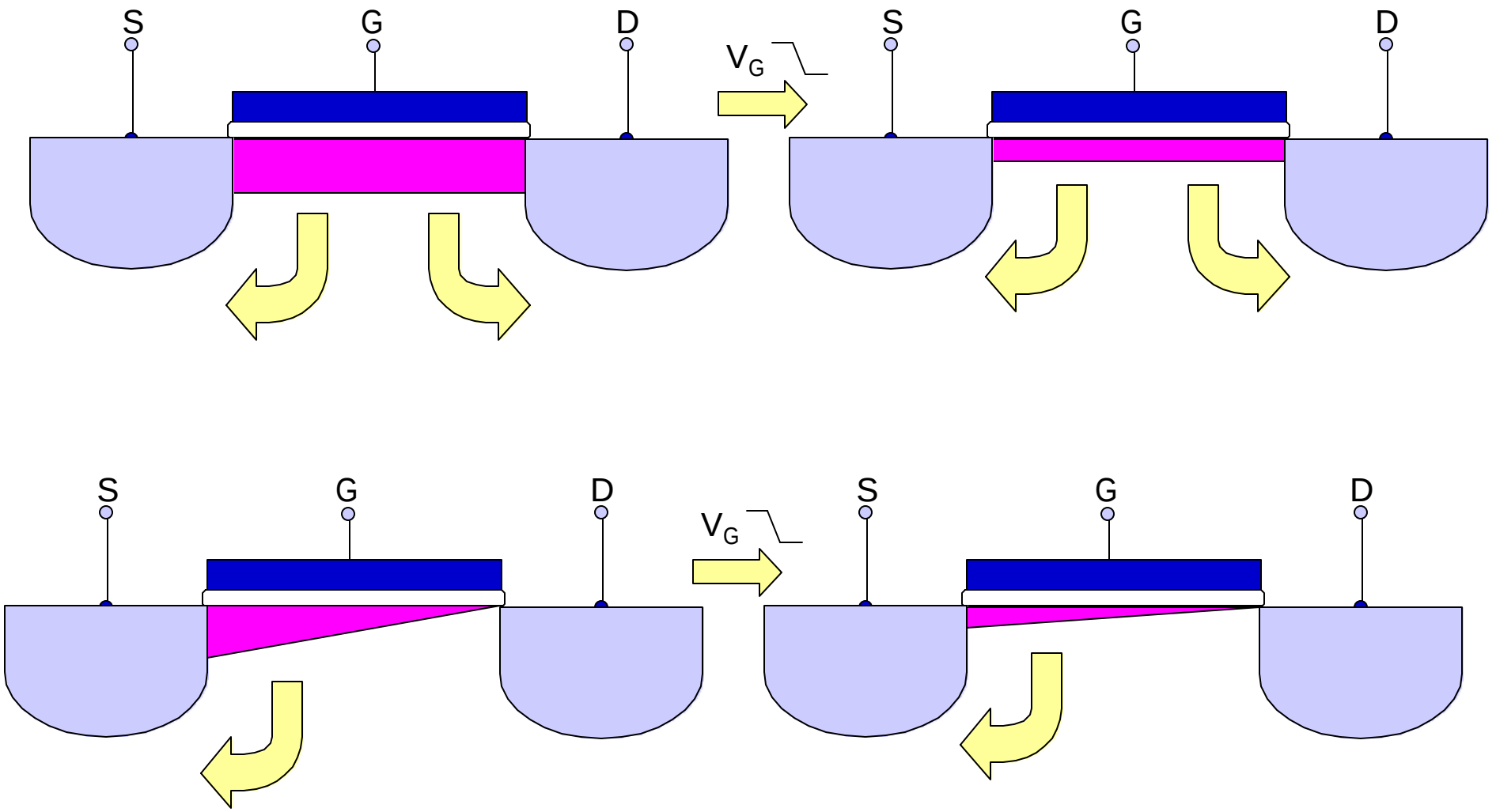


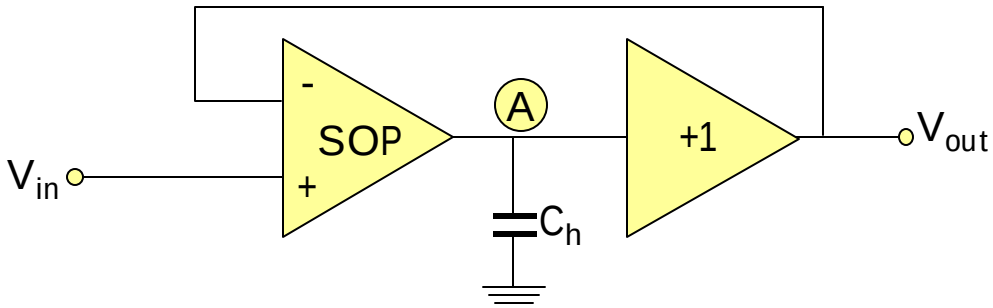
$$Q_{ch} = -WLC_{ox}(V_{GS} - V_T)$$

$$\Delta V' = \frac{k \cdot Q_{ch}}{C_h} = -\frac{kWLC_{ox}(V_{GS} - V_T)}{C_h}$$

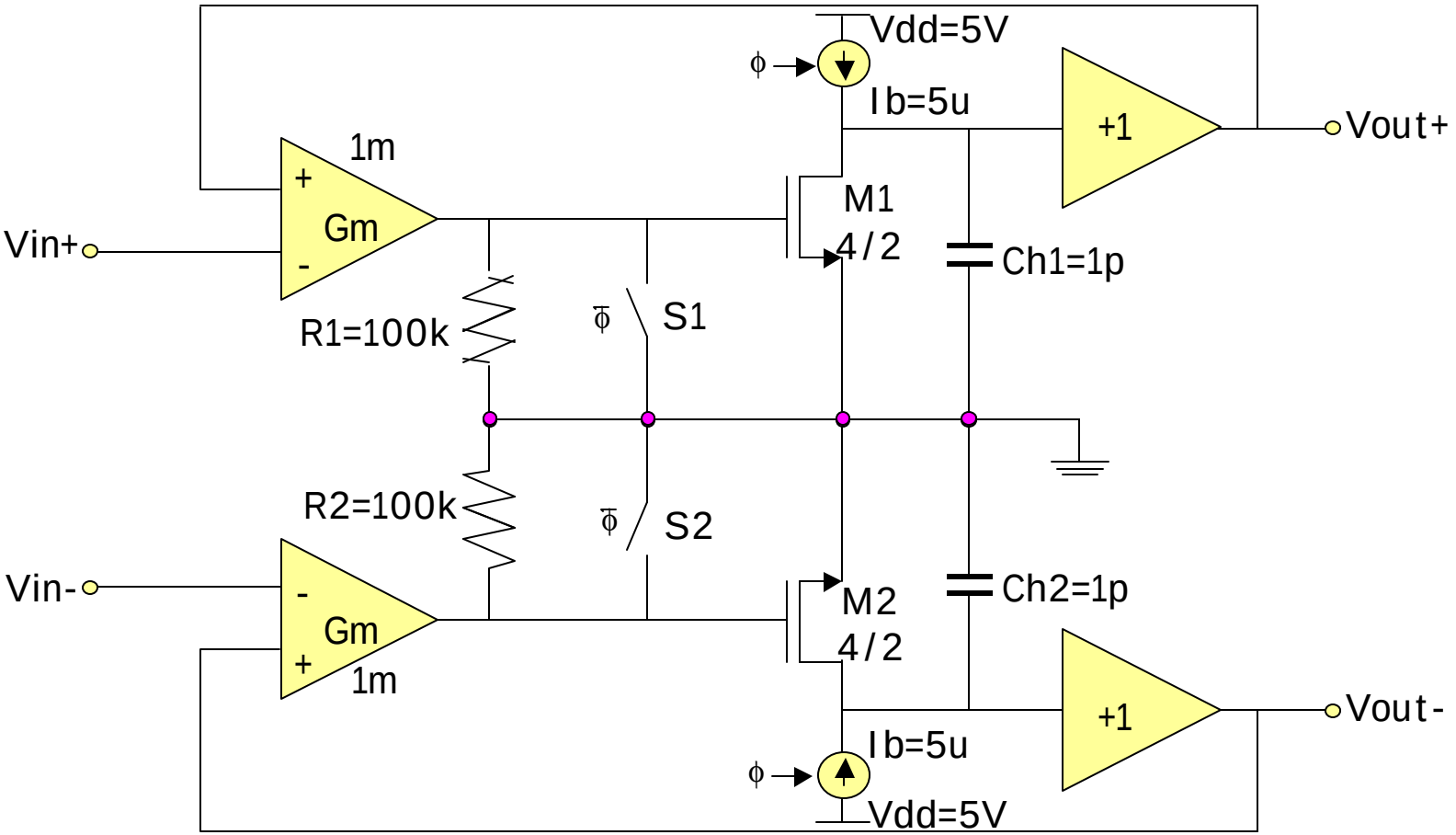
$$\Delta V'' = -\frac{(V_{DD} - V_{SS})C_{para}}{C_{para} + C_h}$$

Channel charge in (top) triode and (bottom) saturation



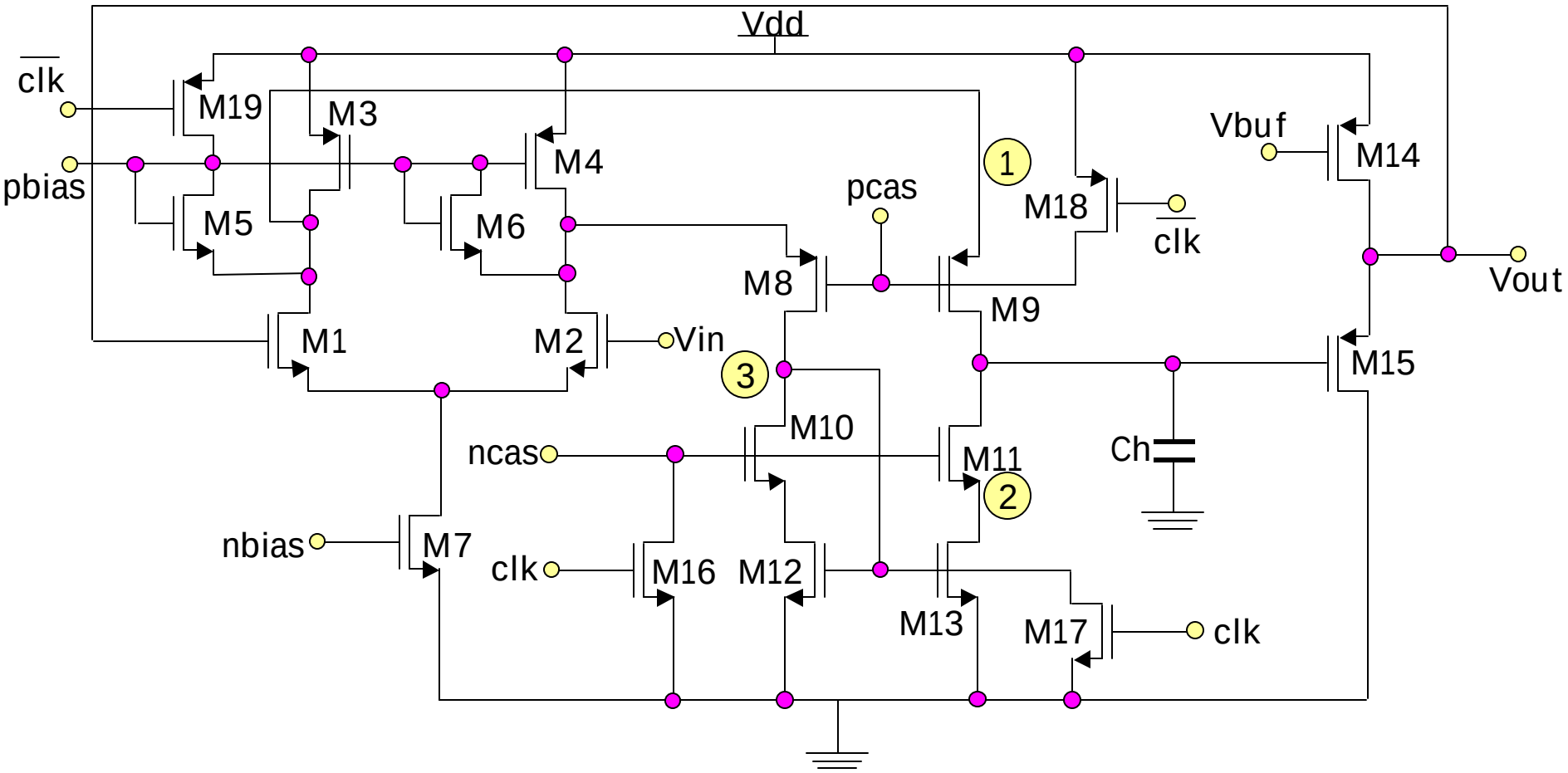


Switched-Op-Amp-Based S/H Circuit



Simplified model of the pseudo-differential SOP-based S/H

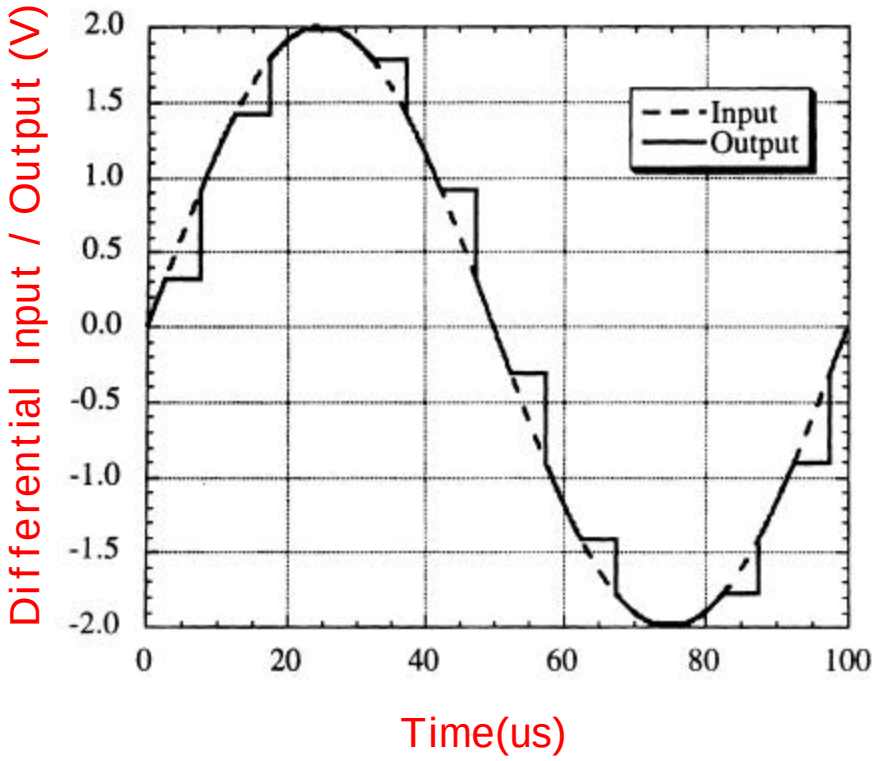
Folded cascode switched op-amp in the unity-gain feedback configuration



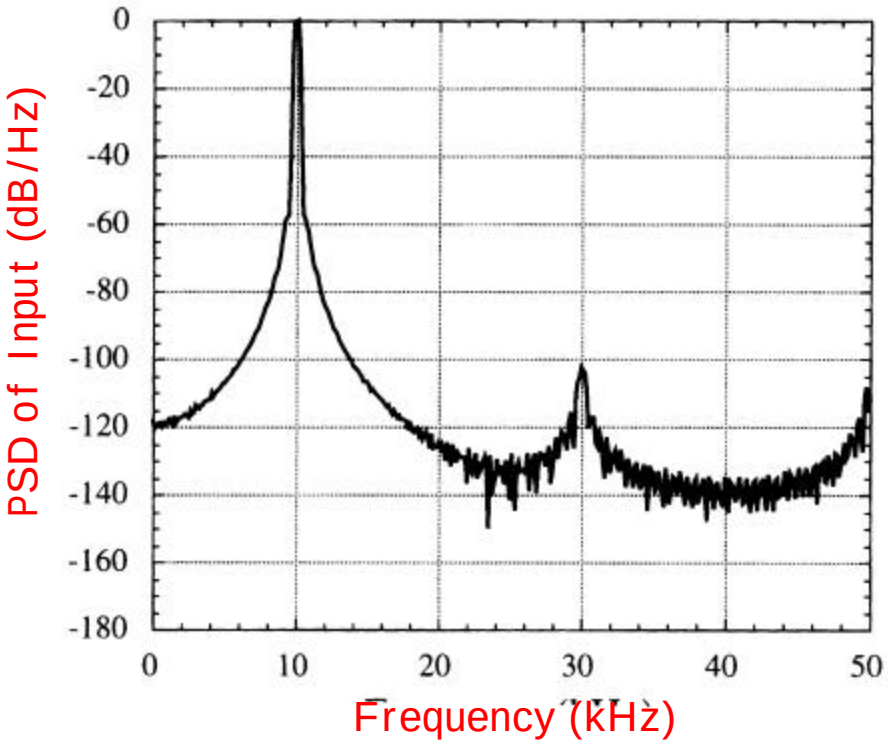
$$V_{Nerr} = -\frac{C_{Npara}}{C_h + C_{Npara}} V_{N_{GS}}$$

$$V_{Perr} = -\frac{C_{Ppara}}{C_h + C_{Ppara}} \left| V_{P_{GS}} \right|$$

Simulation results for a complete cycle of sampled-and-held waveform



Simulation results of the spectrum of the sampled-and-held waveform



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