Types of D/A Converters

	DAC Type	Advantage	Disadvantage
	Current Scaling	Fast, insensitive to switch parasitics	Large element spread, nonmonotonic
	Voltage Scaling	Monotonic, equal resistors	Large area, sensitive to parasitic capacitance
	Charge Scaling	Fast, good accuracy	Large element spread, nonmonotonic

Current Scaling D/As

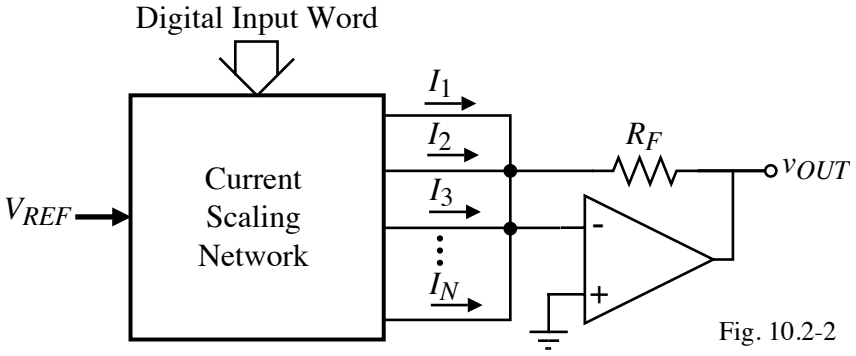


Fig. 10.2-2

The output voltage can be expressed as

$$V_{out} = R_f(I_1 + I_2 + I_3 + \ldots + I_N)$$

where the currents $I1, I2, I3, ...$
are binary weighted currents.

D/As built from R-2R Ladders

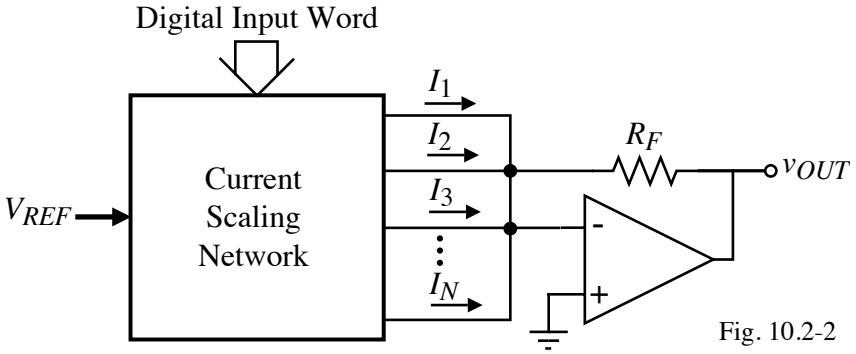
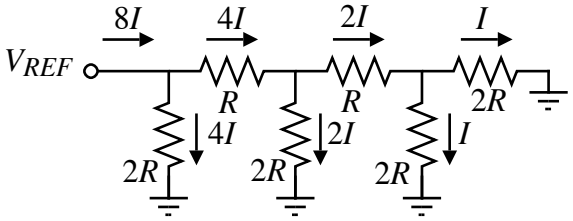


Fig. 10.2-2

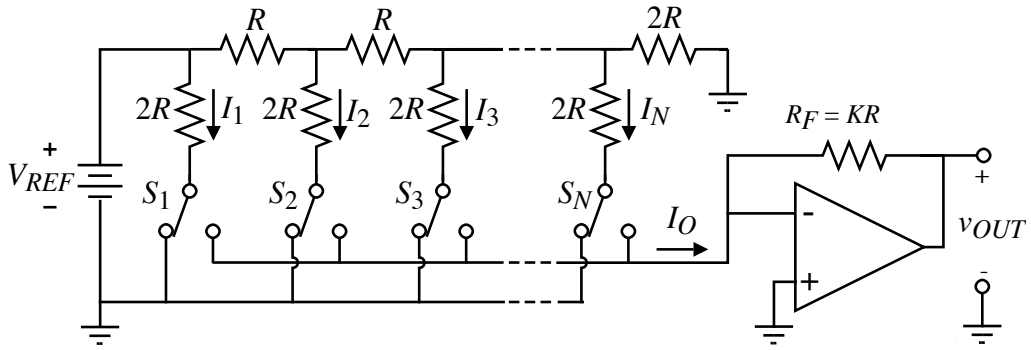
The output voltage can be expressed as

$$V_{out} = R_f(I_1 + I_2 + I_3 + \ldots + I_N)$$

where the currents $I1, I2, I3, \ldots$ are binary weighted currents.



"The resistance seen to the right of any of the vertical $2R$ resistors is $2R$."



Not monotonic

Current Scaling D/As

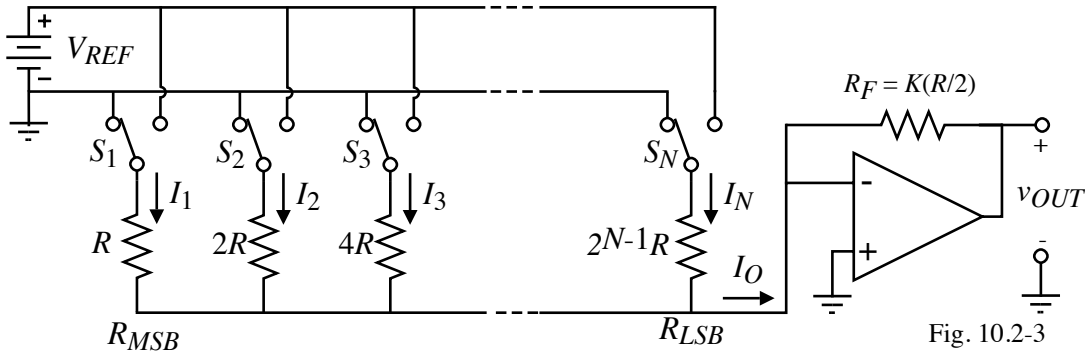


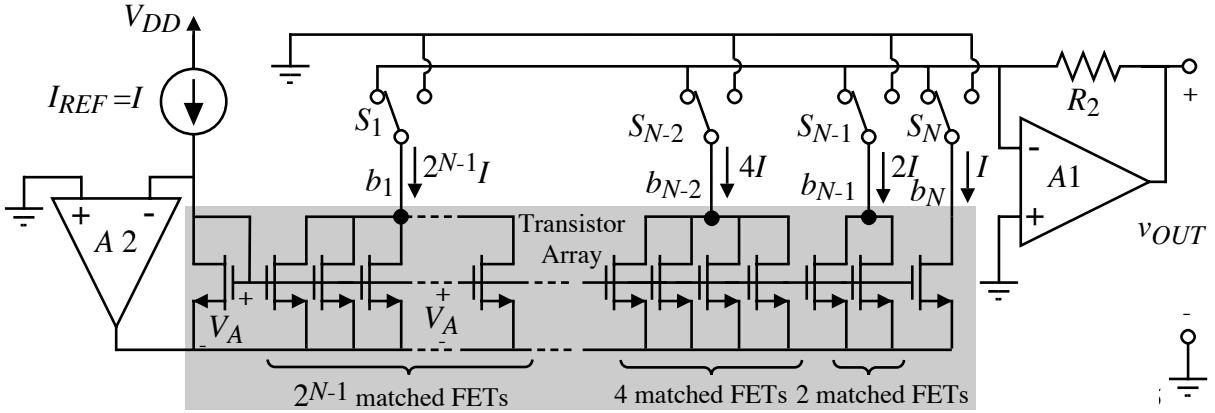
Fig. 10.2-3

The output voltage can be expressed as

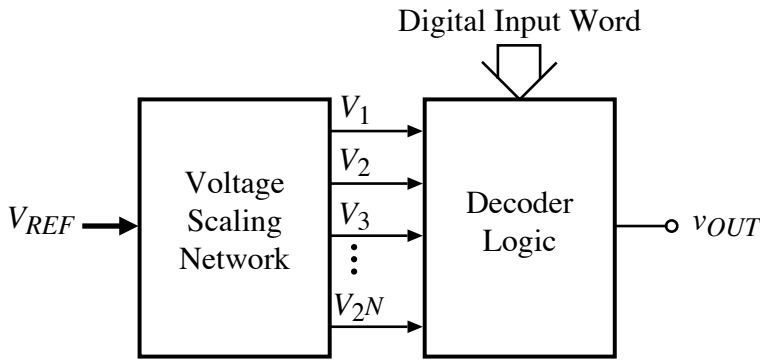
$$V_{out} = R_f(I_1 + I_2 + I_3 + \ldots + I_N)$$

where the currents $I1, I2, I3, \ldots$ are binary weighted currents.

Fast (no moving nodes) and not monotonic (mismatch)



Voltage Scaling D/As



Alternate Approach

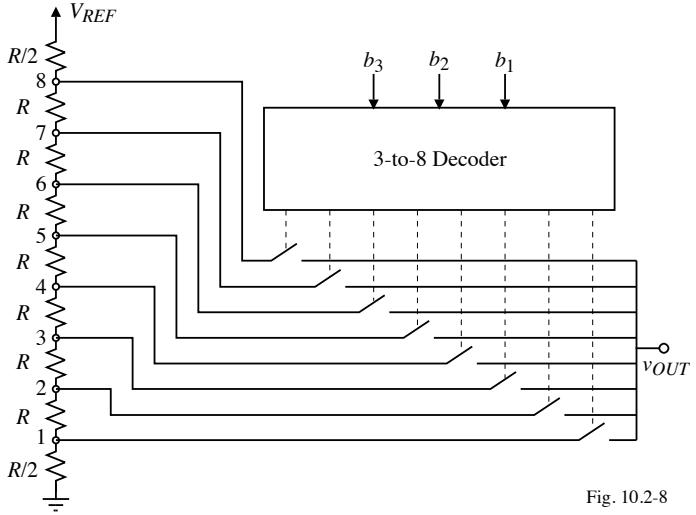
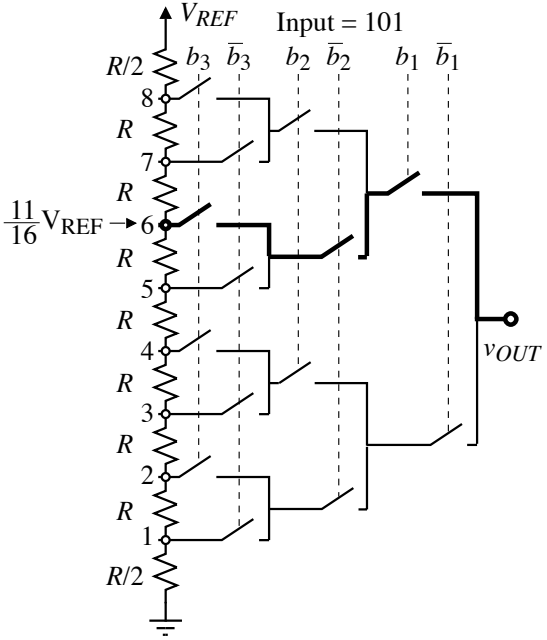
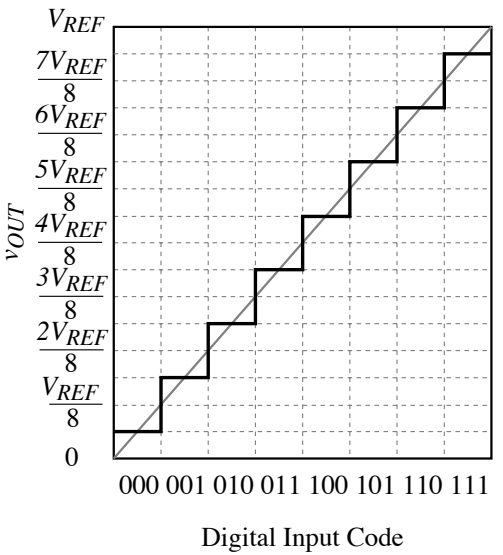


Fig. 10.2-8

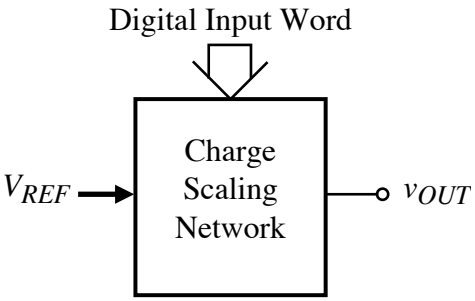
Typical Approach

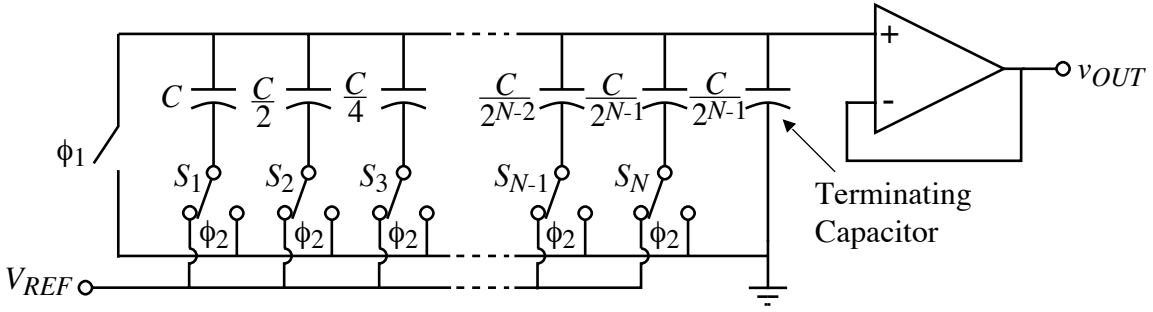




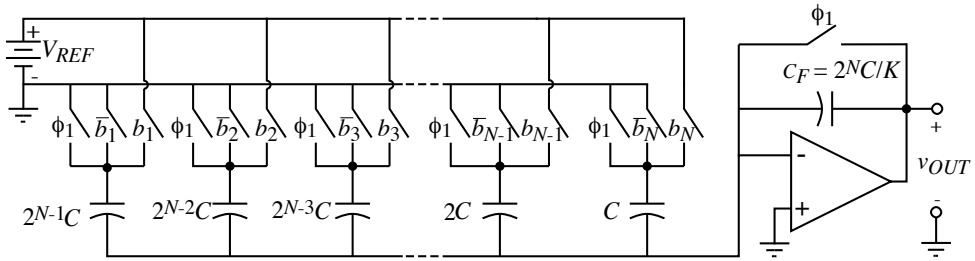
- Guaranteed monotonic,
- Compatible with CMOS technology,
- Large area if *N* is large,
- Sensitive to parasitics,
- Requires a buffer,
- Large current can flow through the resistor string.

Charge Based D/A Converters





Based on capacitor matching (not monotonic)
Charge feedthrough and parasitic issues



No moving nodes
- insensitive to parasitics
  (parasitic-insensitive switched capacitor circuitry)
- fast

Can not eliminate charge feedthrough

Improving D/A Performance

Divide the total resolution *N* into *k* smaller sub-DACs.

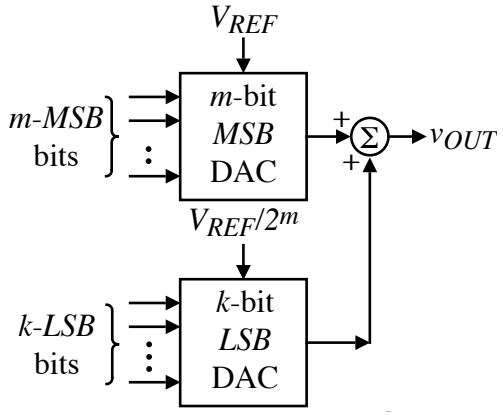
- Smaller total area.
- More resolution (reduced largest to smallest component spread)

So how do we do this?

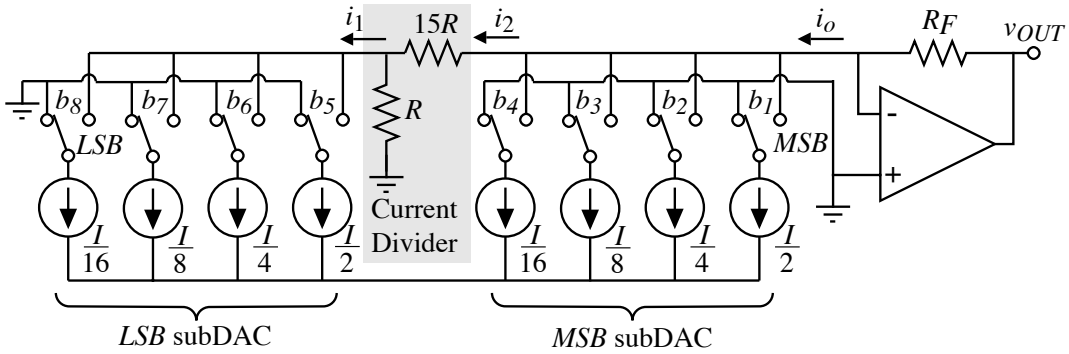
- Combination of similarly scaled subDACs
  - Divider approach (scale the analog output of the subDACs)
  - Subranging approach (scale the reference voltage of the subDACs)

- Combination of differently scaled subDACs

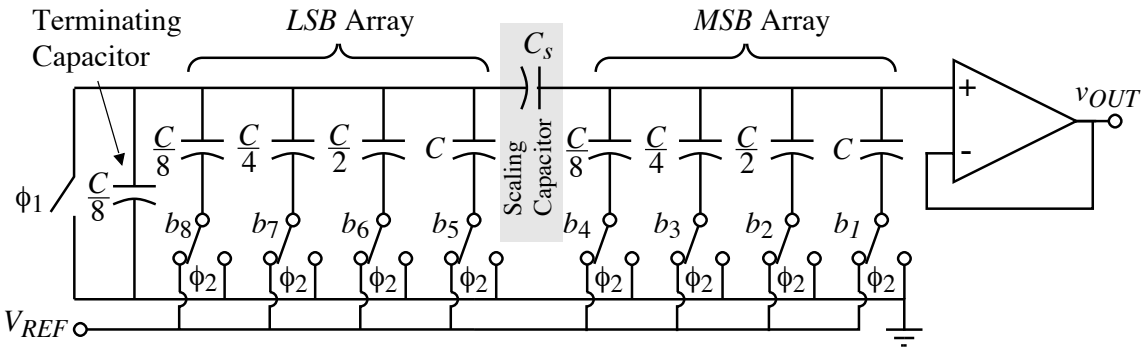
Subranging Converters

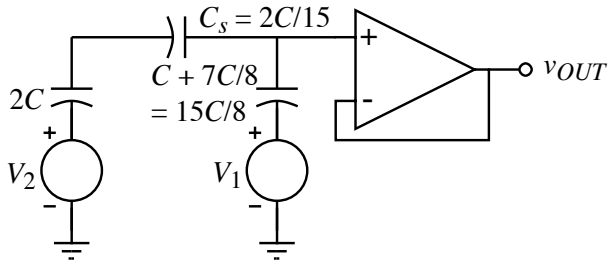


Current DAC



Charge DAC





D/A Based on Two Charge Amps

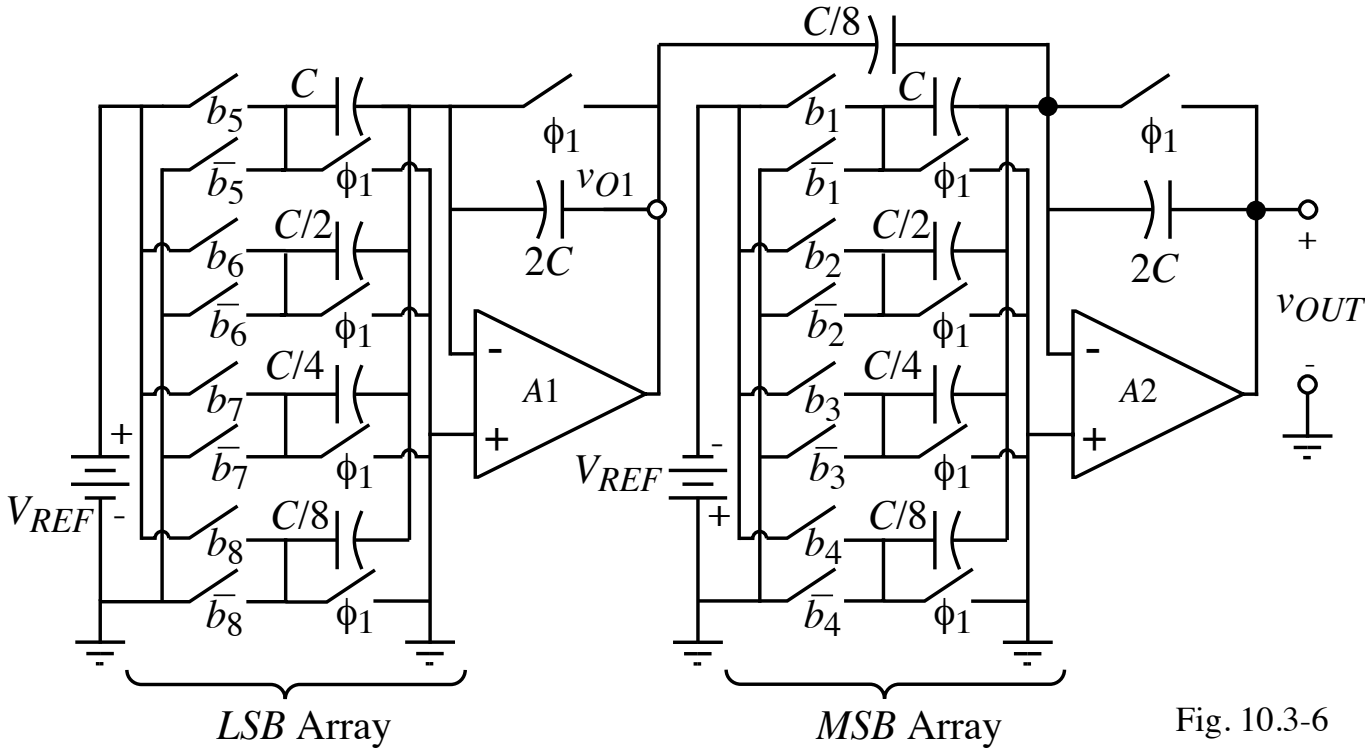
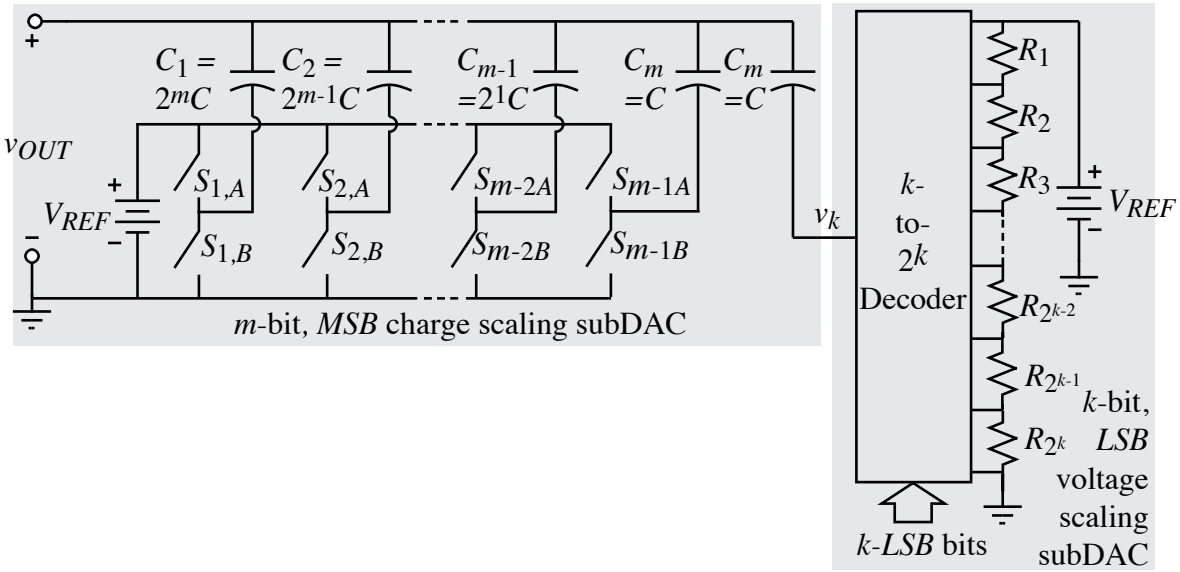


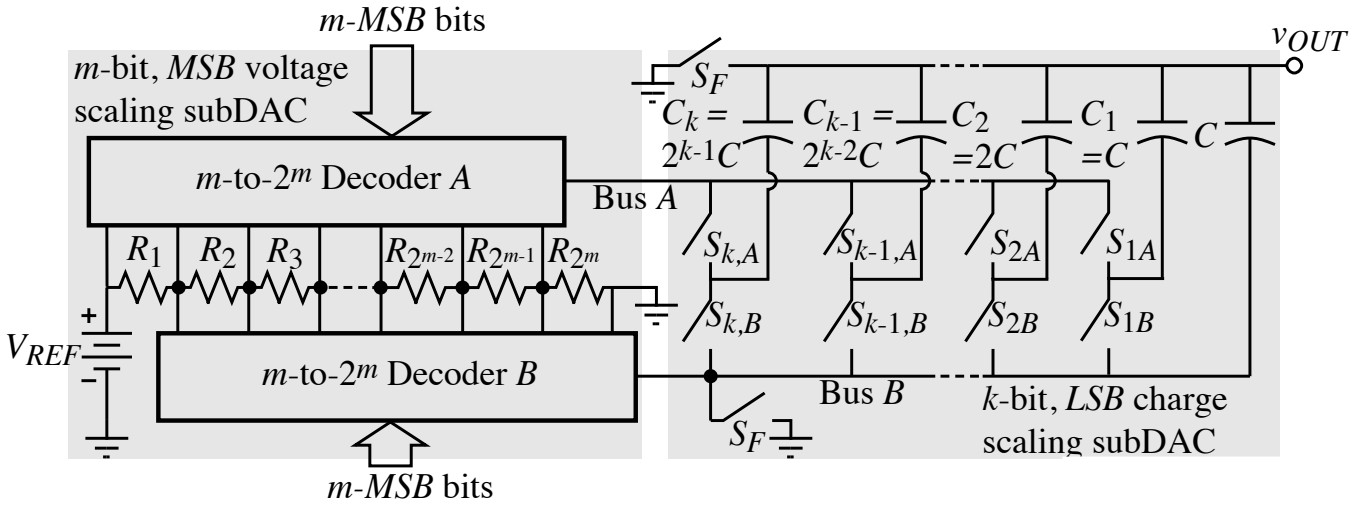
Fig. 10.3-6

- *MSB* subDAC is not dependent upon the accuracy of the scaling factor for the *LSB* subDAC.
- Insensitive to parasitics, fast
- Limited to op amp dynamics

Combining Unique SubDACs

MSB: Charge Scaling
(high # of bits)
LSB: Voltage Scaling
(monotonic)





LSB: Charge Scaling
(high # of bits)
MSB: Voltage Scaling
(monotonic)

Summary of D/A Converters

DAC	Figure	Primary Advantage	Primary Disadvantage
Current-scaling, binary weighted resistors	10.2-3	Fast, insensitive to parasitic capacitance	Large element spread, nonmonotonic
Current-scaling, R-2R ladder	10.2-4	Small element spread, increased accuracy	Nonmonotonic, limited to resistor accuracy
Current-scaling, active devices	10.2-5	Fast, insensitive to switch parasitics	Large element spread, large area
Voltage-scaling	10.2-7	Monotonic, equal resistors	Large area, sensitive to parasitic capacitance
Charge-scaling, binary weighted capacitors	10.2-10	Best accuracy	Large area, sensitive to parasitic capacitance
Binary weighted, charge amplifier	10.2-12	Best accuracy, fast	Large element spread, large area
Current-scaling subDACs using current division	10.3-3	Minimizes area, reduces element spread which enhances accuracy	Sensitive to parasitic capacitance, divider must have ±0.5*LSB* accuracy
Charge-scaling subDACs using charge division	10.3-4	Minimizes area, reduces element spread which enhances accuracy	Sensitive to parasitic capacitance, slower, divider must have ±0.5*LSB* accuracy
Binary weighted charge amplifier subDACs	10.3-6	Fast, minimizes area, reduces element spread which enhances accuracy	Requires more op amps, divider must have ±0.5*LSB* accuracy
Voltage-scaling (*MSBs*), charge-scaling (*LSBs*)	10.3-7	Monotonic in *MSBs*, minimum area, reduced element spread	Must trim or calibrate resistors for absolute accuracy
Charge-scaling (*MSBs*), voltage-scaling (*LSBs*)	10.3-8	Monotonic in *LSBs*, minimum area, reduced element spread	Must trim or calibrate resistors for absolute accuracy
Serial, charge redistribution	10.4-1	Simple, minimum area	Slow, requires complex external circuits
Pipeline, algorithmic	10.4-3	Repeated blocks, output at each clock after *N* clocks	Large area for large number of bits
Serial, iterative algorithmic	10.4-4	Simple, one precise set of components	Slow, requires additional logic circuitry