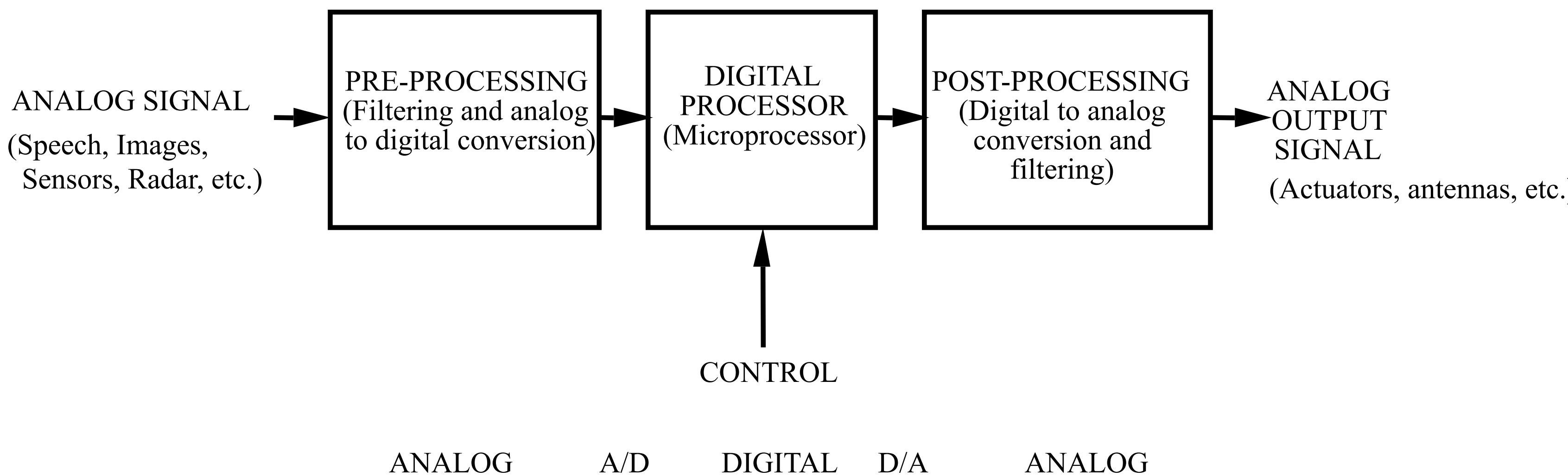
The need for Data Converters



In many applications, performance is critically limited by the A/D and D/A performance

D/A Block Diagram

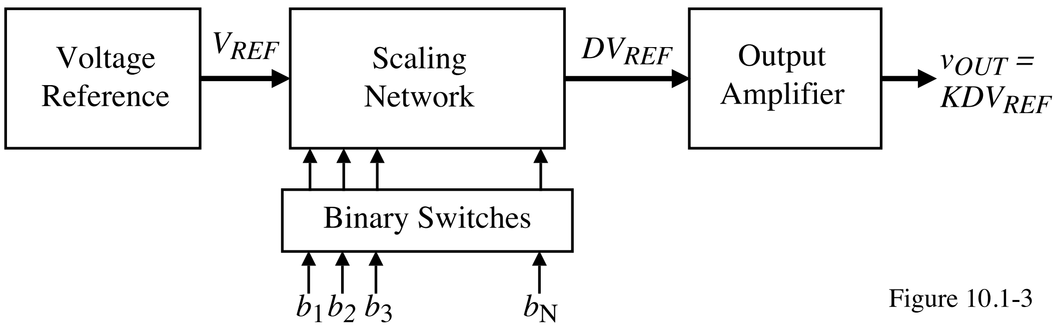


Figure 10.1-3

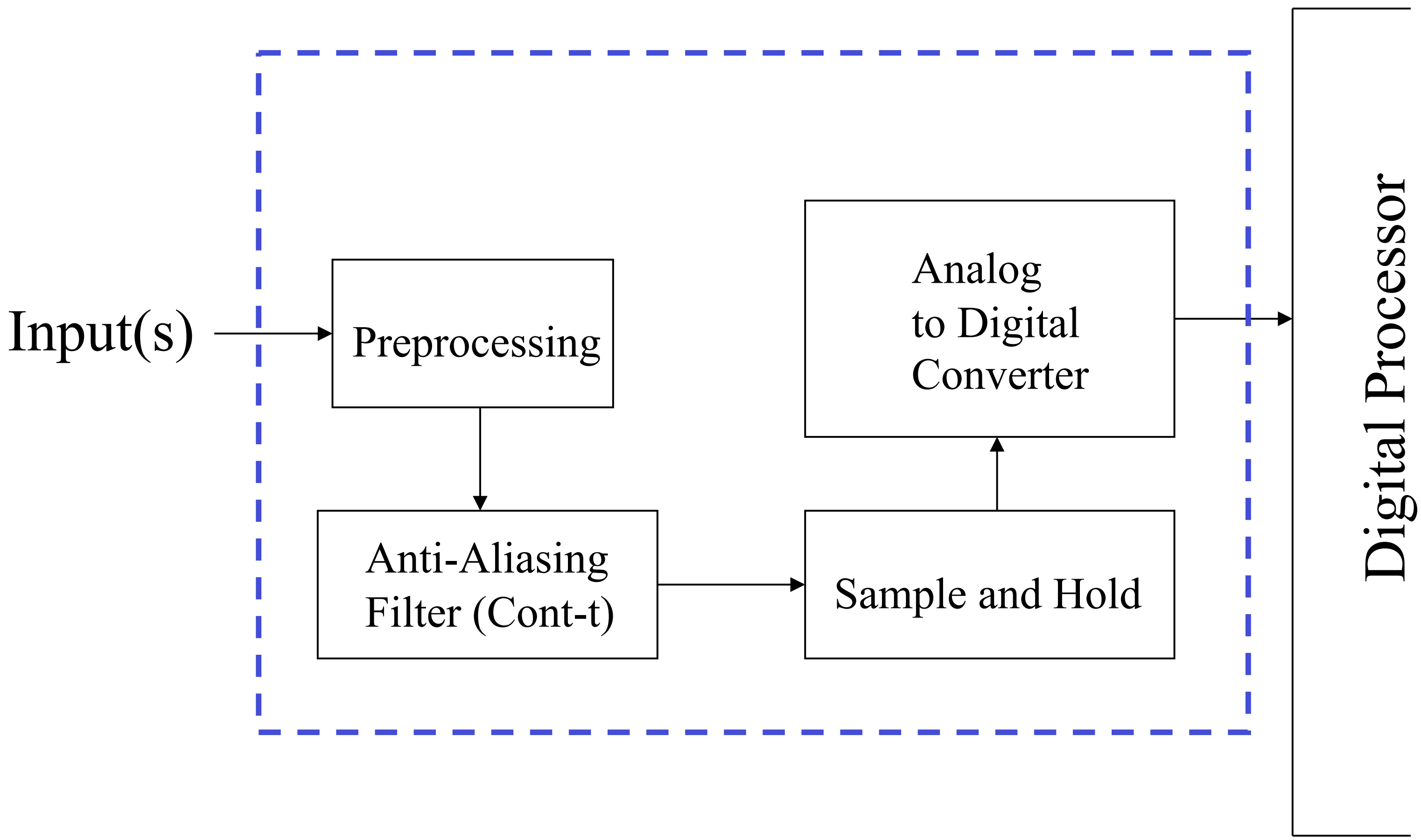
*b*1 is the most significant bit (MSB)

The MSB is the bit that has the most (largest) influence on the analog output

bN is the least significant bit (LSB)

The LSB is the bit that has the least (smallest) influence on the analog output

Where the A/D is in the System



Sometimes the "Digital Processor" does part of the Conversion

Types of A/D Converters

	Conversion Rate	Nyquist ADCs	Oversampled ADCs
	Slow	Integrating (Serial)	Very high resolution >14 bits
	Medium	Successive Approximation 1-bit Pipeline Algorithmic	Moderate resolution >10 bits
	Fast	Flash Multiple-bit Pipeline Folding and interpolating	Low resolution > 6 bits

Ideal input-output characteristics of a 3-bit DAC

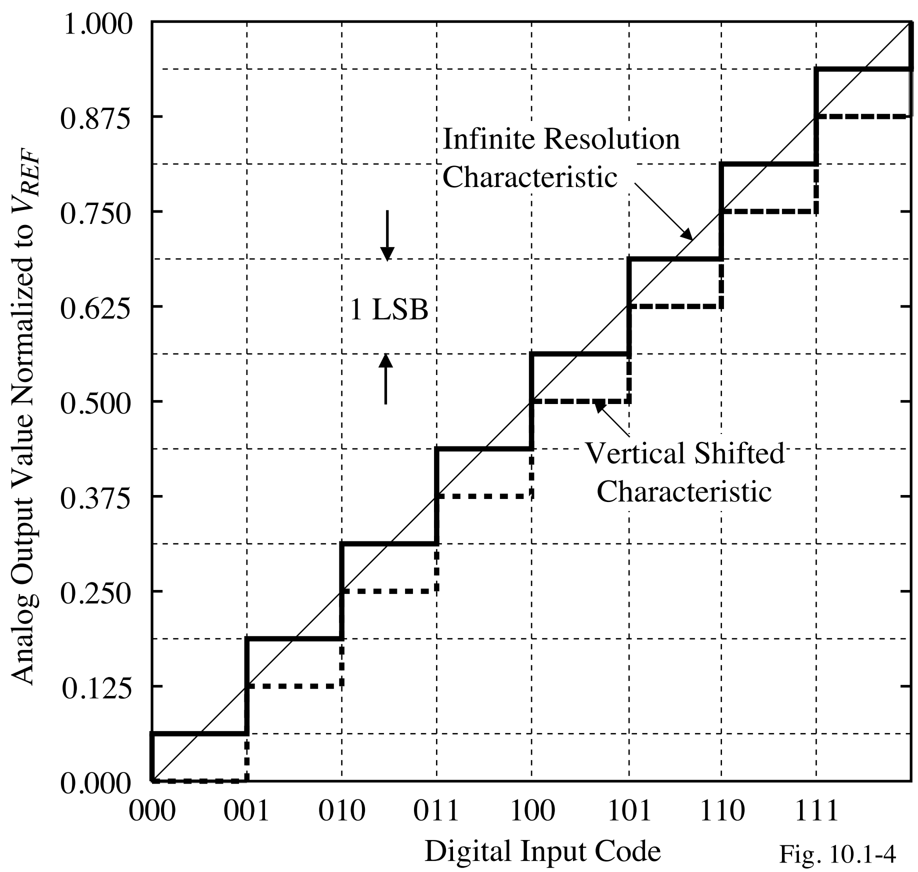


Fig. 10.1-4

D/A Definitions

Resolution of the DAC is equal to the number of bits in the applied digital input word.

Quantization Noise is the inherent uncertainty in digitizing an analog value with a finite resolution converter.

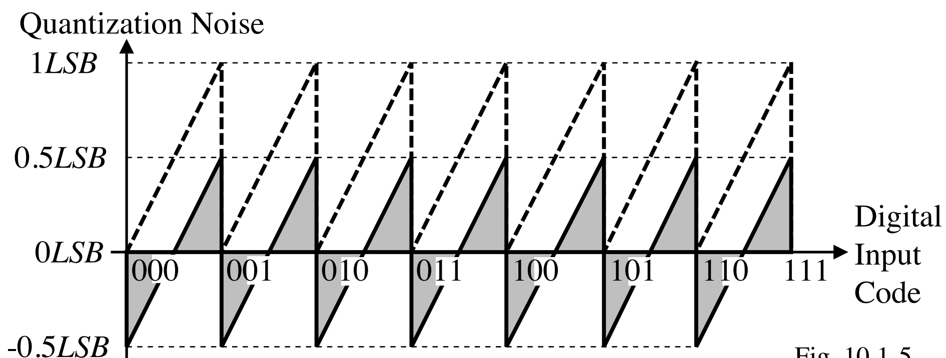


Fig. 10.1-5

A/D Definitions

The *dynamic range, signal-to-noise ratio (SNR)*, and the *effective number of bits (ENOB)* of the ADC are the same as for the DAC

Resolution of the ADC is the smallest analog change that can be distinguished by an ADC.

Quantization Noise is the $\pm 0.5LSB$ uncertainty between the infinite resolution characteristic and the actual characteristic.

Ideal input-output characteristics of a 3-bit ADC

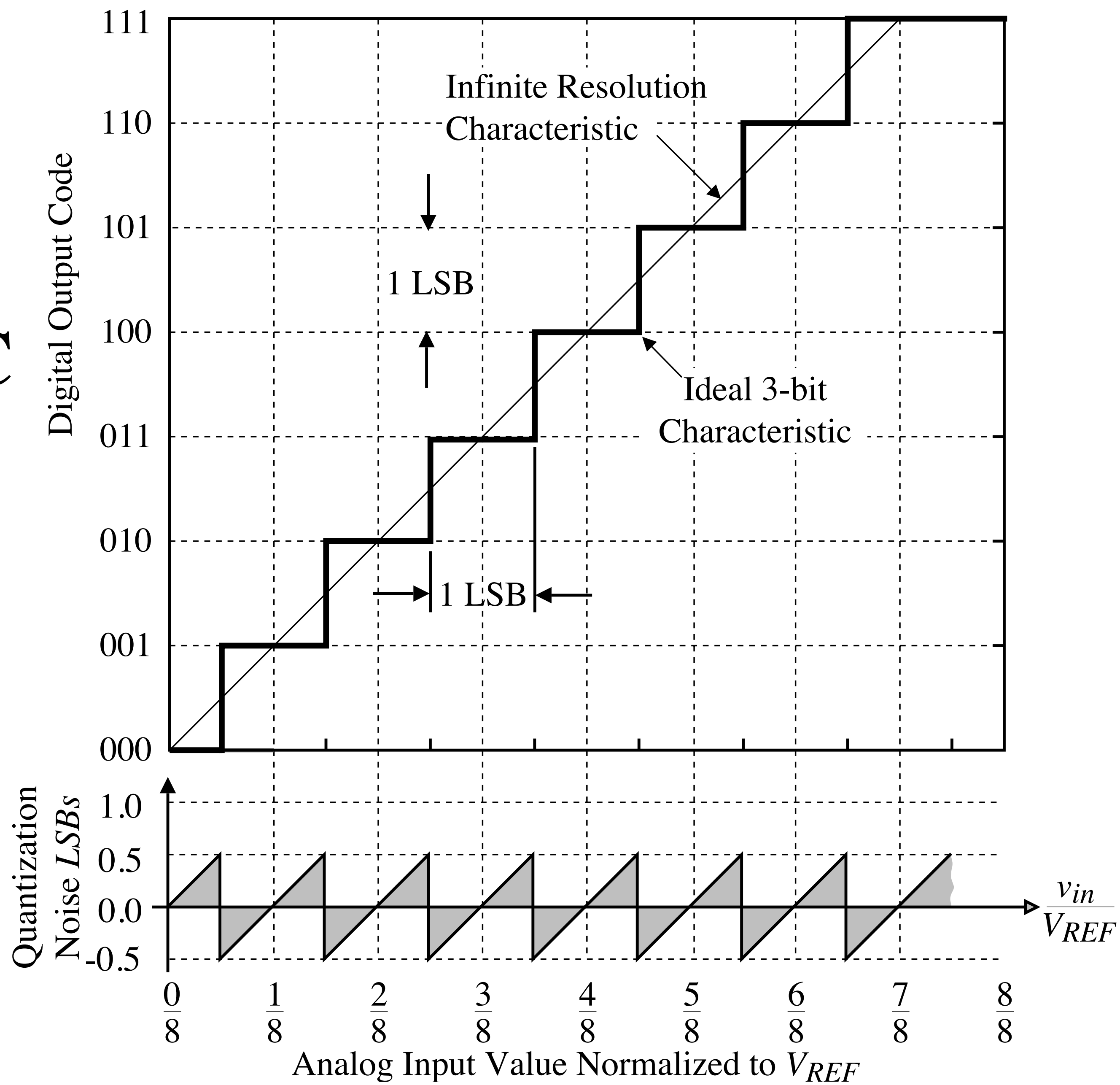


Table 10.5-2 - Digital Output Codes used for ADCs

Types of Encodings in A/Ds

Decimal	Binary	Thermometer	Gray	Two's Complement
0	000	0000000	000	000
1	001	0000001	001	111
2	010	0000011	011	110
3	011	0000111	010	101
4	100	0001111	110	100
5	101	0011111	111	011
6	110	0111111	101	010
7	111	1111111	100	001

Testing of D/A Converters

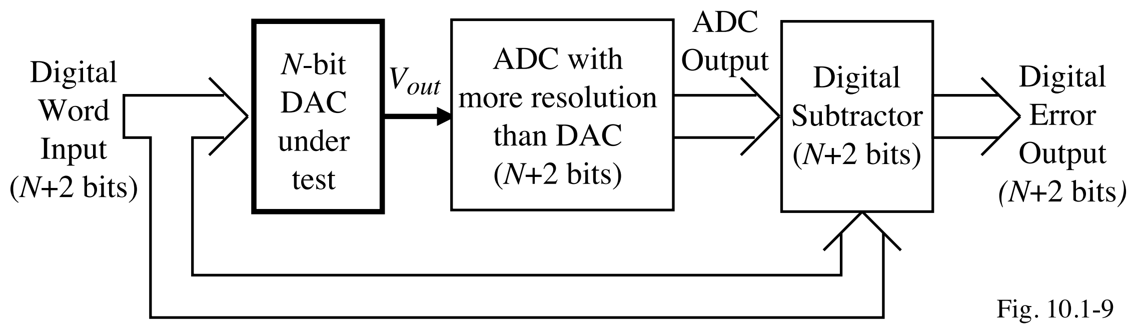


Fig. 10.1-9

Sweep the digital input word from 000...0 to 111...1.

The ADC should have more resolution by at least 2 bits
and be more accurate than the errors of the DAC

INL will show up in the output as the presence of 1's in any bit.
If there is a 1 in the Nth bit, the *INL* is greater than ±0.5*LSB*

DNL will show up as a change between each successive digital error output.

The bits which are greater than *N* in the digital error output
can be used to resolve the errors to less than ±0.5*LSB*

Testing of an A/D Converter

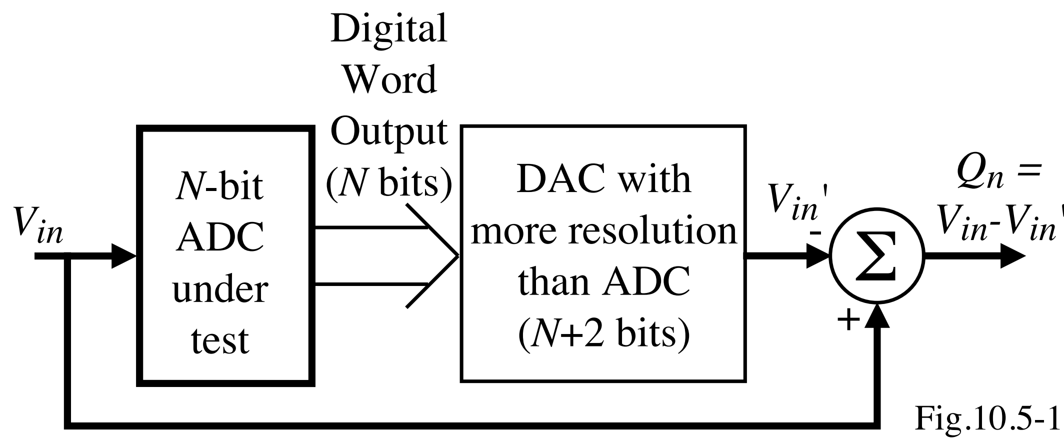


Fig.10.5-17

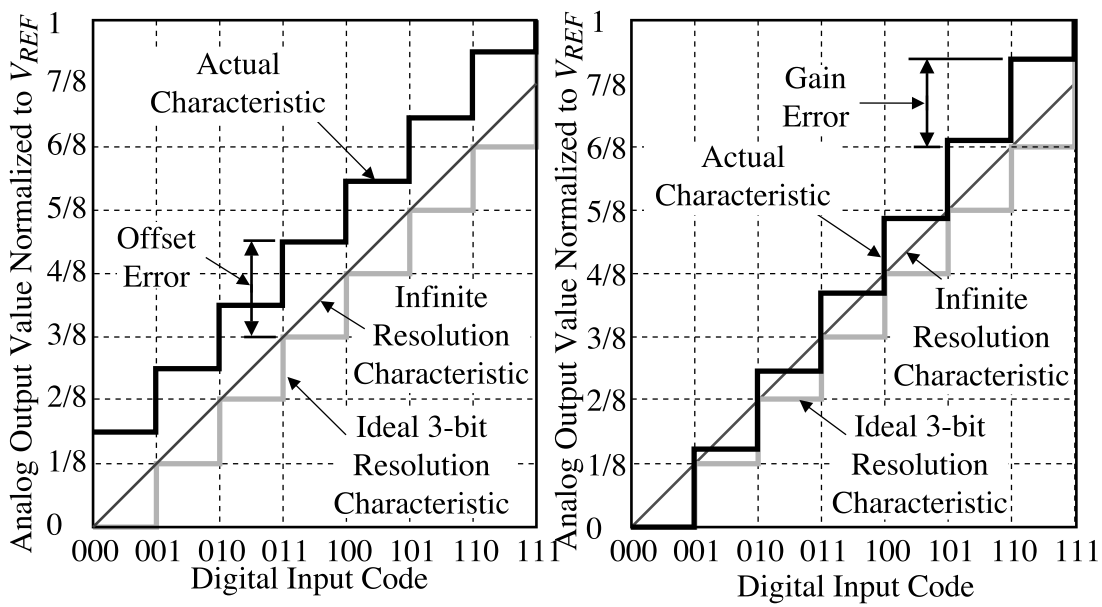
The ideal value of *Qn* should be within ±0.5*LSB*

Can measure:

- Offset error = constant shift above or below the 0 *LSB* line
- Gain error = contant increase or decrease of the sawtooth plot as *Vin* is increased
- *INL* and *DNL*

Offset and Gain Errors in D/As

An *offset error* is a constant difference between
the actual finite resolution characteristic and
the infinite resolution characteristic measured at any vertical jump.



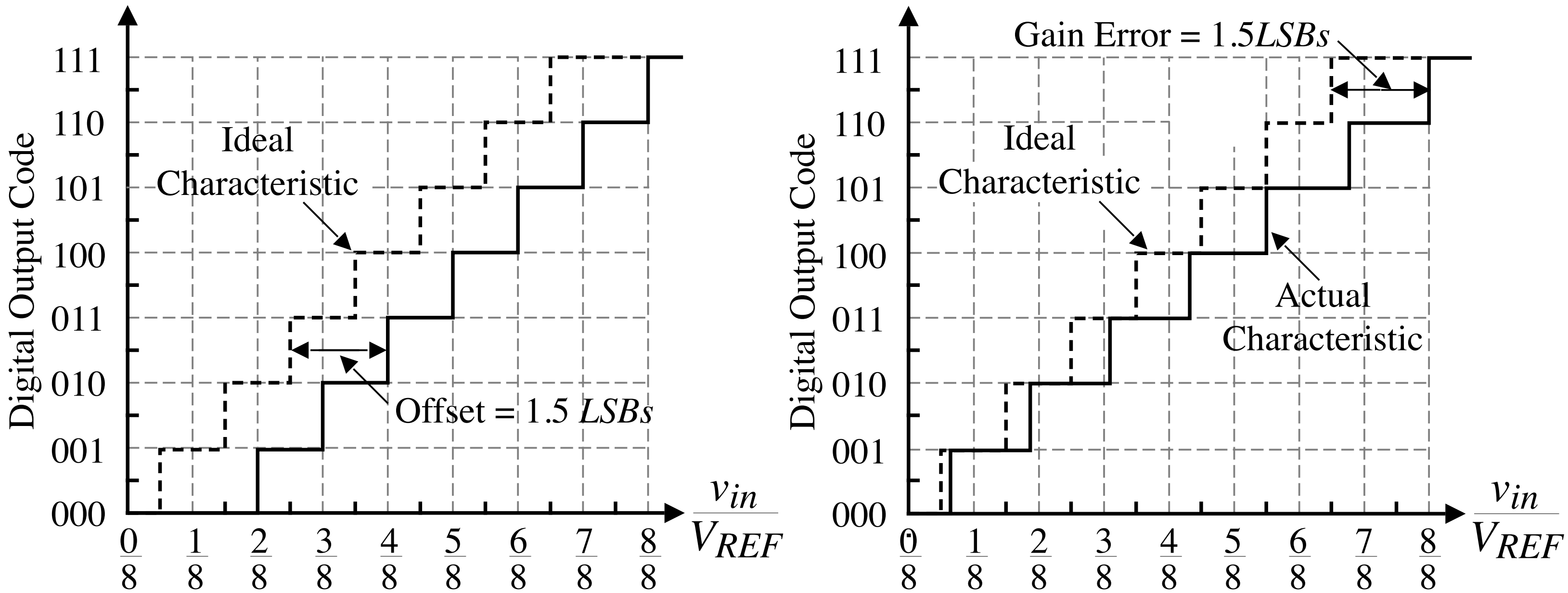
Offset Error in a 3-bit DAC

Gain Error in a 3-bit DAC

Fig. 10.1-6

A *gain error* is the difference between
the slope of an actual finite resolution and
an infinite resolution characteristic measured at the right-most vertical jump.

Offset and Gain Errors in A/Ds



Offset Error is the horizontal difference between the ideal finite resolution characteristic and actual finite resolution characteristic

Gain Error is the horizontal difference between the ideal finite resolution characteristic and actual finite resolution characteristic which is *proportional* to the analog input voltage.

Monotonicity

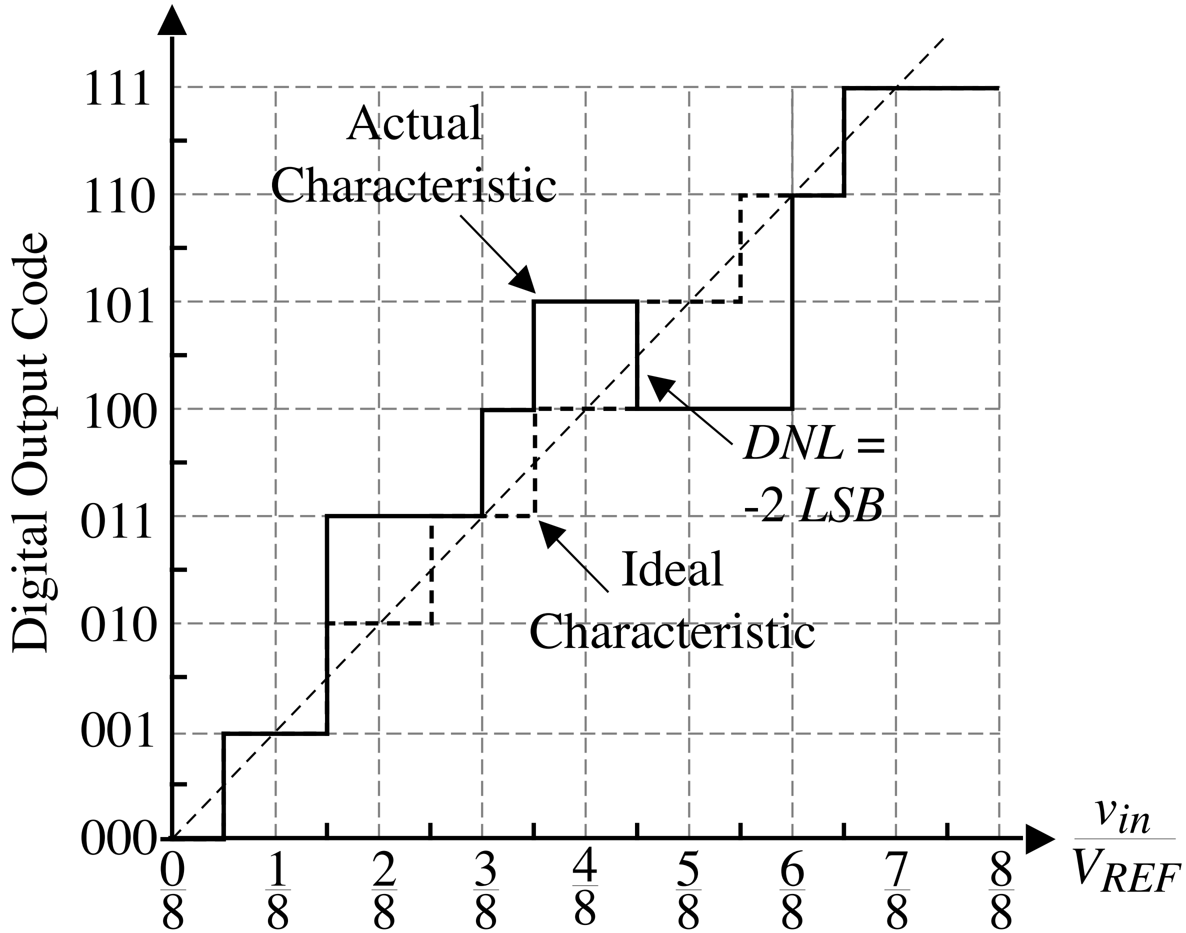


Fig. 10.5-6L

INL and DNL for a D/A

Integral Nonlinearity (*INL*) is
the maximum difference between
the actual finite resolution characteristic
& the **ideal** finite resolution characteristic
measured vertically (% or *LSB*).

Differential Nonlinearity (*DNL*) is
a measure of the separation between
adjacent levels measured
at each vertical jump (% or *LSB*).

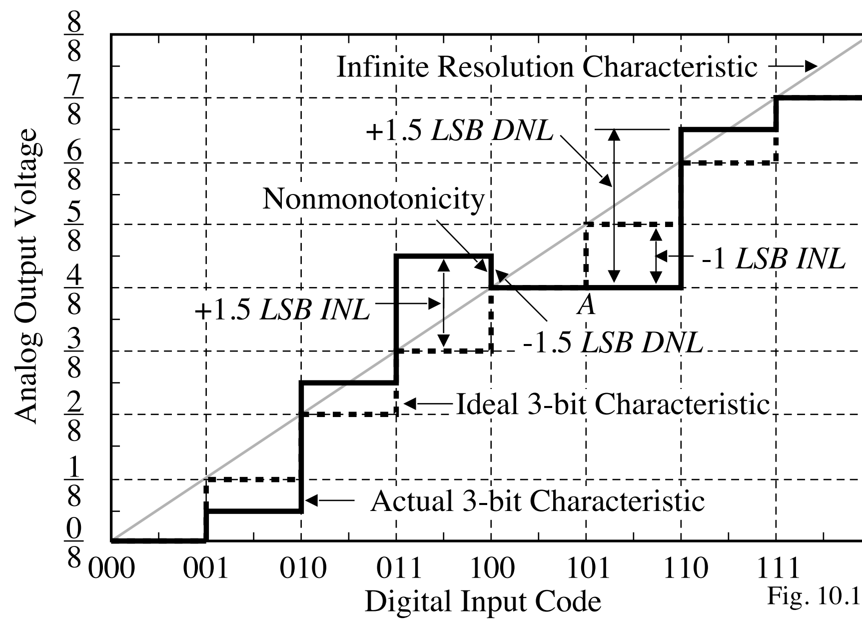


Fig. 10.1-7

Example of INL and DNL of a Nonideal 4-bit DAC

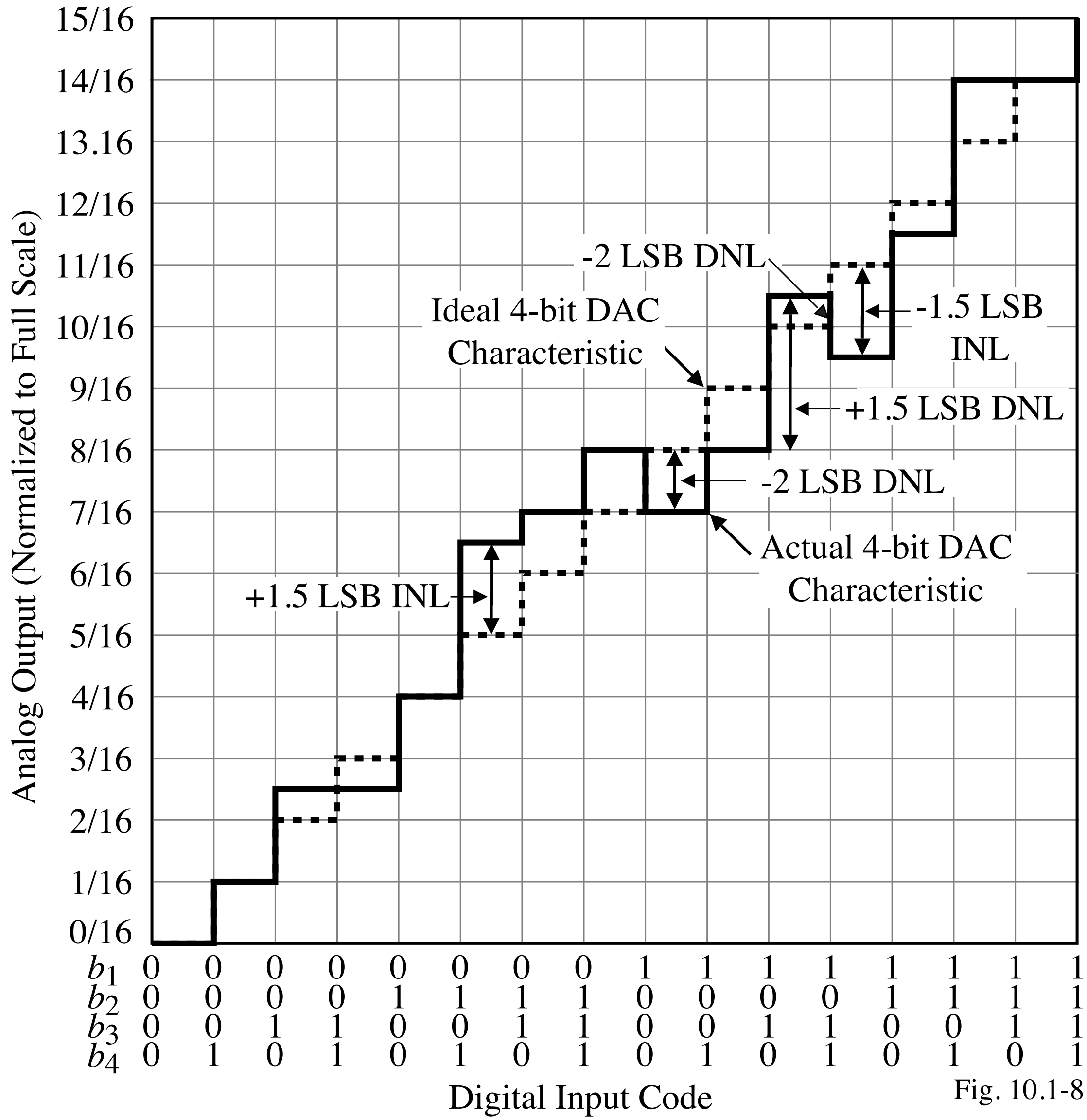


Fig. 10.1-8

INL and *DNL* of a 3-bit ADC

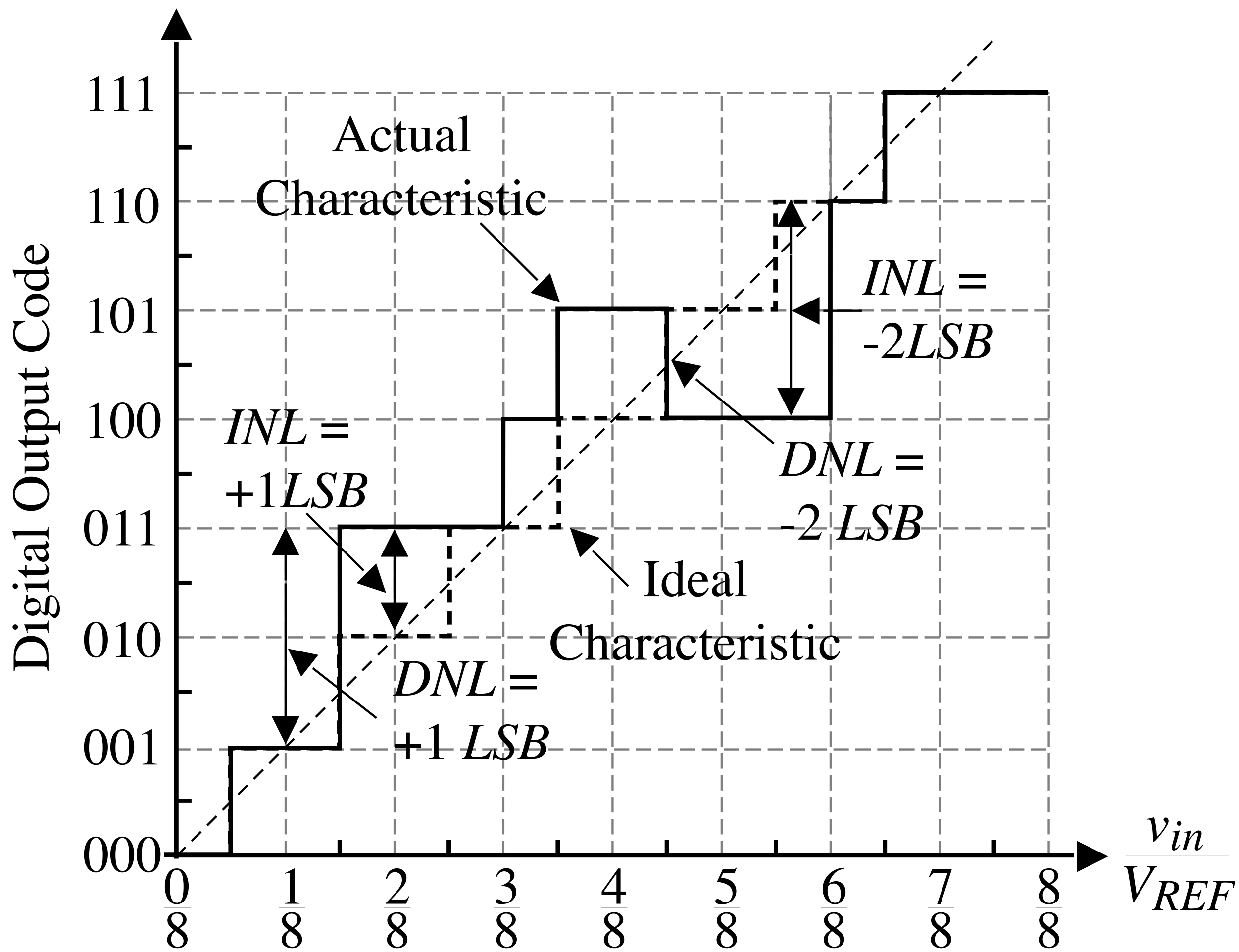
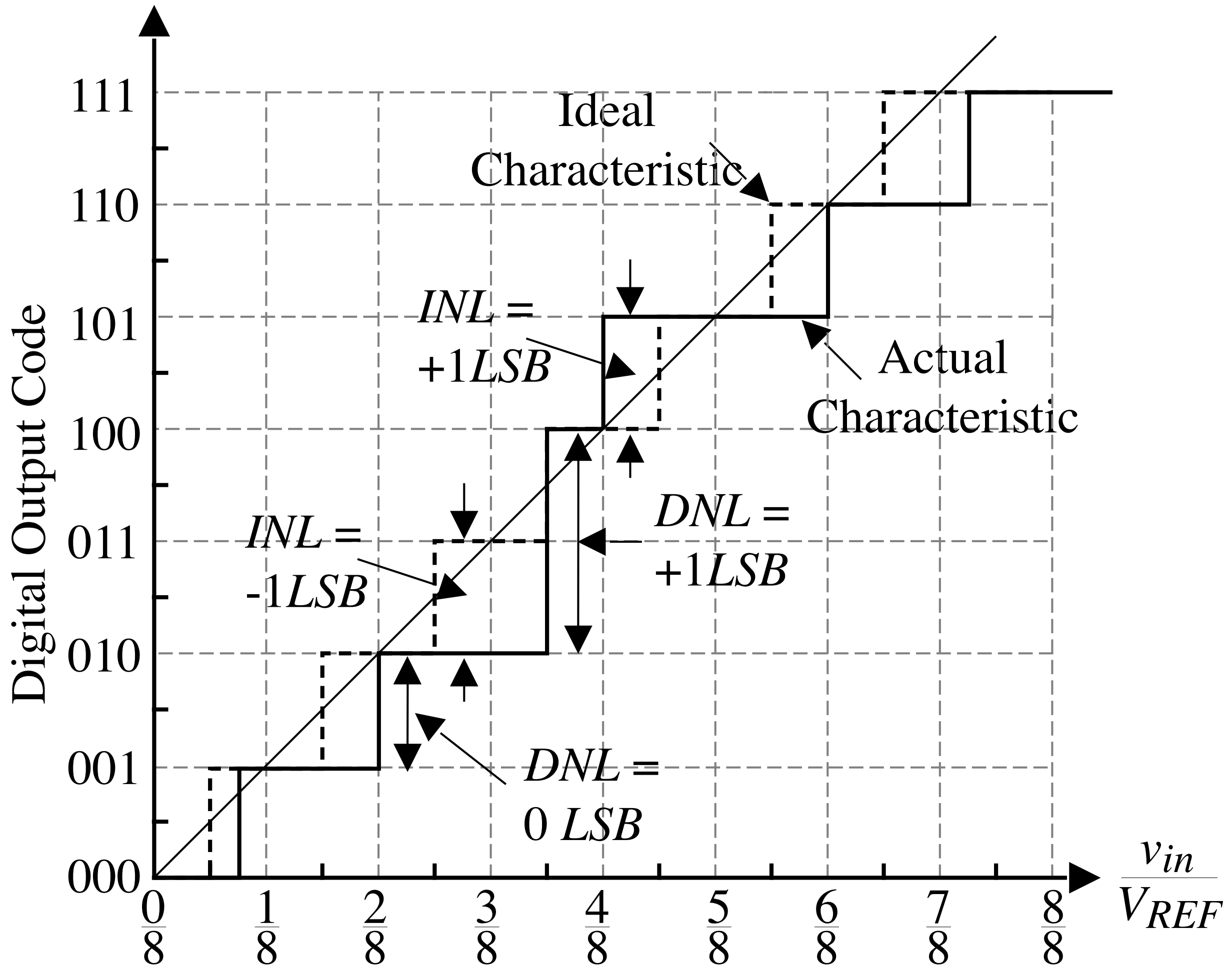


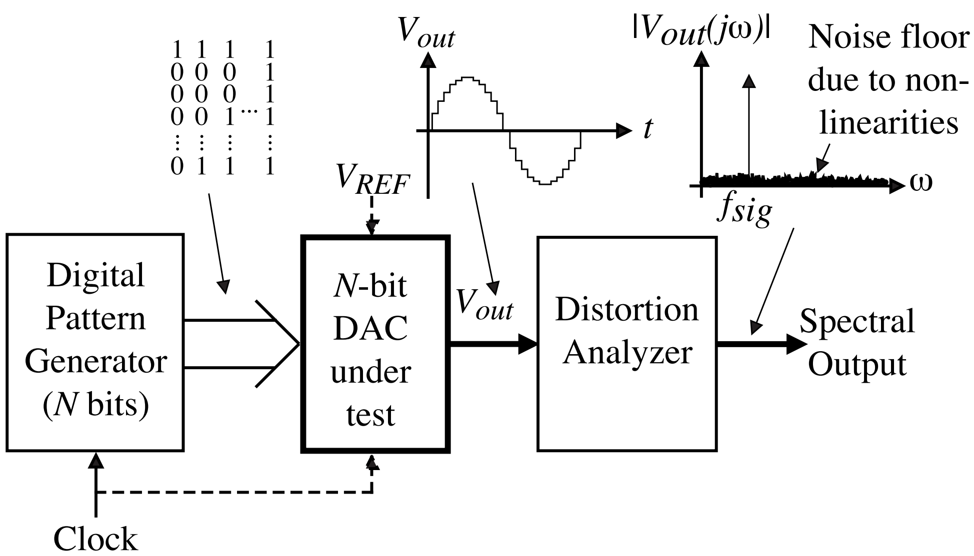
Fig. 10.5-6DL

INL and DNL in A/D converters



Example of *INL* and *DNL* for a 3-bit ADC.) Fig.10.5-5

Dynamic Testing of D/A Converters



Note that the noise contribution of *VREF* must be less than the noise floor due to nonlinearities.

Digital input pattern is selected to have a fundamental frequency which has a magnitude of at least $6N$ dB above its harmonics.

Length of the digital sequence determines the spectral purity of the fundamental frequency.

All nonlinearities of the DAC (i.e. *INL* and *DNL*) will cause harmonics of the fundamental frequency

The THD can be used to determine the SNR dB range between the magnitude of the fundamental and the THD. This SNR should be at least $6N$ dB to have an *INL* of less than $\pm 0.5LSB$ for an ENOB of N-bits.

If the period of the digital pattern is increased, the frequency dependence of *INL* can be measured.