CMOS Active Filters

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Mixed-Mode Electronic System

- Analog filters needed to suppress out-of-band noise and prevent aliasing. Also used, e.g., as loop filters in oversampled ADCs.
- Continuous-time filter allows sampling by discrete-time SCF. SCF performs sharper filtering; DSP filtering may be even sharper.





Frequency Range of Analog Filters

- Discrete active RC filters: 1 Hz 100 MHz
- On-chip continuous-time active filters: 10 Hz 1 GHz
- Switched-capacitor or switched-current filters:
 1 Hz 10 MHz
- Discrete LC: 10 Hz 1 GHz
- Distributed: 100 MHz 100 GHz



Accuracy Considerations

- The *absolute* accuracy of on-chip analog components is bad (10% - 50%). The *matching* accuracy of like elements is much better.
- In analog integrated circuits, on-chip Rs can be matched to each other typically within a few %, Cs within 0.05%, with careful layout. Transconductance (Gm) stages can be matched to about 10 - 30%.
- In an active RC filter, the time constant Tc is determined by RC products, accurate to only 20 – 50%. In a Gm-C filter, *Tc ~ C/Gm*, also inaccurate. Tuning may be used.
- In an SC filter, Tc ~ (C1/C2)/fc, where fc is the clock frequency. Tc accuracy may be 0.05% or better!



Classification of Filters

- Signal types: continuous-time vs. discrete-time filters;
- CT: signal is a continuous function of time. Laplace and Fourier transforms can be used for analysis. Example: Gm-C filters, SCFs in Sit.2 (slide 2).
- DT: only samples processed. Z-transform and DFT must be used. Example: SCFs in Sit.1 (slide 2).
- Signal representation: voltage, charge, current.
- Filter architectures: cascade vs. multi-feedback structures.



Active-RC Filters [1], [4], [5]

- Single-amplifier filters: Sallen-Key filter; Kerwin filter; Rauch filter, Deliyannis-Friend filter.
- Integrator-based filter sections: Tow-Thomas biquads; Ackerberg-Mossberg filter.
- Cascade design, dynamic range optimization.
- Simulated LC filters: gyrator-based and integrator-based filters; dynamic range optimization.



Single-opamp biquad. General diagram:

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 Amplifier not grounded. Common-mode changes with output. Differential implementation difficult.

Sallen-Key Filter

• Transfer function:

$$H(s) = \frac{V_2}{V_1} = \frac{KY_1Y_3}{(Y_1 + Y_2)(Y_3 + Y_4) + Y_3Y_4 - KY_2Y_3}$$

• Second-order transfer function (biquad) if two of the admittances are capacitive. Complex poles achieved by subtraction of term containing *K*.



Sallen-Key Filter

• Low-pass S-K filter (*R1, C2, R3, C4*):

$$H(s) = \frac{a_0}{b_2 s^2 + b_1 s + b_0}$$

- Highpass S-K filter (C1, R2, C3, R4): $H(s) = \frac{a_2 s^2}{b_2 s^2 + b_1 s + b_0}$
- Bandpass S-K filter (*R1, C2, C3, R4 or C1, R2, R3, C4*):

$$H(s) = \frac{a_1 s}{b_2 s^2 + b_1 s + b_0}$$



Sallen-Key Filter

- Pole frequency ω_0 : absolute value of natural mode;
- Pole Q: ωo/[2|real part of pole|]. Determines the stability, sensitivity, and noise gain. Q > 5 is dangerous, Q > 10 can be lethal! For S-K filter
- dQ/Q ~ (3Q –1) dK/K .So, if Q = 10, 1% error in K results in 30% error in Q.
- Pole Q tends to be high in band-pass filters so S-K may not be suitable for those.
- Usually only the peak gain, the Q and the pole frequency ωo are specified. There are 2 extra degrees of freedom. May be used for specified R noise, minimum total C, equal capacitors, or K = 1.
- Use differential difference amplifier for differential circuit.



Kerwin Filter

 Sallen-Key filters cannot realize finite imaginary zeros, needed for elliptic or inverse Chebyshev response.
 Kerwin filter can with Y = G or sC.



Y = G:

$$H(s) = \frac{K(s^2 + a^{-2})}{s^2 + (G + 2 - K)2a^{-1}s + (1 + 2G)a^{-2}}$$

Y = saC:

$$H(s) = \frac{[K/(2C+1)](s^2 + a^{-2})}{s^2 + [2a^{-1}(C+2-K)/(2C+1)]s + a^{-2}(2C+1)}$$



Deliyannis-Friend Filter [1]

Single-opamp bandpass filter:



- Grounded opamp, Vcm = 0. The circuit may be realized in a fully differential form suitable for noise cancellation. CM is analog ground.
- Finite gain slightly reduces gain factor and Q. Sensitivity is not too high even for high Q. Q → Q - K/A.



Deliyannis-Friend Filter [1]

For finite opamp gain:

$$H(s) = \frac{V2}{V1} = \frac{N(s)}{D(s)} = -\left(\frac{A}{1+A}\right) \frac{saG_1/C}{s^2 + s\left(\frac{2G_2}{C} + \frac{G_1/C}{1+A}\right) + \frac{G_1G_2}{C^2}}$$

For infinite opamp gain:

$$H(s) = -\frac{saCG_1}{s^2C^2 + 2sCG_2 + G_1G_2} = -\frac{saG_1/C}{s^2 + s2G_2/C + G_1G_2/C^2}$$



Deliyannis-Friend Filter

• Q may be enhanced using positive feedback:



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Opamp no longer grounded, Vcm not zero, no easy fully differential realization.



Rauch Filter [1]

• Often applied as anti-aliasing low-pass filter:



• Transfer function:

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$$H(s) = \frac{G_2 G_3 / (C_1 C_2)}{s^2 + s(G_1 + G_2 + G_3) / C_1 + G_1 G_2 / (C_1 C_2) + \varepsilon}$$

$$\varepsilon = \frac{1}{A} \left[s^2 + s \left(\frac{G_1 + G_2 + G_3}{C_1} + \frac{G_2}{C_2} \right) + \frac{(G_1 + G_3)G_2}{C_1 C_2} \right]$$

• Grounded opamp, may be realized fully differentially.



Tow-Thomas Biquad [1]

- Multi-opamp integrator-based biquads: lower sensitivities, better stability, and more versatile.
- They can be realized in fully differential form.
- The Tow-Thomas biquad is a sine-wave oscillator, stabilized by one or more additional element:



• In its differential form, the inverter is not required.



Tow-Thomas Biquad

• The transfer functions to the opamp outputs are

$$H_1(s) = -\frac{1/(R_3R_4C_1C_2)}{s^2 + s/(R_1C_1) + 1/(R_2R_4C_1C_2)}$$

$$H_2(s) = (-sC_2R_4) \times [-H_1(s)] = -\frac{(R_1R_3) \cdot s/(R_1C_1)}{s^2 + s/(R_1C_1) + 1/(R_2R_4C_1C_2)}$$

Other forms of damping are also possible. Preferable to damp the second stage, or (for high Q) to use a damping C across the feedback resistor. Zeros can be added by feed-forward input branches.



Ackerberg–Mossberg Filter [1]

• Similar to the Tow-Thomas biquad, but less sensitive to finite opamp gain effects.



• The inverter is not needed for fully differential realization. Then it becomes the Tow-Thomas structure.

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Cascade Filter Design [3], [5]

- Higher-order filter can constructed by cascading loworder ones. The *Hi(s)* are multiplied, provided the stage outputs are buffered.
- The *Hi(s)* can be obtained from the overall *H(s)* by factoring the numerator and denominator, and assigning conjugate zeros and poles to each biquad.
- Sharp peaks and dips in |*H*(*f*)| cause noise spurs in the output. So, dominant poles should be paired with the nearest zeros.



Cascade Filter Design [5]

- Ordering of sections in a cascade filter dictated by low noise and overload avoidance. Some rules of thumb:
- High-Q sections should be in the middle;
- First sections should be low-pass or band-pass, to suppress incoming high-frequency noise;
- All-pass sections should be near the input;
- Last stages should be high-pass or band-pass to avoid output dc offset.



Dynamic Range Optimization [3]

- Scaling for dynamic range optimization important in multiopamp filters.
- Active-RC structure:



 Op-amp output swing must remain in linear range, but as large as this permits to reduce noise gain from the stage to the filter output.



Dynamic Range Optimization

- Multiplying all impedances connected to the opamp *output* by *k*, the output voltage *Vout* becomes *k*.*Vout*, and all output currents remain unchanged.
- Choose *k*. *Vout* so that the maximum swing occupies the linear range of the opamp.
- Find the maximum swing in the time domain by plotting the histogram of *Vout* for a typical input, or in the frequency domain by sweeping the frequency of an input sine-wave to the filter, and compare *Vout* with the maximum swing of the output opamp.



Optimization in Frequency Domain



Impedance Level Scaling

- Lower impedance -> lower noise, more power needed!
- All admittances connected to the *input* node of the opamp may be multiplied by a convenient scale factor without changing the output voltage or output currents. This may be used, e.g., to minimize the area of capacitors.
- Impedance scaling should be done after dynamic range scaling!





Tunable Active-RC Filters [2], [3]

- Tolerance of RC time constants typically 30 ~ 50%, so the frequency response may not be acceptable.
- *R*s may be trimmed, or made variable and automatically tuned to obtain a time constant locked to the period *T* of a crystal-controlled clock signal.
- Simplest: replace Rs by MOSFETs operating in their linear (triode) region. MOSFET-C filters result.
- Compared to Gm-C filters, slower and need more power, but may be more linear, and easier to design.



Two-Transistor Integrators

Vc is the control voltage for the MOSFET resistors.





Two-Transistor Integrators

· For resistor integrator

$$v_{\text{diff}} = \frac{1}{sR_1C_I}(v_{p1} - v_{n1}) + \frac{1}{sR_2C_I}(v_{p2} - v_{n2})$$
(59)

- Negative integration cross-couple wires
- For MOSFET-C integrator

$$r_{DS} = \left(\mu_n C_{ox} \left(\frac{W}{L}\right) (v_{GS} - V_{tn})\right)^{-1}$$
(60)

leading to

$$v_{\text{diff}} = \frac{1}{sr_{DS1}C_I}(v_{p1} - v_{n1}) + \frac{1}{sr_{DS2}C_I}(v_{p2} - v_{n2})$$
(61)
$$r_{DSi} = \left(\mu_n C_{ox} \left(\frac{W}{L}\right)_i (V_C - V_x - V_{tn})\right)^{-1}$$
(62)



2**8**2

MOSFET-C Biquad Filter [2], [3]

• Tow-Thomas biquad:





Four-Transistor Integrator

 Improved linearity of MOSFET-C integrators by using 4 transistors rather than 2:



 May be analyzed by treating it as a two-input integrator with inputs (Vpi-Vni) and (Vni-Vpi).

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Four-Transistor Integrator

• If all four transistor are matched in size,

$$v_{\text{diff}} = v_{po} - v_{no} = \frac{1}{sr_{DS}C_{I}}(v_{pi} - v_{ni})$$
$$r_{DS} = \left(\mu_{n}C_{ox}\left(\frac{W}{L}\right)(V_{C1} - V_{C2})\right)^{-1}$$

- Model for drain-source current shows non-linear terms not dependent on controlling gate-voltage;
- All even and odd distortion products will cancel;
- Model only valid for older long-channel length technologies;
- In practice, about a 10 dB linearity improvement.



Tuning of Active-RC Filters

• *R*s may be automatically tuned to match to an accurate off-chip resistor, or to obtain an accurate time constant locked to the period *T* of a crystal-controlled clock signal:



 In equilibrium, R.C = T. Match Rs and Cs to the ones in the tuning stage using careful layout. Residual error 1-2%.

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Switched-R Filters [6]

- Replace tuned resistors by a combination of two resistors and a periodically opened/closed switch.
- Automatically tune the duty cycle of the switch:





Simulated LC Filters [3], [5]

 A doubly-terminated LC filter with near-optimum power transmission in its passband has low sensitivities to all L & C variations, since the output signal can only decrease if a parameter is changed from its nominal value.





Simulated LC Filters

• Simplest: replace all inductors by gyrator-C stages:



• Using transconductances:







Simulated LC Filters Using Integrators



(b)



Cascade vs. LC Simulation Design

 Cascade design: modular, easy to design, lay out, trouble-shoot. Passband sensitivities moderate (~0.3 dB), stopband sensitivities excellent, since stopband losses of the sections add.




Cascade vs. LC Simulation Design

- LC simulation: passband sensitivities (and hence noise suppression) excellent due to Orchard's Rule.
- Stopband sensitivities high, since suppression is only achieved by cancellation of large signals at the output:





Gm-C Filters [1], [2], [5]

- Alternative realization of tunable continuous-time filters: Gm-C filters.
- Faster than active-RC filters, since they use open-loop stages, and (usually) no opamps..
- Lower power, since the active blocks drive only capacitive loads.
- More difficult to achieve linear operation (no feedback).



Gm-C Integrator



- Uses a transconductor to realize an integrator;
- Output current of Gm is (ideally) linearly related to input voltage;
- Output impedance is ideally infinite.
- Gm is not an operational transconductance amplifier (OTA) which has a high Gm value but is not very linear.



Multiple-Input Gm-C Integrator

• Can process several inputs:



$$V_o = \frac{1}{sC_1} (G_{m1}V_1 - G_{m2}V_2 + G_{m3}V_3)$$



Fully-Differential Integrators

• Better noise and linearity than for single-ended operation:



- Uses a single capacitor between differential outputs.
- Requires some sort of common-mode feedback to set output common-mode voltage.
- Needs some extra capacitors for compensating the common-mode feedback loop.



Fully-Differential Integrators

$$v_{i} \stackrel{+}{\xrightarrow{}}_{-\infty} \stackrel{+}{\xrightarrow{}}_{+} \stackrel{+}{\xrightarrow{}}_{-\infty} \stackrel{+}{\xrightarrow{}_{-\infty} \stackrel{+}{\xrightarrow{}}_{-\infty} \stackrel{+}{\xrightarrow{}_{-\infty} \stackrel{+}{\xrightarrow{}}_{-\infty} \stackrel$$

- Uses two grounded capacitors;
- Still requires common-mode feedback but here the compensation capacitors for the common-mode feedback can be the same grounded capacitors as used for the signal.



Fully-Differential Integrators



- Integrated capacitors have top and bottom plate parasitic capacitances.
- To maintain symmetry, usually two parallel capacitors turned around are used, as shown above.
- Note that parasitic capacitance affects the time constant.



Gm-C-Opamp Integrator



- Uses an extra opamp to improve linearity and noise performance.
- Output is now buffered.



Gm-C-Opamp Integrator

Advantages

- Effect of parasitics reduced by opamp gain —more accurate time constant and better linearity.
- Less sensitive to noise pick-up, since transconductor output is low impedance (due to opamp feedback).
- *Gm* cell drives virtual ground output impedance of *Gm* cell can be lower, and smaller voltage swing is needed.

Disadvantages

- Lower operating speed because it now relies on feedback;
- Larger power dissipation;
- Larger silicon area.



A Simple Gm-C Opamp Integrator

•Pseudo-differential operation. Simple opamp:



• A low input impedance on the order of $2/(g_{m2}^2 r_{ds})$ due to common-gate input impedance and feedback.

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First-Order Gm-C Filter



General first-order transfer-function

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{k_1 s + k_0}{s + \omega_0}$$

- Built with a single integrator and two feed-in branches.
- ω_0 sets the pole frequency



First-Order Filter



• Transfer function is given by

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{sC_X + G_{m1}}{s(C_A + C_X) + G_{m2}} = \frac{s\left(\frac{C_X}{C_A + C_X}\right) + \left(\frac{G_{m1}}{C_A + C_X}\right)}{s + \left(\frac{G_{m2}}{C_A + C_X}\right)}$$
(5)



Fully-Differential First-Order Filter



- Same equations as for single-ended case, but capacitor sizes are doubled.
- 3 coefficients, 4 parameters. May make Gm1 = Gm2.
- Can also realize K1 < 0 by cross-coupling wires at Cx.



• Tow-Thomas biquad:





 Fully differential realization:





•Transfer function:

$$H(s) = \frac{V_{out}(s)}{V_{in}(s)} = \frac{s^2 \left(\frac{C_X}{C_X + C_B}\right) + s \left(\frac{G_{m5}}{C_X + C_B}\right) + \left(\frac{G_{m2}G_{m4}}{C_A(C_X + C_B)}\right)}{s^2 + s \left(\frac{G_{m3}}{C_X + C_B}\right) + \left(\frac{G_{m1}G_{m2}}{C_A(C_X + C_B)}\right)}$$
(12)

- There is a restriction on the high-frequency gain coefficients *k*₂, just as in the first-order case (not for differential realization).
- *Gm*³ sets the damping of the biquad.
- G_{m1} and G_{m2} form two integrators, with unity-gain frequencies of ω_0/s .



- 5 coefficients to match in *H(s)*, 8 designable parameters (5 *Gm*s, 3 capacitances).
- Extra degrees of freedom may be used for dynamic range at internal node and impedance scaling, and for using matched Gm blocks.
- In cascade design, the input admittance *Yin* is important. If Cx = 0, *Yin* = 0. Otherwise, it is *Yin* = sCx [1 - H(s)].
- Yin may be absorbed in the previous stage's output capacitor CB.



Scaling of Cascade Gm-C Filter

- In a cascade of biquads, H(s) = H1(s).H2(s). Before realization, scale all Hi(s) so that the maximum output swings are the largest allowable. This takes care of the output swings of Gm2, Gm3, and Gm5.
- Multiply *Gm1* and *Gm4*, or divide *CA*, by the desired voltage scale factor for the internal capacitor *CA*. This takes care of the output swings of *Gm1* and *GM4*.
- It is possible to multiply the *Gm*s and capacitors of both integrators by any constant, to scale the impedances of the circuit at a convenient level (noise vs. chip area and power).



References

- [1] R. Schaumann et al., Design of Analog Filters (2nd edition), Oxford University Press, 2010.
- [2] D. A. Johns and K. Martin, Analog Integrated Circuits, Wiley, 1997.
- [3] R. Gregorian and G. C. Temes, Analog MOS Integrated Circuits for Signal Processing, Wiley, 1986.
- [4] Introduction to Circuit Synthesis and Design, G. C. Temes and J. W. LaPatra, McGraw-Hill, 1977.
- [5] John Khoury, Integrated Continuous-Time Filters, Unpublished Lecture Notes, EPFL, 1998.
- [6] P. Kurahashi et al., "A 0.6-V Highly Linear Switched-R-MOSFET-C Filter, CICC, Sept. 2006, pp. 833-836.



Switched-Capacitor Filters

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Switched-Capacitor Circuit Techniques [2], [3]

- Signal entered and read out as voltages, but processed internally as charges on capacitors. Since CMOS reserves charges well, high SNR and linearity possible.
- Replaces absolute accuracy of R & C (10-30%) with matching accuracy of C (0.05-0.2%);
- Can realize accurate and tunable large RC time constants;
- Can realize high-order dynamic range circuits with high dynamic range;
- Allows medium-accuracy data conversion without trimming;
- Can realize large mixed-mode systems for telephony, audio, aerospace, physics etc. Applications on a single CMOS chip.
- Tilted the MOS VS. BJT contest decisively.



- Switched-current circuitry: Can be simpler and faster, but achieves lower dynamic range & much more THD; Needs more power. Can use basic digital technology; now SC can too!
- Continuous-time filters: much faster, less linear, less accurate, lower dynamic range. Need tuning.



LCR Filters to Active-RC Filters

INDUCTORS REPLACED BY R,C,OP-AMP BLOCKS. SPACE REQUIREMENT FOR TELEPHONE FILTERS REDUCED FROM 3"x3"x.5" TO ABOUT 1.5"x1.5"x.2", OR LESS WITH THICK FILM IMPLEMENTATION.





(b)



Typical Applications of SC Technology – (1)

Line-Powered Systems:

- Telecom systems (telephone, radio, video, audio)
- Digital/analog interfaces
- Smart sensors
- Instrumentation
- Neural nets.
- Music synthesizer



Typical Applications of SC Technology – (2)

Battery-Powered Micropower Systems:

- Watches
- Calculators
- Hearing aids
- Pagers
- Implantable medical devices
- Portable instruments, sensors
- Nuclear array sensors (micropower, may not be battery powered)



New SC Circuit Techniques

To improve accuracy:

- Oversampling, noise shaping
- Dynamic matching
- Digital correction
- Self-calibration
- Offset/gain compensation

To improve speed, selectivity:

- GaAs technology
- BiCMOS technology
- N-path, multirate circuits



Typical SC Stages

- Amplifiers: Programmable, precision, AGC, buffer, driver, sense
- Filters
- S/H and T/H stages
- MUX and deMUX stages
- PLLs
- VCOs
- Modulators, demodulators
- Precision comparators
- Attenuators
- ADC/DAC blocks



Active - RC Integrator



Can be transformed by replacing R1 by an SC branch.





SC Integrator (Analog Accumulator)

Stray insensitive version:



Figure 5.9 (a) active RC integrator; (b) stray-insensitive switched-capacitor integrator circuit; (c) clock signals; (d) output voltage waveform.



SC Integrator (Analog Accumulator)





Low-Q SC Biquad – (1)





Low-Q SC Biquad – (2)







Low-Q SC Biquad – (3)

Approximate design equations for $\omega_0 T \ll 1$:

$$(\omega_0 T)^2 \cong \frac{C_2 C_3}{1 + C_4 / 2} <<1 \qquad R = T / C$$

$$Q \cong \frac{\omega_0 T}{C_4 / C_{A,B}} \qquad \text{If } Q > 1 \quad C_4 \text{ very small!}$$

$$DC \text{ gain} \cong \frac{C_1}{C_2} \qquad \frac{C_4}{C_A} \sim \frac{\omega_0 T}{Q} <<1$$

$$C_A = C_B \equiv 1$$

$$C_2 = C_3 \qquad \text{for minimum spread} \sim \omega_0 T$$
Exact equations:

$$H(z) = -\frac{a_2 z^2 + a_1 z + a_0}{b_2 z^2 + b_1 z + b_0} = -\frac{(C_1' + C_1'') z^2 + (C_1 C_3 - C_1' - 2C_1'') z + C_1''}{(1 + C_4) z^2 + (C_2 C_3 - C_4 - 2) z + 1}$$



Low-Q SC Biquad – (4)

For b₀ = 1, matching coefficients:

$$C_1'' = a_0$$
$$C_1' = a_2 - a_0$$
$$C_4 = b_2 - 1$$

$$C_2C_3 = 1 + b_1 + b_2 \rightarrow C_2 = C_3 = \sqrt{1 + b_1 + b_2}$$

 $C_1 = (a_0 + a_1 + a_2) / C_3$

Preliminary C_i values. Scaling to follow!



High-Q Biquad – (1)



(a) High Q switched-capacitor biquad; (b) clock and signal waveform



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High-Q Biquad – (2)

$$\frac{V_{out}}{V_{in}} = H(z) = \frac{a_m z^m + a_{m-1} z^{m-1} + \cdots}{V_{in}}$$

H, z both dimensionless $\leftarrow z = e^{st}$ $a_m = f(C_1, C_2, \cdots) = f'\left(\frac{C_1}{C_2} \cdots\right)$

Approximate design equations :

$$(\omega_0 T)^2 \cong C_2 C_3 <<1 \qquad \left(\frac{C_2 C_3}{C_A C_B}\right)$$
$$Q \cong 1 / C_4 \quad (C_A / C_4)$$
$$DC \text{ Gain} = \frac{C_1}{C_2}$$
$$Good \text{ choice} : \begin{array}{c} C_2 = C_3 \cong \omega_0 T <<1 \\ C_4 \cong 1 / Q > C_2 \end{array}$$

Then, $C_{\text{max}} / C_{\text{min}} \sim 1 / \omega_0 T$ as before.


High-Q Biquad – (3)

Exact equations:

$$H(z) = \frac{V_{out}(z)}{V_{in}(z)} = -\frac{C_1''z^2 + (C_1C_3 + C_1'C_3 - 2C_1'')z + (C_1'' - C_1'C_3)}{z^2 + (C_2C_3 + C_3C_4 - 2)z + (1 - C_3C_4) \leftarrow (z - 1)^2}$$

For $b_2 = 1$, coefficient matching gives C spread & sensitivities reasonable even for high $Q \& f_c/f_o$, since C_2 , C_3 , C_4 enter only in products:

$$C_{1}^{"} = a_{2} \qquad C_{4} = \frac{1 - b_{0}}{C_{3}}$$

$$C_{1}^{'} = \frac{a_{2} - a_{0}}{C_{3}} \qquad C_{2}C_{3} = 1 + b_{0} + b_{1}$$

$$C_{1} = \frac{a_{0} + a_{1} + a_{2}}{C_{3}} \qquad C_{2} = C_{3} = \sqrt{1 + b_{0} + b_{1}}$$



Linear Section – (1)





Linear Section – (2)

For fully differential circuit, less restrictions.

Stray insensitive branch shown below (cannot be used as feedback branch!).





Cascade Design – (1)







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Cascade Design – (2)

Easy to design, layout, test, debug, <u>Passband</u> sensitivities "moderate," *Sens* = 0.1 - 0.3 dB/% in passband. <u>Stopband</u> sensitivities good. Pairing of num. & denom., ordering of sections all affect S/N, element spread and sensitivities.





Cascade Design – (3)

Cascade Order

$$\begin{array}{c} VI \\ O \\ H_{t}(S) \\ H_{t}(S) \\ H_{t}(S) \\ H_{t}(S) \\ \end{array}$$

Many factors practical factors influence the optimum ordering. A few examples [5]:

1.Order the cascade to equalize signal swing as much as possible for dynamic range considerations

3.Choose the first biquad to be a lowpass or bandpass to reject high frequency noise, to prevent overload in the remaining stages.

3. If the offset at the filter output is critical, the last stage should be a highpass or bandpass to reject the DC of previous stages



Cascade Design – (4)

- The last stage should NOT in general be high Q because these stages tend to have higher fundamental noise and worse sensitivity to power supply noise
- 6. In general do not place allpass stages at the end of the cascade because these have wideband noise. It is usually best to place allpass stages towards the beginning of the filter.
- 8. If several highpass or bandpass stages are available one can place them at the beginning, middle and end of the filter. This will prevent input offset from overloading the filter, will prevent internal offsets of the filter itself from accumulating (and hence decreasing available signal swing) and will provide a filter output with low offset.
- The effect of thermal noise at the filter output varies with ordering; therefore, by reordering several dB of SNR can often be gained. (John Khouri, unpublished notes)



Ladder Filter

For optimum passband matching, for nominal $\partial V_o / \partial x \sim 0$ since V_o is maximum *x* values. *x*: any L or C.



Use doubly-terminated LCR filter prototype, with 0 flat passband loss. **State equations:** $V = -\frac{1}{V_m} \left[\frac{V_m - V_1}{V_m - V_1} + sC_n V_n - I_n \right]_{KCL@,1}$

$$-V_{1} = \frac{1}{s(C_{1} + C_{2})} \left[\frac{1}{R_{s}} + sC_{2}V_{3} - I_{2} \right] KCL(e)$$
$$-I_{2} = \frac{-1}{sL_{2}} \left[V_{1} - V_{3} \right] KVL$$
$$V_{3} = \frac{-1}{s(C_{2} + C_{3})} \left[-sC_{2}V_{1} - I_{2} + \frac{V_{3}}{R_{L}} \right] KCL@3$$



The Exact Design of SC Ladder Filters

Purpose: $H_a(s_a) \leftrightarrow H(z)$, where $s_a = \frac{2}{T} \frac{z-1}{z+1}$.

Then, gain response is only frequency warped.



has a simple z-domain realization.



S_a-domain block diagram



Realization of input branch: $Q_{in} = V_{in}/s_a R_s$, which becomes, $Q_{in}(z) = \frac{T}{2} \frac{(z+1)}{(z-1)} \frac{V_{in}(z)}{R_s}$

This relation can be rewritten in the form $\Delta Q_{in} = (1 - z^{-1})Q_{in}(z) = \frac{T}{2R_s}(1 + z^{-1})V_{in}(z)$ or, in the time domain $\Delta q_{in}(t_n) = q_{in}(t_n) - q_{in}(t_{n-1}) = \frac{C_s}{2} \left[v_{in}(t_n) + v_{in}(t_{n-1}) \right].$ $\Delta q_{in}(t_n) : \text{ incremental charge flow during } t_{n-1} < t < t_n, \text{ in SCF.}$

Oregon State

Final Circuit





Damping resistors in input & output stages – (2)

Using bandpass realization tables to obtain low-pass response gives an extra op-amp, which can be eliminated:



Sixth-order bandpass filter: LCR prototype and SC realization.





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Scaling for Optimal DR and Chip Area – (1)



To modify $V_o \rightarrow kV_o$; $Y_i/Y_f \rightarrow kY_i/Y_f \forall i$. Hence, change Y_f to Y_f/k or Y_i to kY_i . (It doesn't matter which; area scaling makes the results the same.) To keep all output currents unchanged, also $Y_a \rightarrow Y_a/k$, etc.

Noise gain:
$$V_{on} = V_0 \Big|_{V_i = 0 \quad \forall i} = V_n + \frac{I_n}{Y_f} = V_n \left[1 + \frac{\sum_{i} Y_i}{Y_f} \right]$$



Scaling for Optimal DR and Chip Area – (2)

Hence, $V'_{on} = \frac{1+k\sum_{i}Y_{i}/Y_{f}}{1+\sum_{i}Y_{i}/Y_{f}}V_{on}$. The output noise currents are also divided

by \underline{k} , due to $Y'_a = Y_a/k$, etc. Hence, the overall output noise from this stage changes by a factor





Scaling for Optimal DR and Chip Area – (3)

The output signal does not change, so the SNR improves with increasing \underline{k} . However, the noise reduction is slower than 1/k, and also this noise is only one of the terms in the output noise power.

If $V_o > V_{DD}$, distortion occurs, hence $k \le k_{max}$ is limited such that Y_o saturates for the same V_{in} as the overall V_{out} . Any $k > k_{max}$ forces the input signal to be reduced by \underline{k} so the SNR will now decrease with \underline{k} .

<u>Conclusion:</u> k_{max} is optimum.



Scaling of SCF's. – (1)

Purposes :

- 1. Maximum dynamic range
- 2. Minimum C_{max} / C_{min} , $\sum C / C_{min}$,
- 3. Minimum sens. to op-amp dc gain effects.

1. Dynamic range



Assume that opamps have same input noise v_n^2 , and max. linear range $|V_{max}|$. For an optimum dynamic range $V_{in max} / V_{in min}$, each opamp should have the same $V_{imax}(f)$, so they all saturate at the same $V_{in max}$. Otherwise, the *S*/ *N* of the op-amp is not optimal.



Scaling of SCF's. – (2)



To achieve $V_{1 max} = V_{2 max} = \cdots = V_{out max}$, use amplitude scaling:



Figure 5.17 SC filter section.



Scaling of SCF's. – (3)

Simple rule:

Multiply all C_j connected or switched to the output of opamp *i* by k_i !





Scaling of SCF's. – (4)

2. Minimum C_{max}/C_{min:}

If all $f_n(z) & h(z)$ are multiplied by the same l_i , nothing will not change. Choose $l_i = C_{min} / C_{i \min}$ where $C_{i \min}$ is the smallest Cconnected to the input of op-amp \underline{i} , and C_{min} is the smallest value of cap. permitted by the technology (usually $0.1 \ pF \le C_{min} \le 0.5 \ pF$ for strayinsensitive circuits). Big effect on C_{max} / C_{min} !

3. Sensitivities:

The sensitivity of the gain to C_k remain unchanged by scaling; the sens. To op-amp gain effects are very much affected. Optimum dynamic-range scaling is nearly optimal for dc gain sens. as well.



Scaling of SCF's. – (5)



FIGURE 5.36. Sixth-order bandpass filter: (a) LCR prototype; (b) SC realization.



Scaling of SCF's. – (6)





Scaling of SCF's. – (7)





Scaling of SCF's. – (8)





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SC Filters in Mixed-Mode System

Two situations; example:



Situation 1: Only the sampled values of the output waveform matter; the output spectrum may be limited by the DSP, and hence $V_{RMS,n}$ reduced.

Situation 2: The complete output waveform affects the *SNR*, including the S/H and direct noise components. Usually the S/H dominates. Reduced by the reconstruction filter.



Direct-Charge-Transfer Stage – (1)



Advantages:

Opamp does not participate in charge transfer \rightarrow no slewing distortion, clean S/H output waveform. Finite DC gain A, introduces only a scale factor $K = 1/[1+1/A_o]$.



Direct-Charge-Transfer Stage – (2)

Analysis gives

$$V_o'(z) = K \cdot \left[V_{o,ideal}'(z) + V_n(z) \right]$$

where
$$V'_{o,ideal} = [C_1 \cdot V_1(z) + C_2 \cdot V_2(z)] / [(C + C_1 + C_2) - C/z]$$

is the ideal lowpass filter response.

Applications:

•SC-to-CT buffer in smoothing filter for D-S DAC (Sooch et al., AES Conv., Oct. 1991)

•DAC + FIR filter + IIR filter (Fujimori et al., JSSC, Aug. 2000).



Double Sampled Data Converter – (1)

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Low-Voltage Double-Sampled $\Sigma\Delta$ Converters

Daniel Senderowicz, Member, IEEE, Germano Nicollini, Sergio Pernici, Angelo Nagari, Member, IEEE, Pierangelo Confalonieri, and Carlo Dallavalle, Member, IEEE



Fig. 2. (a) Simplified conventional double-sampled SC integrator. (b) Equivalent conventional double-sampled SC integrator.



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